Lithography

Peter Hadley

BYU Basic Lithography Tutorial

Basic Lithography

A Simple Tutorial

Start Over   Previous   Next

http://www.cleanroom.byu.edu/virtual_cleanroom.parts/Lithography.html

SU-8 Processing

1. Substrate Pretreat

1. Clean wafer/substrate
2. Dehydration Bake - 200° C for at least 5 minutes
3. **BYU Dehydration Bake - 150° C for 15 minutes
4. (Optional) Apply Omnicoat

2. Spin Coat

1. Put wafer in spinner and set spin speed for desired thickness - see table for more information
2. Microchem recommends: ramp to 500 rpm at 100 rpm/second then ramp to the final speed at 300 rpm/second and hold final speed for 30 seconds
3. **BYU 5 µm SU-8 10 core: 500 rpm at 100 rpm/sec (6 sec) then 4400 rpm at 1200 rpm/sec (60 sec) and 6000 rpm at 6000 rpm/sec (2 sec) to remove edge beads
4. Apply approximately 1ml of SU-8 per inch of substrate diameter to the center of wafer
5. Spin to spread out the SU-8
6. After applying the SU-8, avoid grasping the wafer with tweezers, as this will push up ridges in the SU-8.

3. Softbake

1. Pre-bake the wafer at 65° C
2. Ramp to 95° C and bake for more time
3. A hot plate is the recommended baking method
4. **BYU tip: cool back down to 65° C on the hotplate then to room temperature on a level nonmetal surface
5. For bake times see the table

http://www.cleanroom.byu.edu/su8.phtml

Spin coater

Photoresist is applied to the wafer by spin coating or spray coating.

Spin Speed and Thickness

Tables of various photoresists used in the BYU Cleanroom. These tables are rough estimates of photoresist thicknesses obtained at different spin speeds.
NOTE: When changing the thickness of the photoresist layer the appropriate exposure time and developing time will change as well.

AZ 3312

Spin Speed (rpm)	Thickness (nm)
1000	2200
2000	1550
3000	1250
4000	1100
5000	950
6000	900

AZ 3330

Spin Speed (rpm)	Thickness (nm)
1000	5250
2000	3700
3000	3000
4000	2500
5000	2300
6000	2100

Shipley 1.2L

Spin Speed (rpm)	Thickness (nm)
2000	1900
3000	1590
4000	1400
5000	1300
6000	1200
7000	1020

Shipley 1.8L

Spin Speed (rpm)	Thickness (nm)
2000	2800
3000	2300
4000	2000
5000	1800
6000	1620
7000	1550

SU-8 5

Spin Speed (rpm)	Thickness (nm)
1000	7000
2000	4000
3000	3250
4000	2700
5000	2400
6000	2200

SU-8 10

Spin Speed (rpm)	Thickness (nm)
1000	-
2000	-
3000	-
4000	-
5000	-
6000	-

SU-8 25

Spin Speed (rpm)	Thickness (nm)
1000	32000
2000	13000
3000	9500
4000	7500
5000	7000
6000	6600

nLOF 2020

Spin Speed (rpm)	Thickness (nm)
1000	3400
2000	2350
3000	1900
4000	1700

http://www.cleanroom.byu.edu/thickness.phtml

4. Exposure

1. SU-8 is optimized for near UV (350-400nm) exposure
2. For best results energy below 350nm should be filtered out
3. Expose the wafer to UV light on an aligner
4. If the time is too short, the features will come off during development
5. Overexposure will increase the width of features
6. Thicker SU-8 requires more exposure energy
7. For more information on exposure energy check the MicroChem datasheets in the "Links and Datasheets" section

5. Post Exposure Bake (PEB)

1. Bake the wafer at 65° C
2. Slowly ramp to 95° C and bake for more time
3. A hot plate is the recommended baking method
4. Do not rapidly cool the wafer after the PEB
5. **BYU tip: cool back down to 65° C on the hotplate then to room temperature on a level nonmetal surface
6. For bake times see the table

6. Development

1. Pour some SU-8 developer into a glass dish
2. Place the wafer in the developer and gently agitate the developer the whole time
3. Strong agitation is recommended for structures with a high aspect ratio or large thickness
4. Development rates vary widely with agitation, temperature, and other processing parameters
5. Pour the SU-8 developer into the waste container and rinse the dish with IPA when finished
6. Typical development times are in the table

http://www.cleanroom.byu.edu/su8.phtml

7. Rinse and Dry

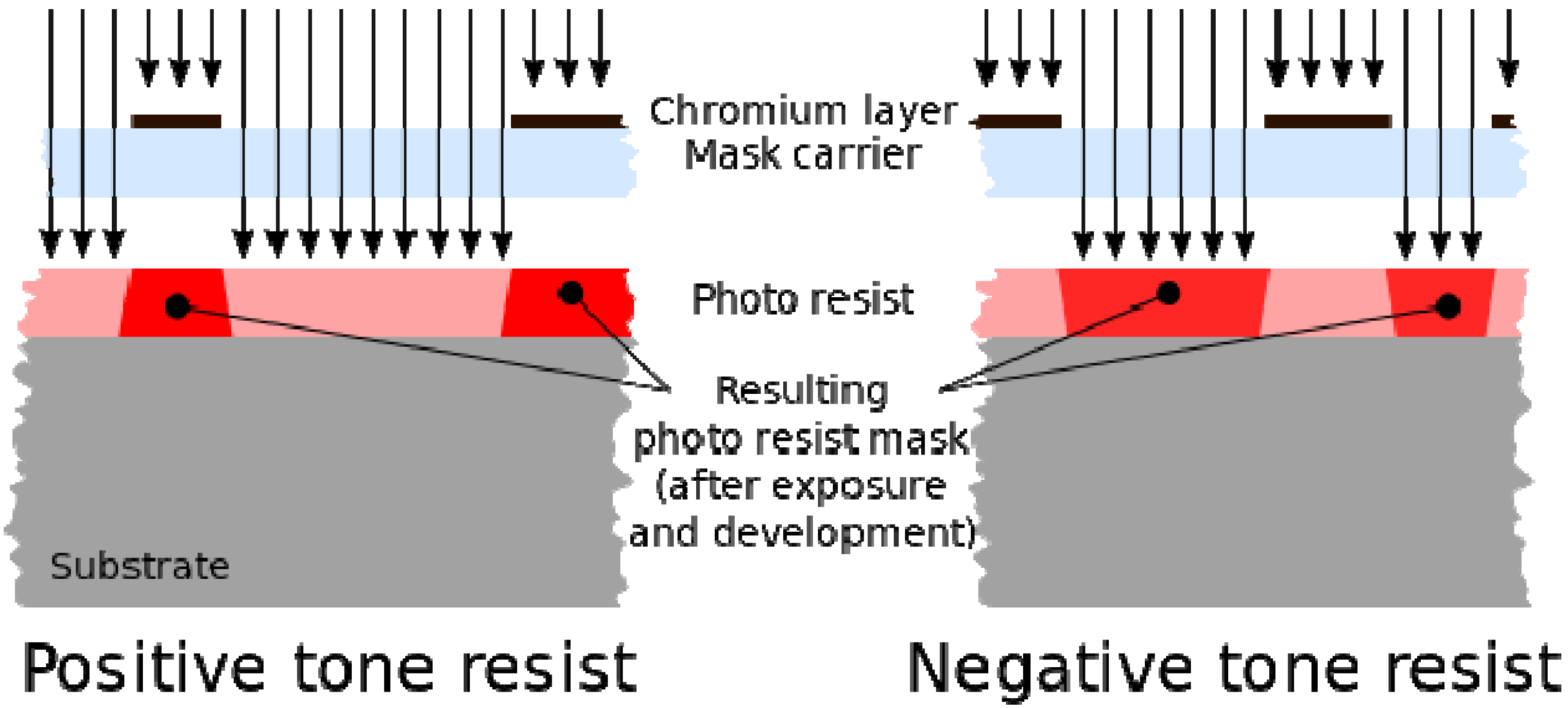
1. Rinse the wafer with IPA
2. If a white film is visible while rinsing then more development is needed
3. Dry with a nitrogen gun

8. Hard Bake/Cure(optional)

1. A hard bake is recommended if the SU-8 is to be left on as part of the final device or if there will be further thermal processing
2. A hard bake may also help to anneal any surface cracks after development
3. Typical hard bake temperatures are in the range of 150 °C to 250 °C
4. Typical times are between 5 and 30 minutes
5. Better results seem to be achieved by ramping from room temperature to the bake temperature and then ramping back down
6. **BYU 5 µm core process:
7. **Hard bake 1 - ramp on hotplate from RT to 200°C, bake at 200°C 10 min, ramp down to 95°C
8. **Descum - PE2, 90 sec 50 W, 100 sccm Oxygen
9. **Hard bake 2 - ramp on hotplate from RT to 250°C, bake at 250°C 5 min, ramp down to 95°C

http://www.cleanroom.byu.edu/su8.phtml

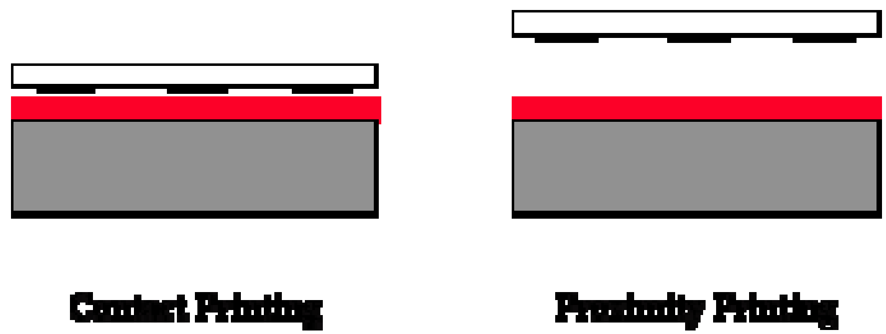
Positive / negative resist



http://en.wikipedia.org/wiki/Photoresist#mediaviewer/File:Comparison_positive_negative_tone_resist.svg

Optical Lithography

Contact printing, proximity printing with a mask aligner

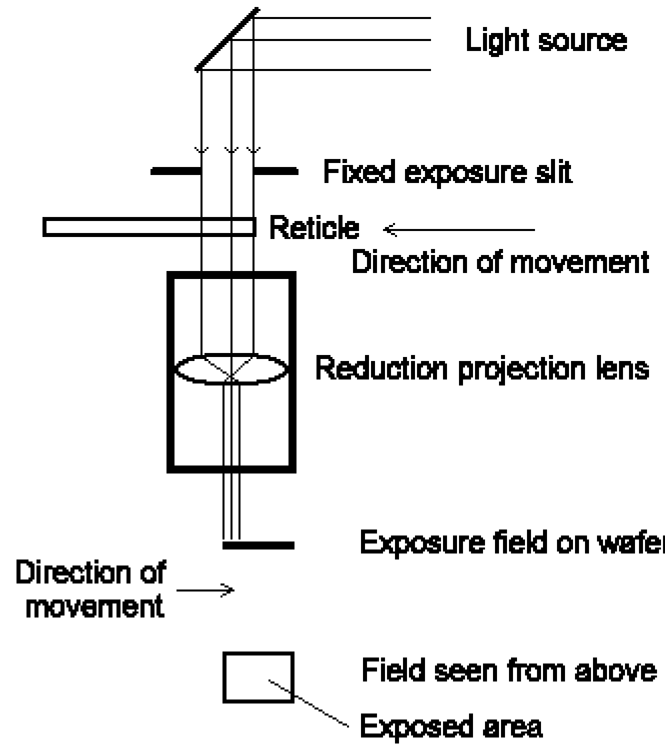


http://www.lithoguru.com/scientist/lithobasics.html

http://www2.warwick.ac.uk/fac/sci/eng/research/sensors/mbl/facilities/

Optical Lithography

Projection lithography with a stepper or scanner.



http://en.wikipedia.org/wiki/Stepper#/media/File:Scanendnew.gif

http://www.lithoguru.com/scientist/lithobasics.html

Resist over topography

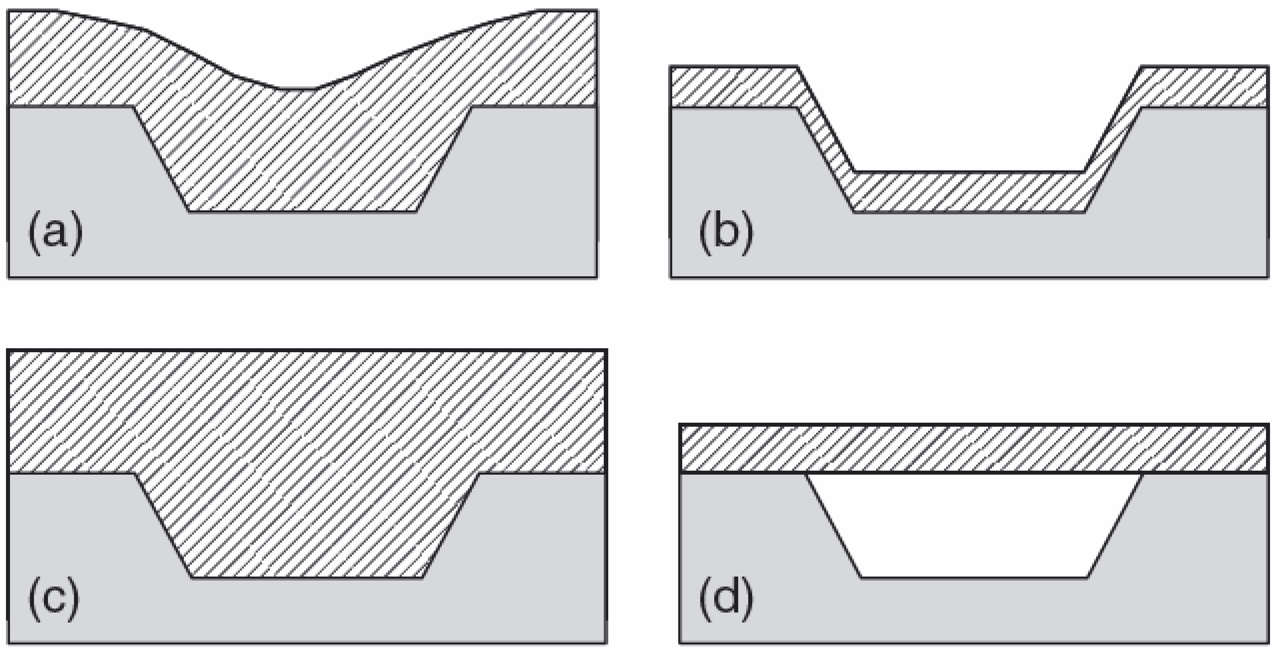


Figure 9.8 Resist over topography: (a) spin coated; (b) spray coated; (c) cast; (d) laminated dry film

Dose test

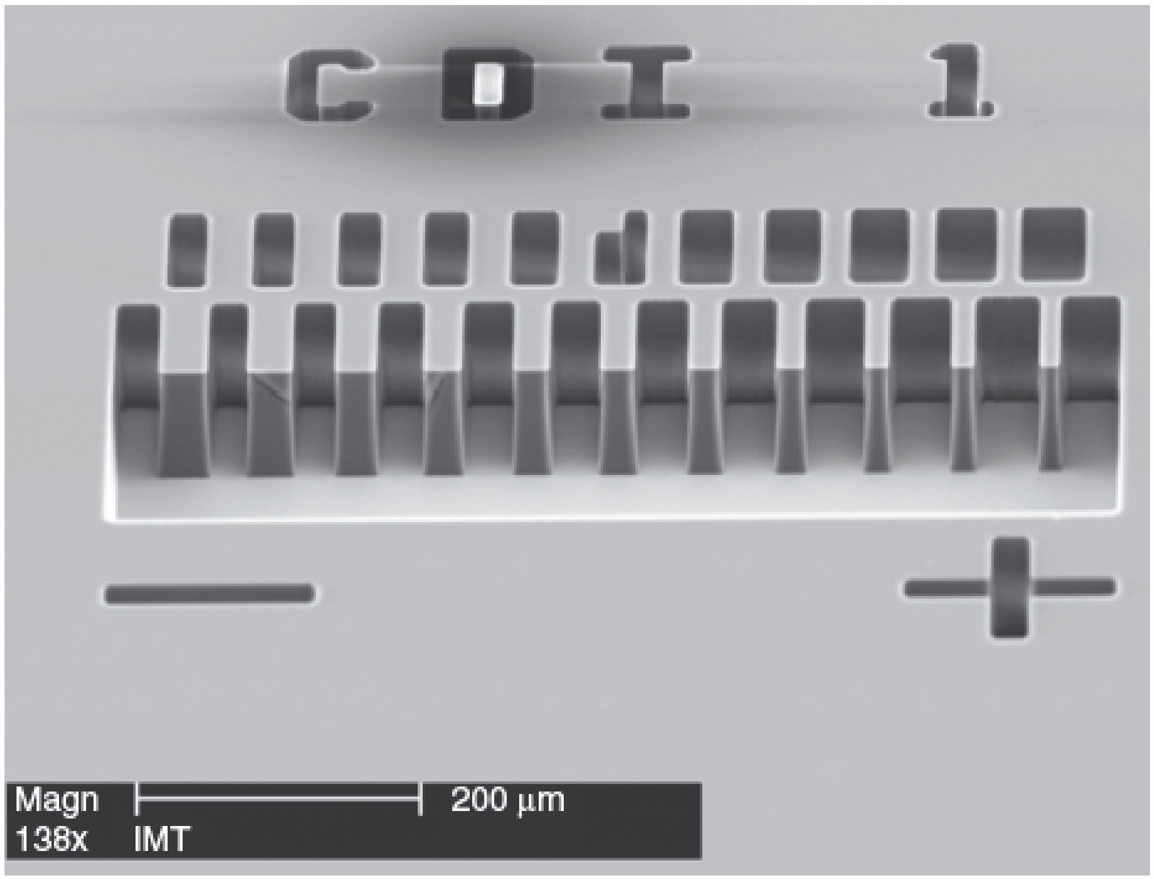


Figure 9.6 Linewidth test structure of positive photoresist in SEM micrograph. Reproduced from Roth *et al.* (1999)

Clean room

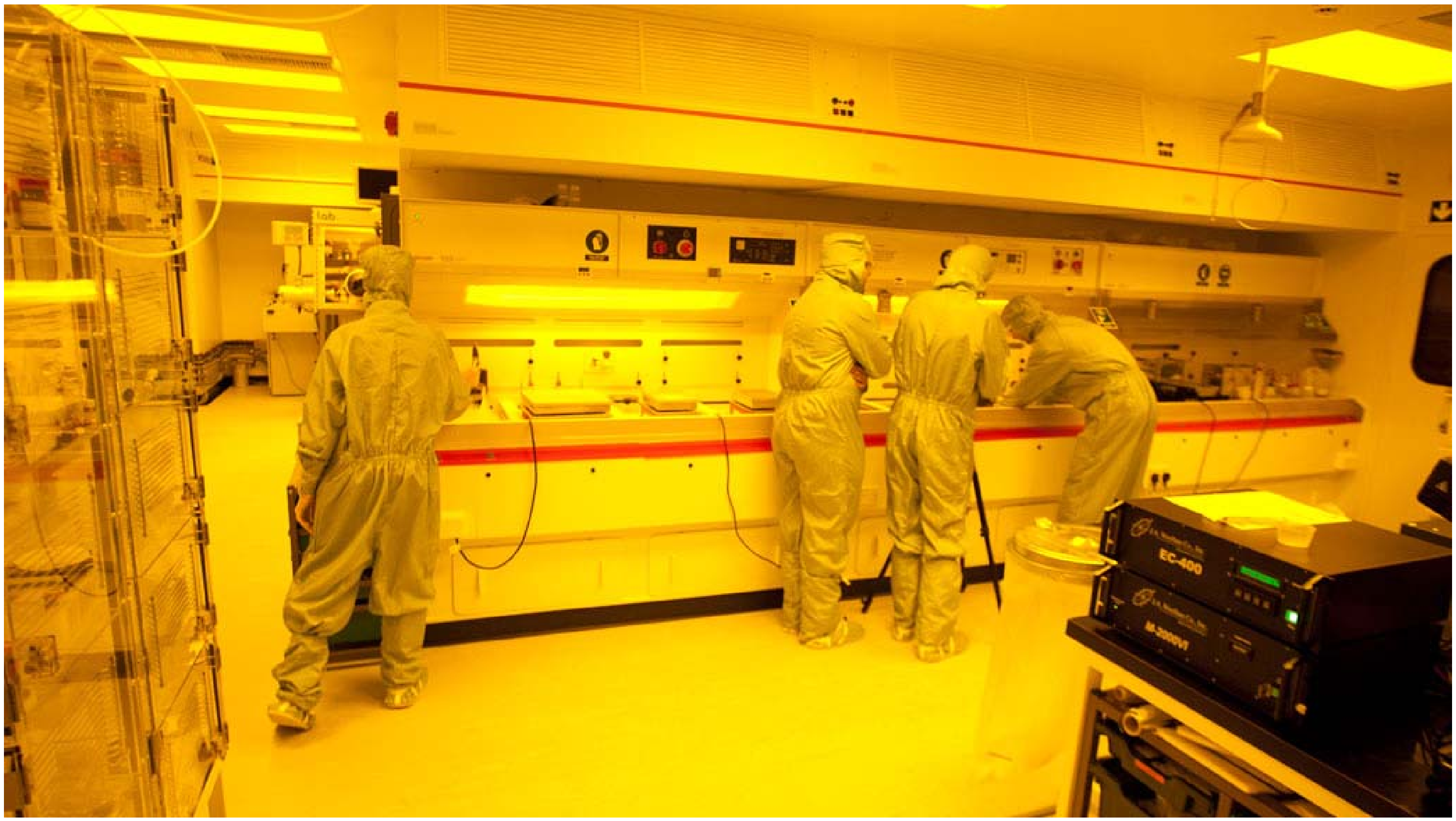


Table 9.1 Resist requirements for different applications

Ion implantation:

- resist thickness of 1 μm will stop B, P, As, Sb ions with <200 keV energy
- beam current heats resist: cooling or current limitation are needed
- resist carbonizes under heavy doses ($>10^{15}\,cm^{-2}$), difficult to remove

Wet etching:

- resist adhesion is important, resist may peel off
- resist will not tolerate strong acids or alkaline etch solutions
- hot etch baths degrade resist fast

Molding:

- smooth surface
- non-negative profile
- minimize chemical reactions with polymers

Table 9.1 Resist requirements for different applications

Plasma etching:

- resist will be etched in plasma: its size and shape will change
- resist will be damaged by plasma (both bombardment and thermal effects)
- removal of damaged resist is difficult

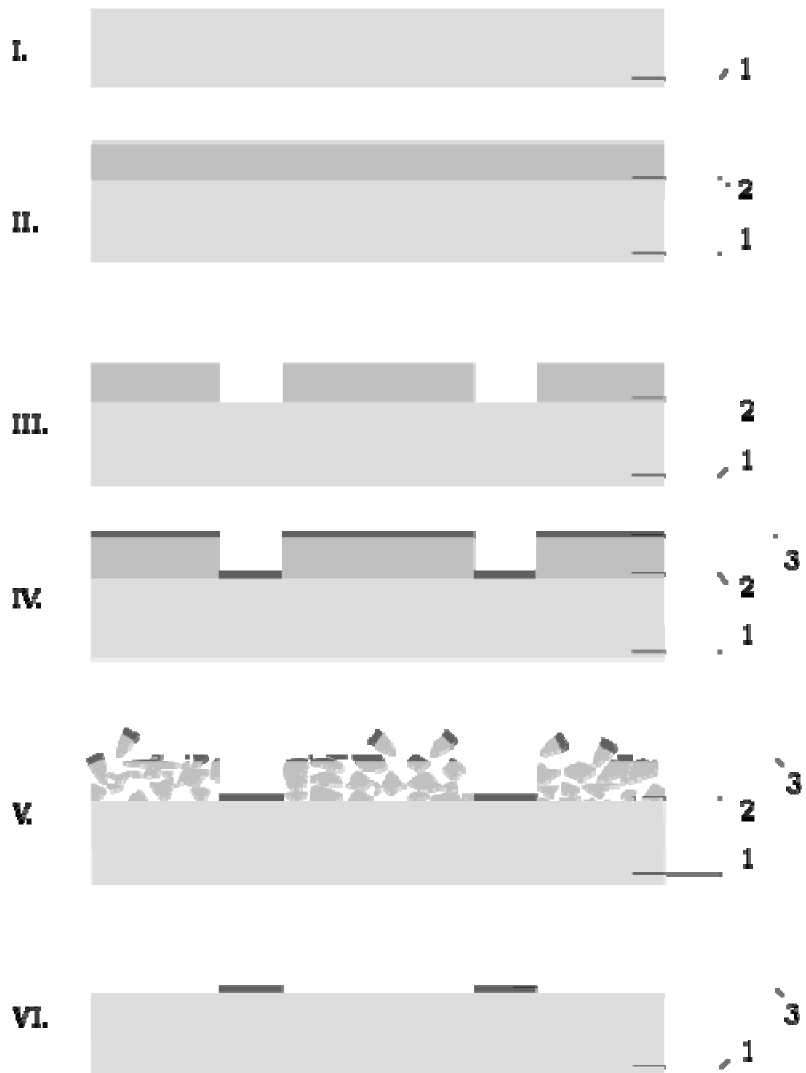
Electroplating:

- plating solutions are often chemically aggressive
- adhesion is important

Lift-off:

- thickness of the film needs to be less than resist thickness
- resist sidewall profile preferably retrograde
- deposition process $T < 120\,^{\circ}\mathrm{C}$ because of resist thermal limitation

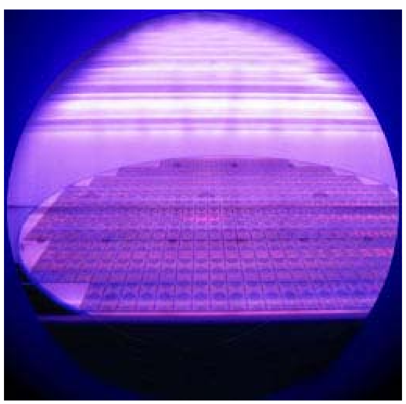
Lift off



http://en.wikipedia.org/wiki/Lift-off_%28microtechnology%29#/media/File:Lift-off_%28microtechnology%29_process.svg http://www.tepla.com/en/applications/photo-resist-processing.html

Table 9.2 Photoresist stripping

Techniques	Mechanism
Oxygen plasma	Oxidation in vacuum
Ozone discharge	Oxidation under atmospheric pressure
Acetone	Dissolution in liquid
Ozonized water	Bond breaking and dissolution
Sulfuric acid	Oxidation in liquid
Organic amines	Oxidation and dissolution in liquid
Hydrogen peroxide	Oxidation in liquid



Mask

http://www.elveflow.com/microfluidic-reviews-and-tutorials/microfluidics-and-microfluidic-device-a-review

Laser pattern generator

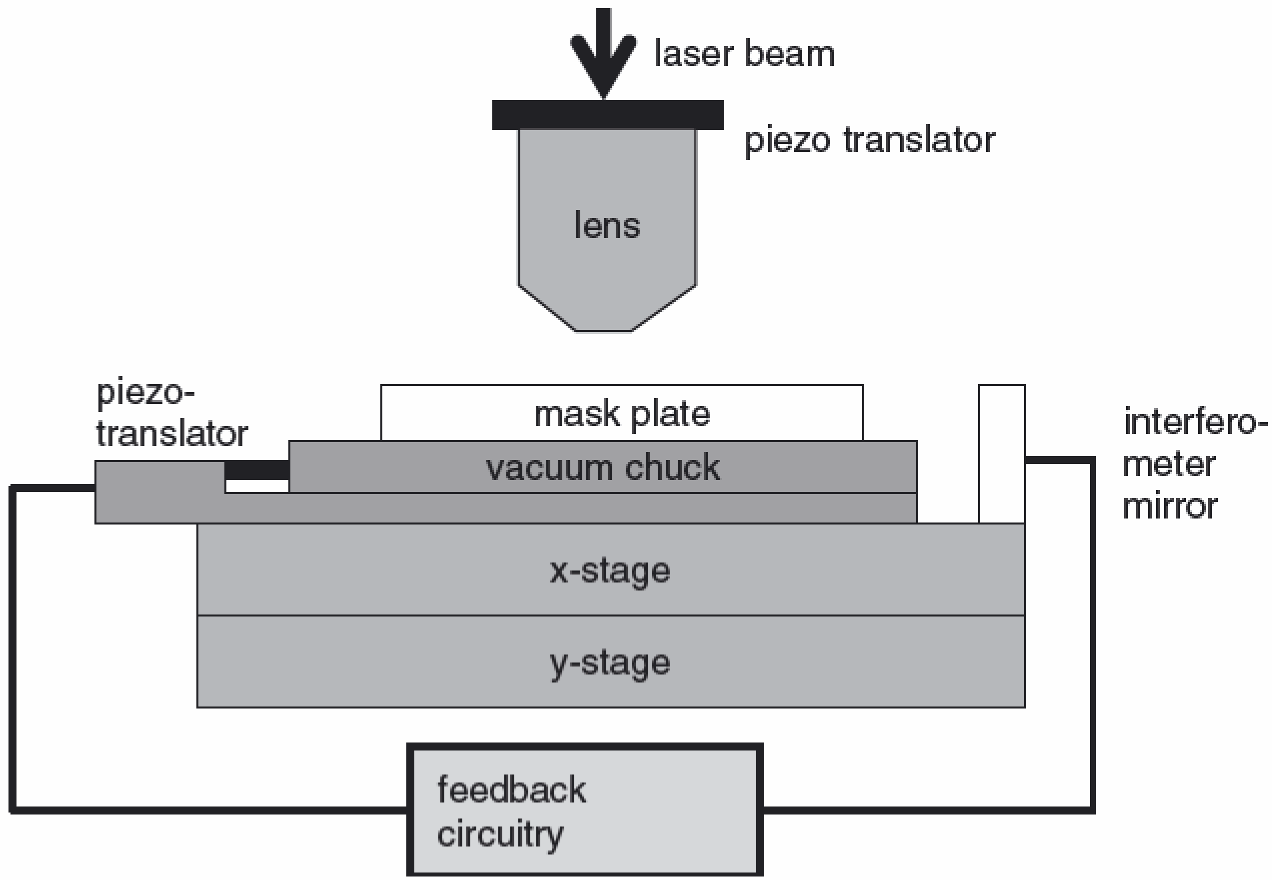


Figure 8.7 Mechanics of the laser mask writer stage

For simple projects you can use a laser printer.

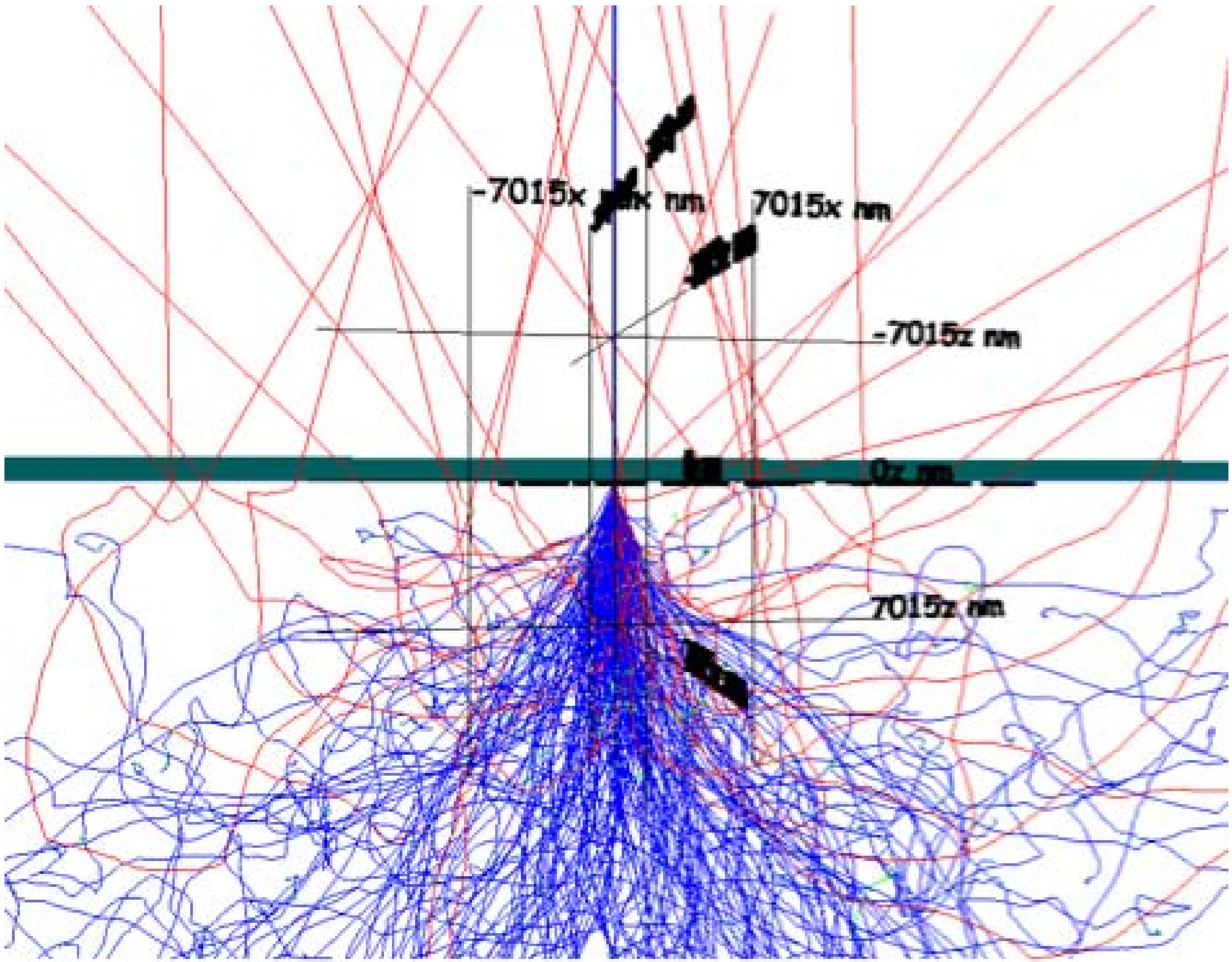
EBPG (Electron beam pattern generator)

100 kV $\rightarrow \lambda = 0.12$ nm

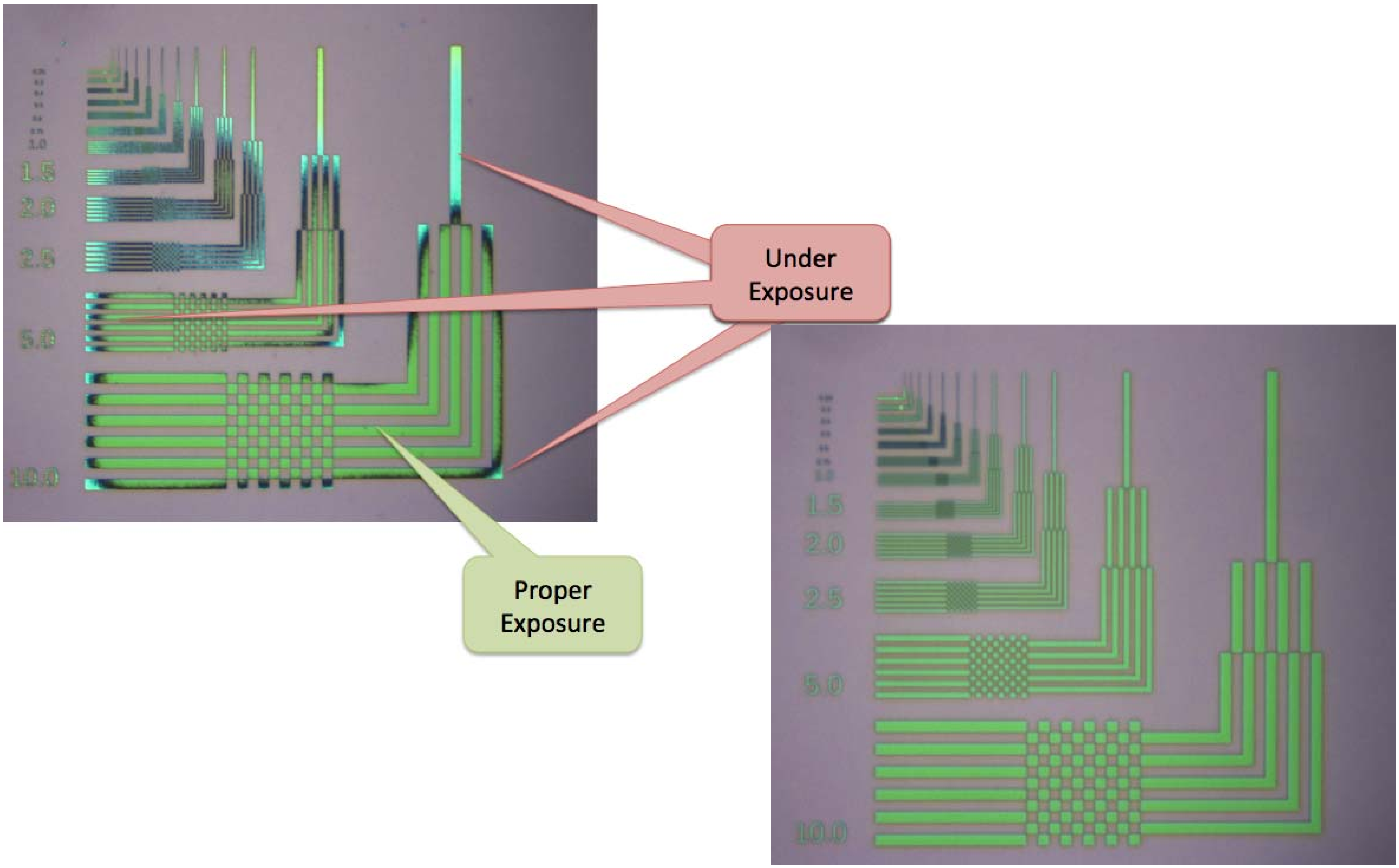
A mask may take hours to write.

KFU Jo Krenn
NTC, JR-Materials Wiez

Proximity effects

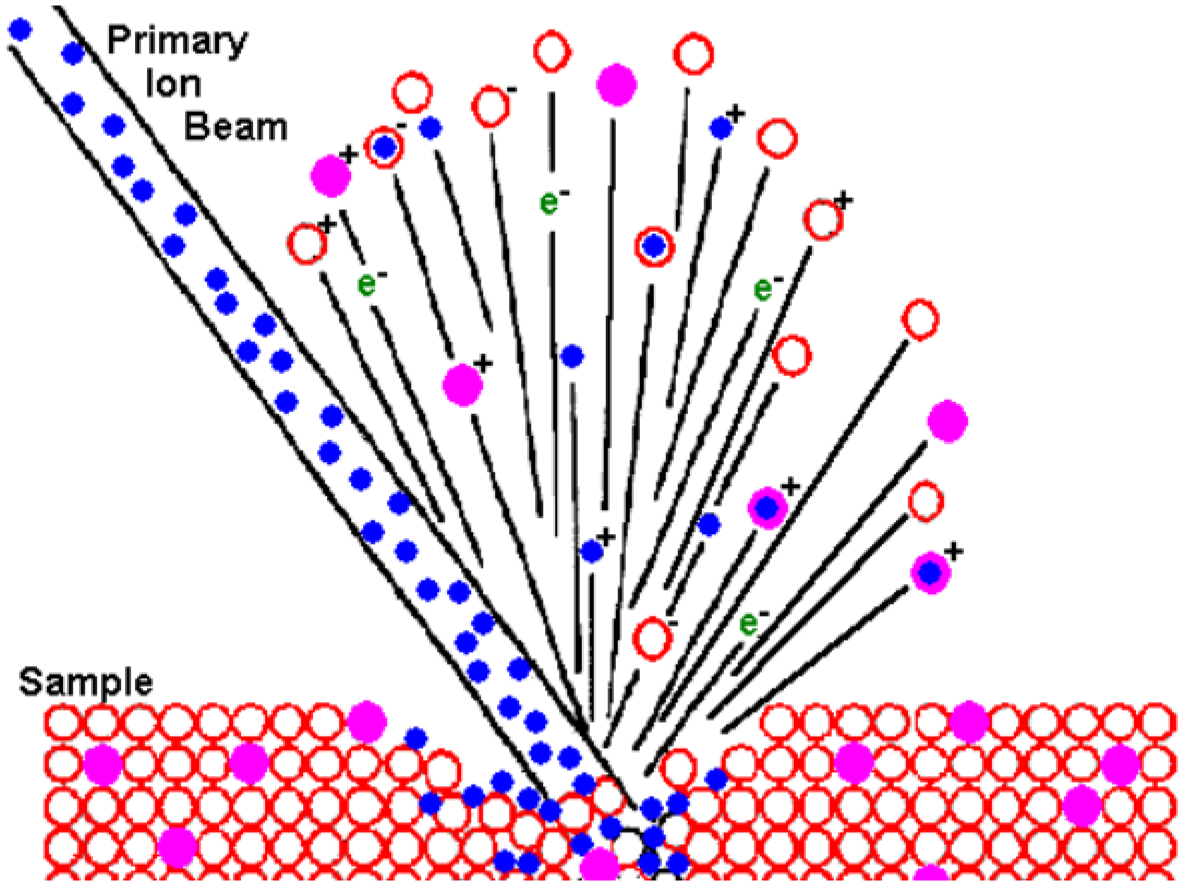


Proximity effects



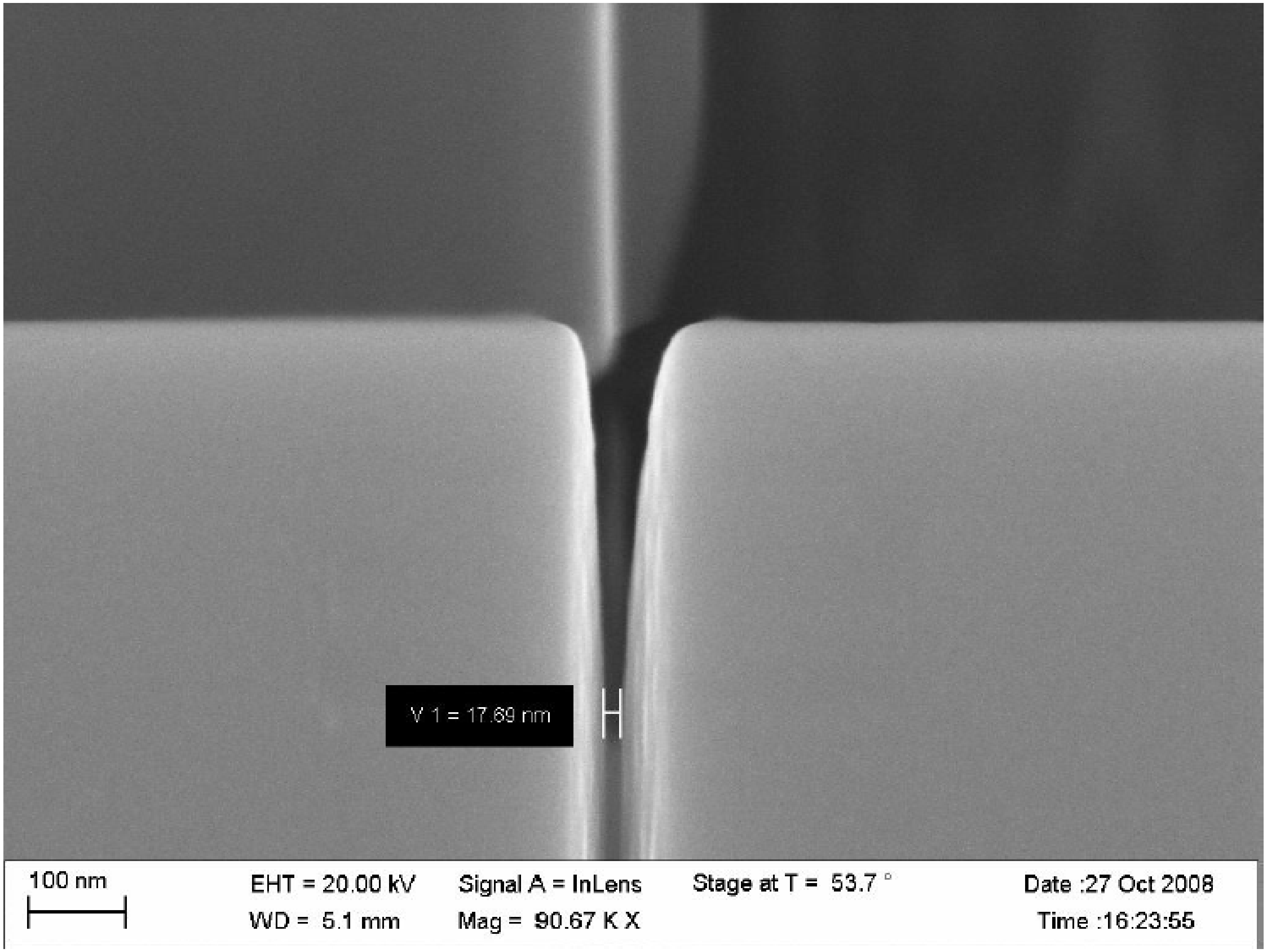
https://ebeam.mff.uw.edu/ebeamweb/doc/patternprep/patternprep/proximity_main.html

Focused ion beam



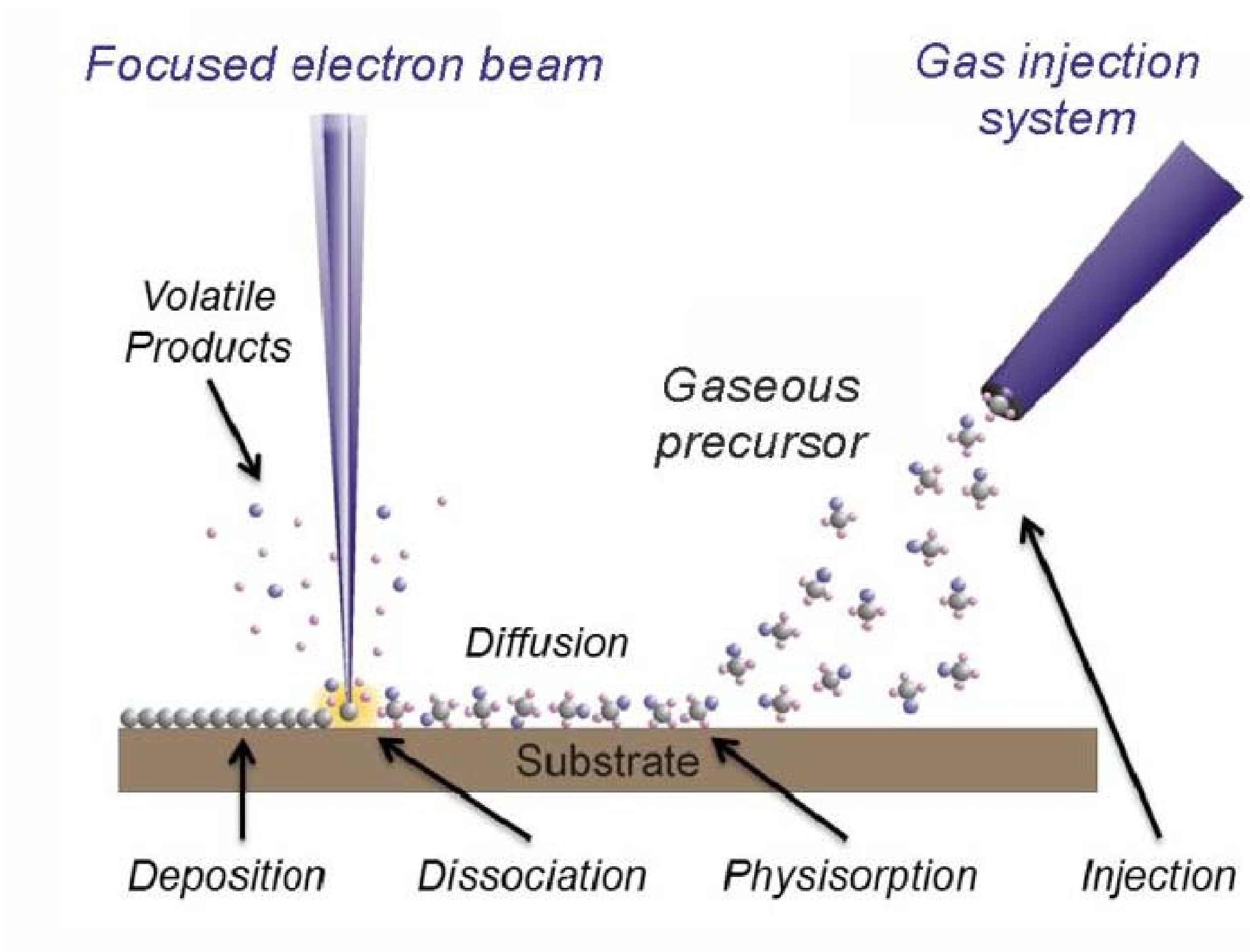
http://www.eag.com/mc/sims-ion-beam-sputtering.html#next

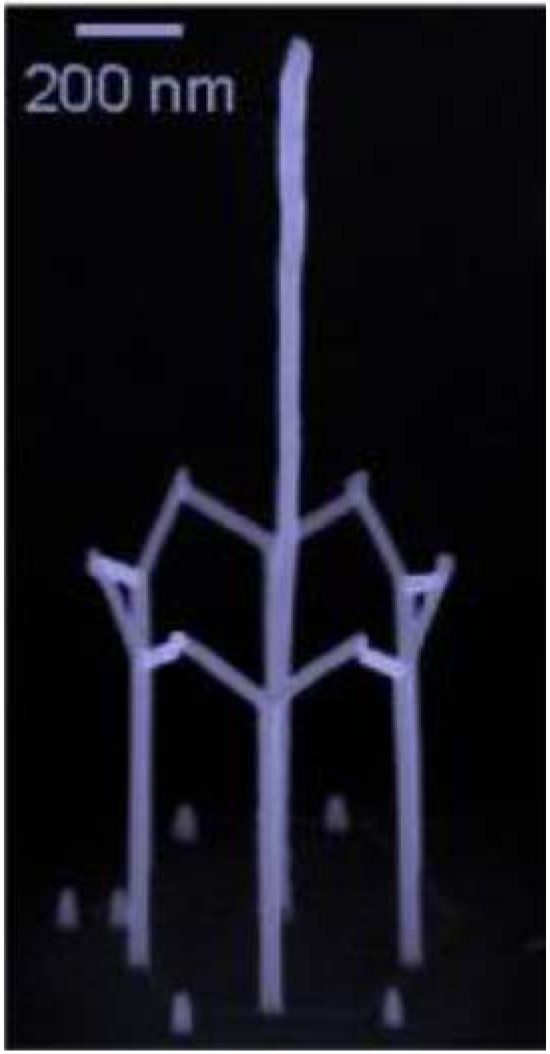
Focused ion beam



http://www.wsi.tum.de/Portals/0/Media/Lectures/20082/cb899e9b-2deb-4cb9-bfd5-344821c84fe9/focused_ion_beam_guenthner.pdf

Focused Electron Beam Induced Deposition





Harald Plank, Focused Electron Beam Induced Deposition: from Fundamentals towards Applications, Habilitationsschrift

Focused ion beam repairs

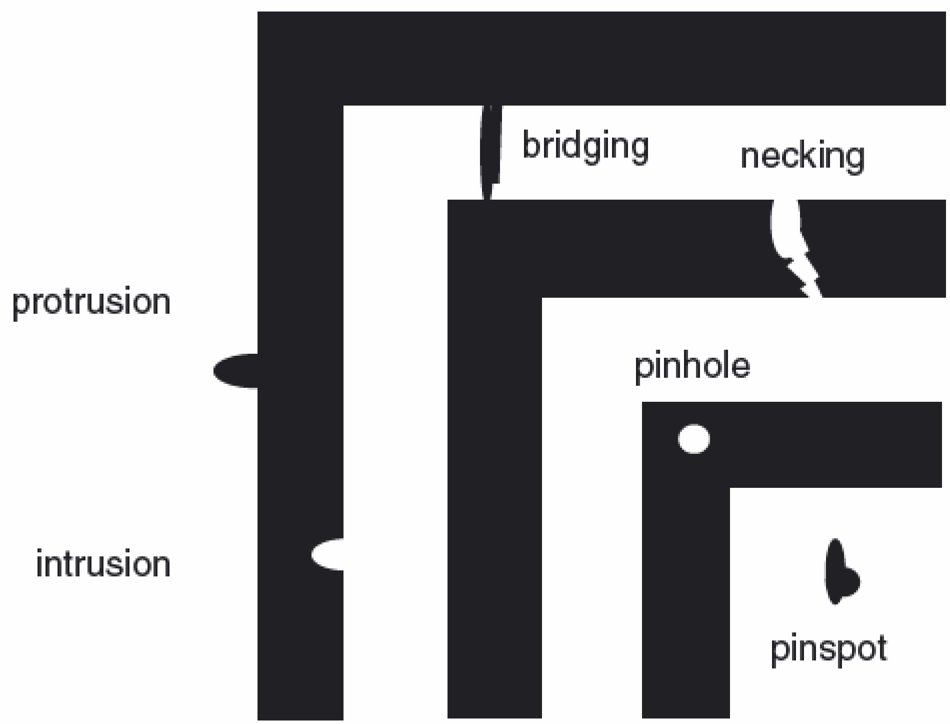
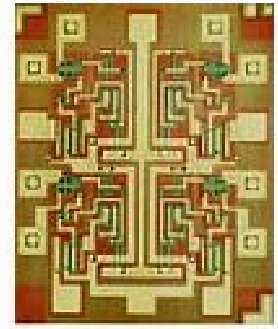


Figure 8.10 Mask defects: extra chrome (protrusion, bridging, pinspot) and missing chrome (necking, intrusion and pinhole). If defect is very small, it may cosmetic only because it does not print in lithography. Redrawn after ref. Skinner

EUV lithography
Self-aligned doubled patterning
Parallel e-beam lithography
Nano-imprint lithography
Directed self-assembly

Semiconductor manufacturing processes



10 µm – 1971
6 µm – 1974
3 µm – 1977
1.5 µm – 1982
1 µm – 1985
800 nm – 1989
600 nm – 1994
350 nm – 1995
250 nm – 1997
180 nm – 1999
130 nm – 2001
90 nm – 2004
65 nm – 2006
45 nm – 2008
32 nm – 2010
22 nm – 2012
14 nm – 2014
10 nm – 2017
7 nm – *~2018*
5 nm – *~2020*

International Technology Roadmap for Semiconductors
2013 Edition

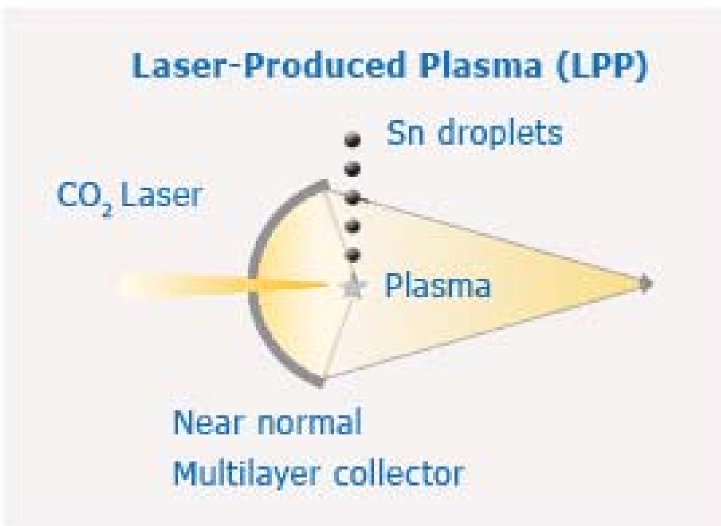
Historically, lithography resolution has been improved by decreasing the exposure wavelength, by increasing the NA of exposure tools and by using improved materials and processes. The NA of 193nm exposure tools cannot be extended since higher index immersion fluids are not available. Smaller optical wavelengths such as 157nm cannot be used due to lack of a suitable immersion fluid and/or the lack of a lens material. So the industry has been working on extending resolution by using EUV, which has a wavelength of 13.5 nm. EUV exposure tools with 0.33NA started shipping in 2013 for use in chip research and development and pilot production and these tools should be operational in the first half of 2014. These tools have resolution capability of well under 30nm for contact hole half pitch and well under 20nm for line and space half pitch. But these tools will need source upgrades with brighter light sources if they are to have sufficient throughput for production use. Such EUV light sources have not yet been demonstrated. So EUV is considered a possible option for meeting the future needs of the lithographic roadmap.

193 nm = ArF excimer laser, 13.5 nm is emitted by a dense plasma

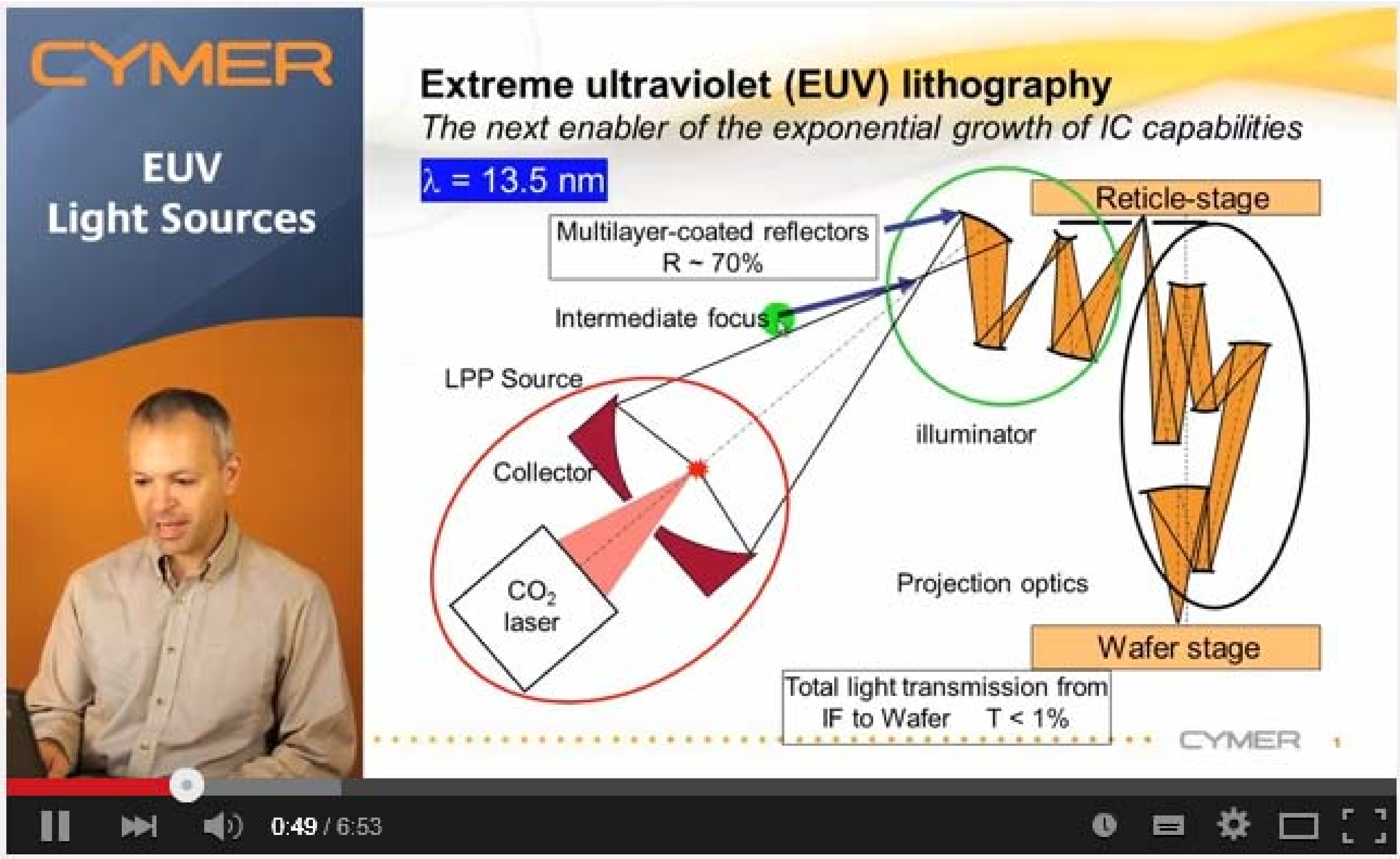
EUV Lithography

A CO_2 laser fires on droplets of molten tin to produce a plasma that emits 13.5 nm photons.

Lens absorb at this wavelength so the light is focused by mirrors.



https://www.cymer.com/euv-lithography/why-lpp



https://www.youtube.com/watch?v=8xJEs3a-1QU

Lenses are not possible.
Perfect mirrors required.
Air absorbs UV.

Pattern multiplication could continue to be extended to greater multiplication factors. In principle, this can be done by using existing process technology and adapting it to smaller features and tighter tolerances. However, lithographic exposures are some of the most expensive processes in a fab and doubling or tripling or more the number of exposures per layer for key layers can quickly become unaffordable. In addition, many exposures and/or many pattern multiplication process steps create many complicated tolerance stack ups and may require process control that is undoable.

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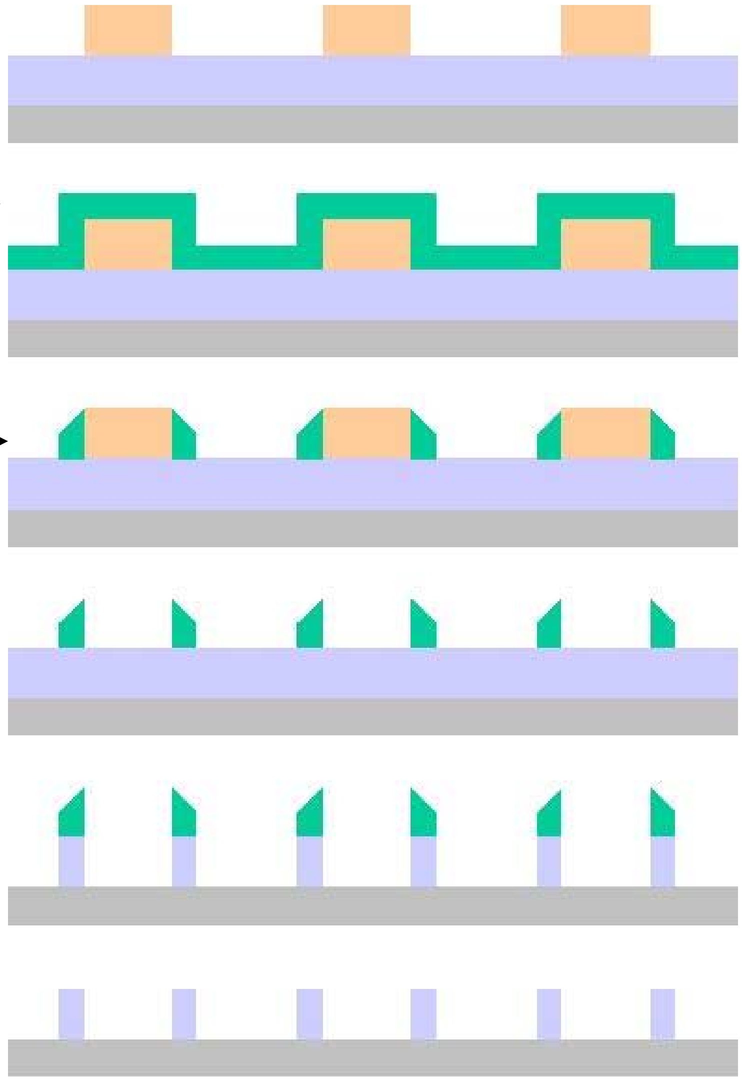
Details of these processes and the challenges of extending them to smaller features are described in the chapter section “Multiple Patterning/Spacer Technology”.

Self-Aligned Doubled Patterning (SADP)

Conformal deposition.

Anisotropic etch leaves only the sidewalls.

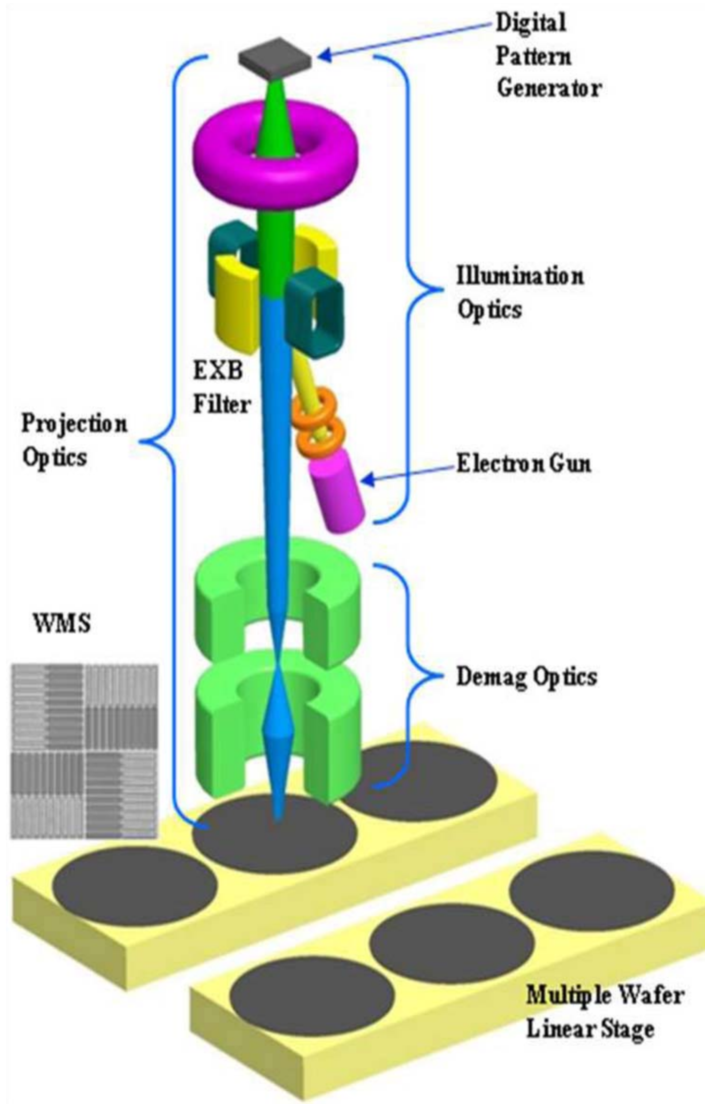


http://en.wikipedia.org/wiki/Multiple_patterning

E-beam lithography or maskless lithography (ML) uses e-beams to do direct write of features in e-beam sensitive resist. Writing high resolution features with a directed e-beam is intrinsically slow, so in order to get sufficient throughput, massively parallel writing with thousands of independently directed e-beams is necessary. Two different companies are developing tools to do this with a projected delivery date of pilot tools to semiconductor companies of sometime in 2016.

https://www.youtube.com/watch?feature=player_embedded&v=OQBcDbhw-0Y

Reflective e-beam lithography (REBL)



http://spie.org/x91889.xml

Nanoimprint is a potential solution that involves coating a thin pattern of liquid on a wafer and using a mask with high resolution relief patterns to physically stamp the wafer and create a relief pattern. The relief pattern can then be used as an etch mask in much the same way that patterned photoresist is. The leading implementation of this technique using step and flash, where a transparent mask is used to stamp one chip at a time and enable photochemical curing of the patterned material before the stamp is lifted from the wafer. Since this is a contact technique, defects are a significant concerns and a system of master and secondary masks is used to accommodate a short lifetime for the masks used for the actual chip patterning and improve the defectivity of the process.

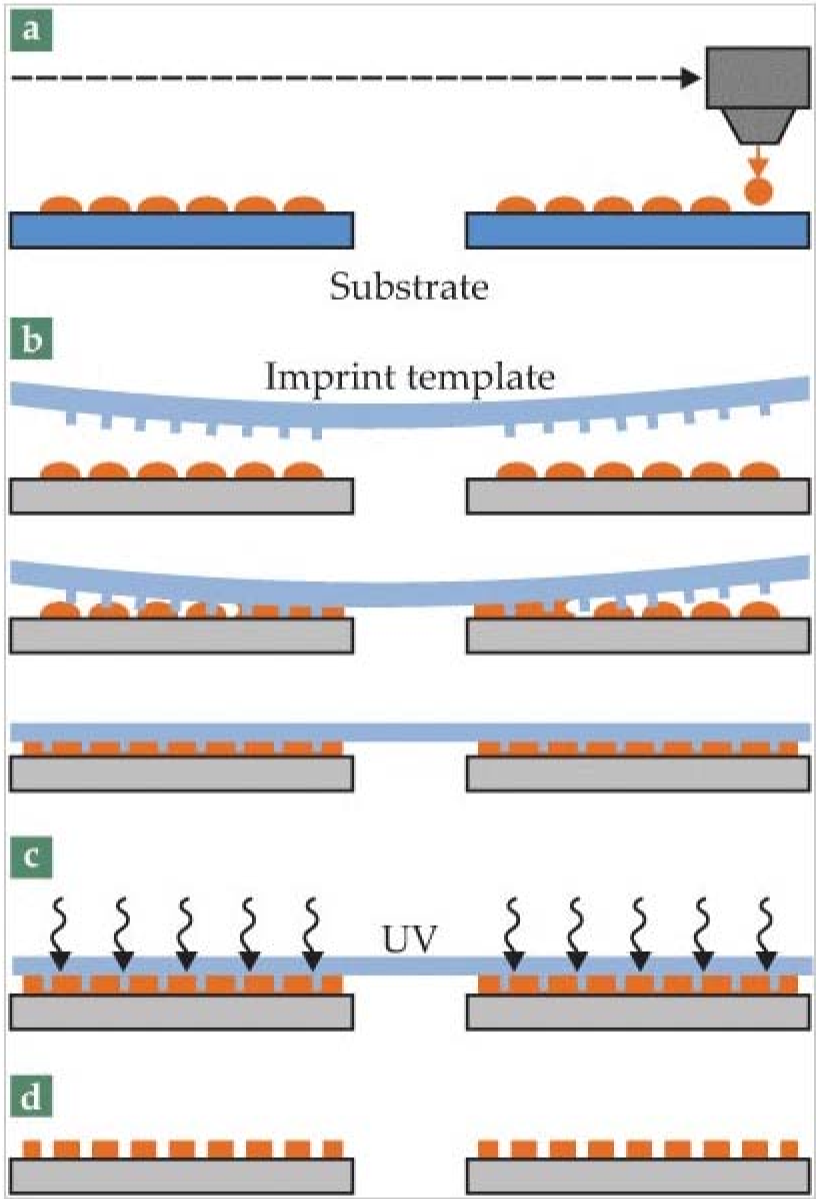


Figure 3. Nanoimprint lithography, the nanoscale version of a rubber stamp. After the liquid resist (orange) is dispensed onto the substrate **(a)**, the imprint template **(b)** mechanically molds it into the desired patterns. The resist is cured with UV light **(c)** to produce the nanoscale pattern **(d)**. (Adapted from ref. 18 .)

Citation: Phys. Today **67**, 12, 45 (2014); http://dx.doi.org/10.1063/PT.3.2621

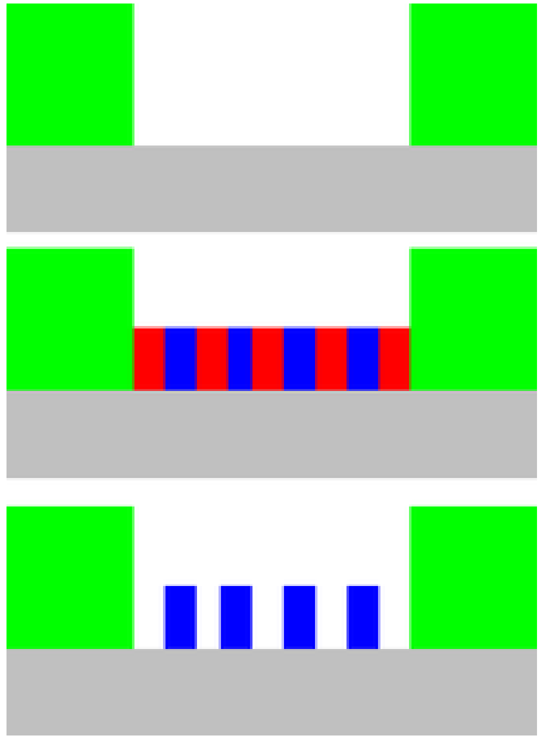
JOANNEUM RESEARCH - MATERIALS
Roll-to-Roll Nanoimprint

video: http://www.joanneum.at/materials/forschungsbereiche/rolle-zu-rolle-nanoimprinten.html

A patterning technique that has shown a lot of progress in the last two years is directed self-assembly (DSA). This technique takes advantage of the fact that required feature sizes are reaching a size similar to that of polymer molecules that can be readily made in the lab. The most common implementation uses special polymers called block copolymers, which consist of two connected polymers each made from a different monomer. If the monomers are selected properly, the blocks will separate into phase domains when annealed. The phase domains will have a size determined by the size of the individual polymer blocks and the shapes of the domains will be determined by the ratio of the sizes of each polymer block. By creating guiding features on a wafer, this domain formation process can be constrained to give line or hole patterns with the lines and holes in desired locations. Patterns printed with 193nm immersion lithography can be used as guide patterns and pitch multiplication factors of three or four times are readily accessible. This technique was considered a research topic two years ago, but now most major semiconductor producers have substantial programs exploring the possibility of implementing this technique in actual chip production.

Directed self-assembly (DSA)

Copolymers such as PMMA/PS form stripe or dot patterns. The positions of the stripes or dots can be guided by topography.



http://en.wikipedia.org/wiki/Multiple_patterning

Lithography overview

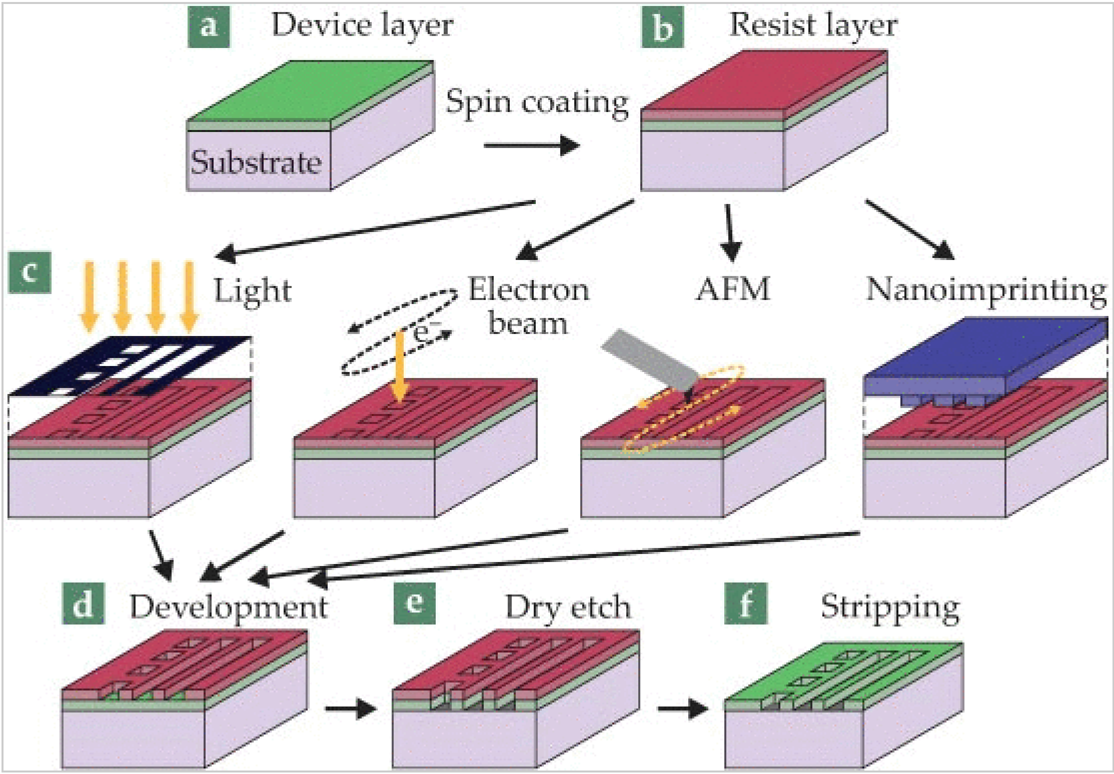


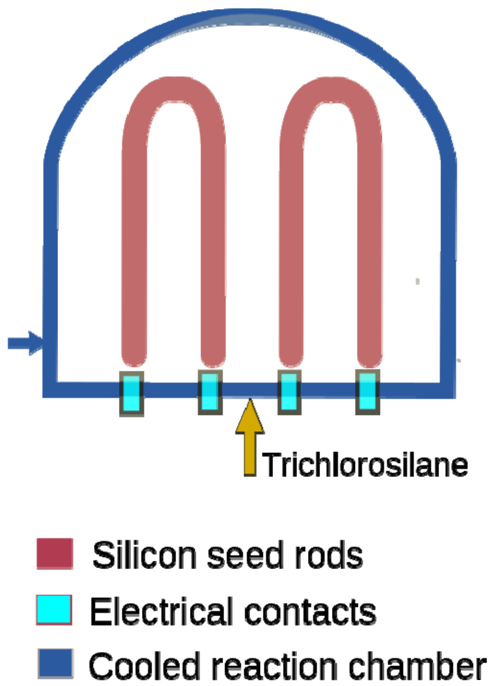
Figure 2. Resist-based lithography. The device layer **(a)** is spin coated with a thin layer of polymer resist **(b)**. The resist can be patterned using any of a wide range of technologies **(c)**, including photons and a mask, an electron beam, an atomic force microscope (AFM), and a nanoimprint template. The development step **(d)** removes the exposed area. An anisotropic dry etch **(e)** removes the unwanted material from the device layer. A final step strips the resist **(f)** to leave behind the micro- and nanodevices. Multiple iterations of depositions and lithography sequences result in complex multilayered structures.

Citation: Phys. Today **67**, 12, 45 (2014); http://dx.doi.org/10.1063/PT.3.2621

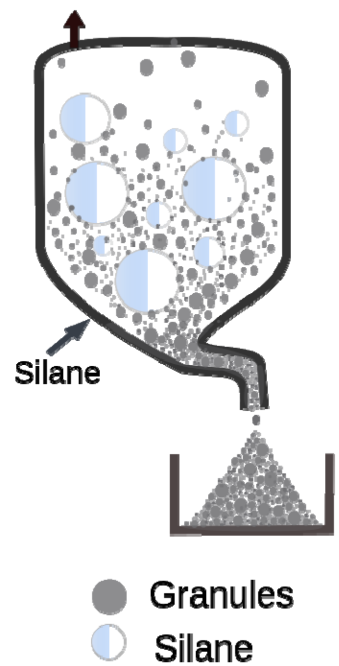
Silicon purification

Conversion of silicon into liquids ($HSiCl_3$ or $SiCl_4$) or gases (SiH_4). Distillation then the deposition of polysilicon.

Siemens process



FBR process

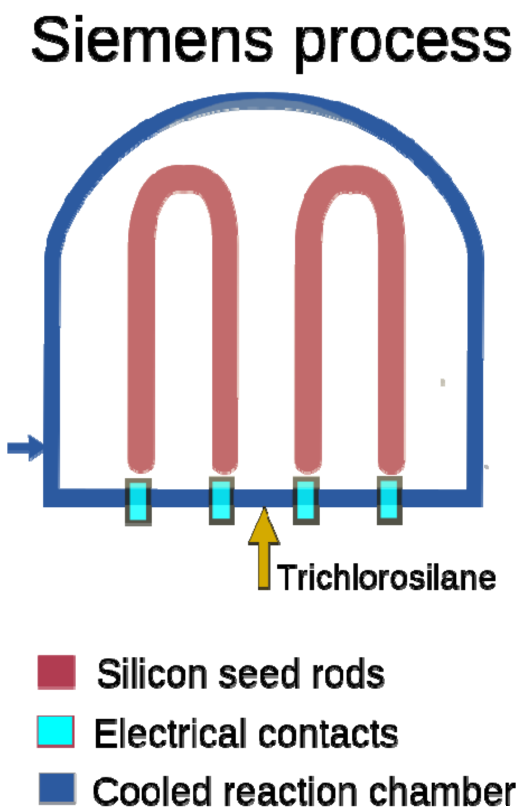


http://www.polyplantproject.com/images/cvdreactors2.png

http://en.wikipedia.org/wiki/Silicon#Production

Silicon purification

Conversion of silicon into liquids ($HSiCl_3$ or $SiCl_4$) or gases (SiH_4). Distillation then the deposition of polysilicon.

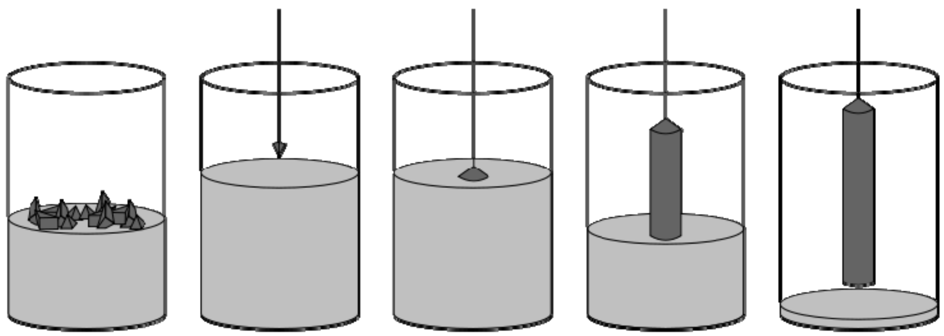


http://en.wikipedia.org/wiki/Polycrystalline_silicon

http://en.wikipedia.org/wiki/Silicon#Production

Crystal growth

Czochralski Process



add dopants to the melt

Cz wafers always contain O, N, C.

images from wikipedia

Float zone Process

A polycrystalline silicon rod made by the Siemens process

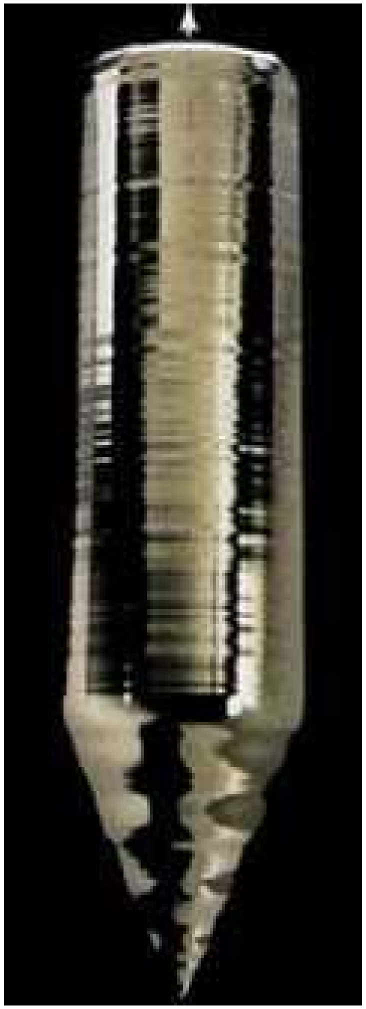
image from wikipedia

Neutron transmutation

$$^{30}\mathrm{Si} + \mathrm{n} \rightarrow \ ^{31}\mathrm{Si} + \gamma$$
$$^{31}\mathrm{Si} \rightarrow \ ^{31}\mathrm{P} + \beta$$

Fz wafers contain less O, N, C than Cz wafers. Diameter limited.

Silicon wafers



- Cut with a diamond saw
- Lapping to remove saw damage
- Etching /cleaning to remove lapping damage
- Edge rounding for handling
- Polishing (fine slurry)
- Cleaning: Ammonium Hydroxide - dilute Hydrofluoric acid - DI water Rinse - Hydrochloric acid and Hydrogen peroxide - DI water rinse.

http://www.processpecialties.com/siliconp.htm

https://www.youtube.com/watch?v=AMgQ1-HdElM