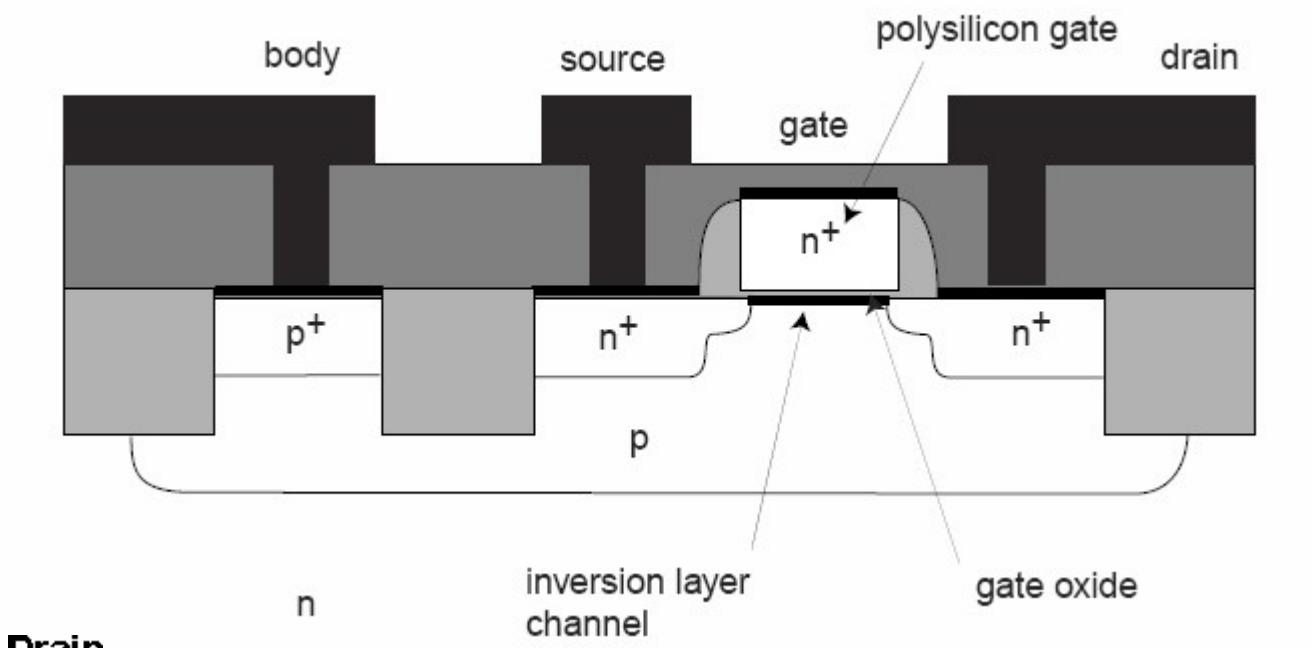
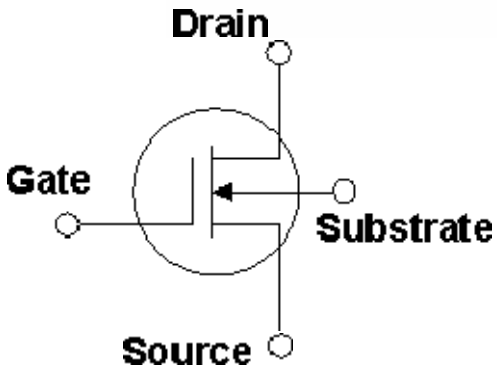
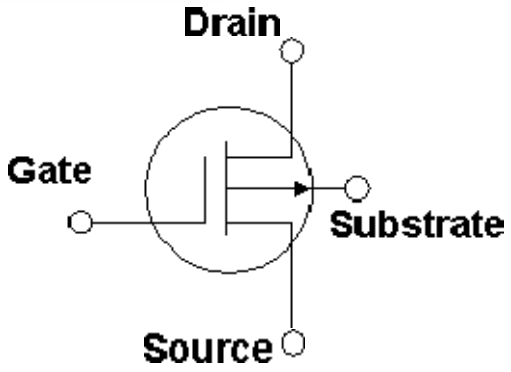
MOSFETs





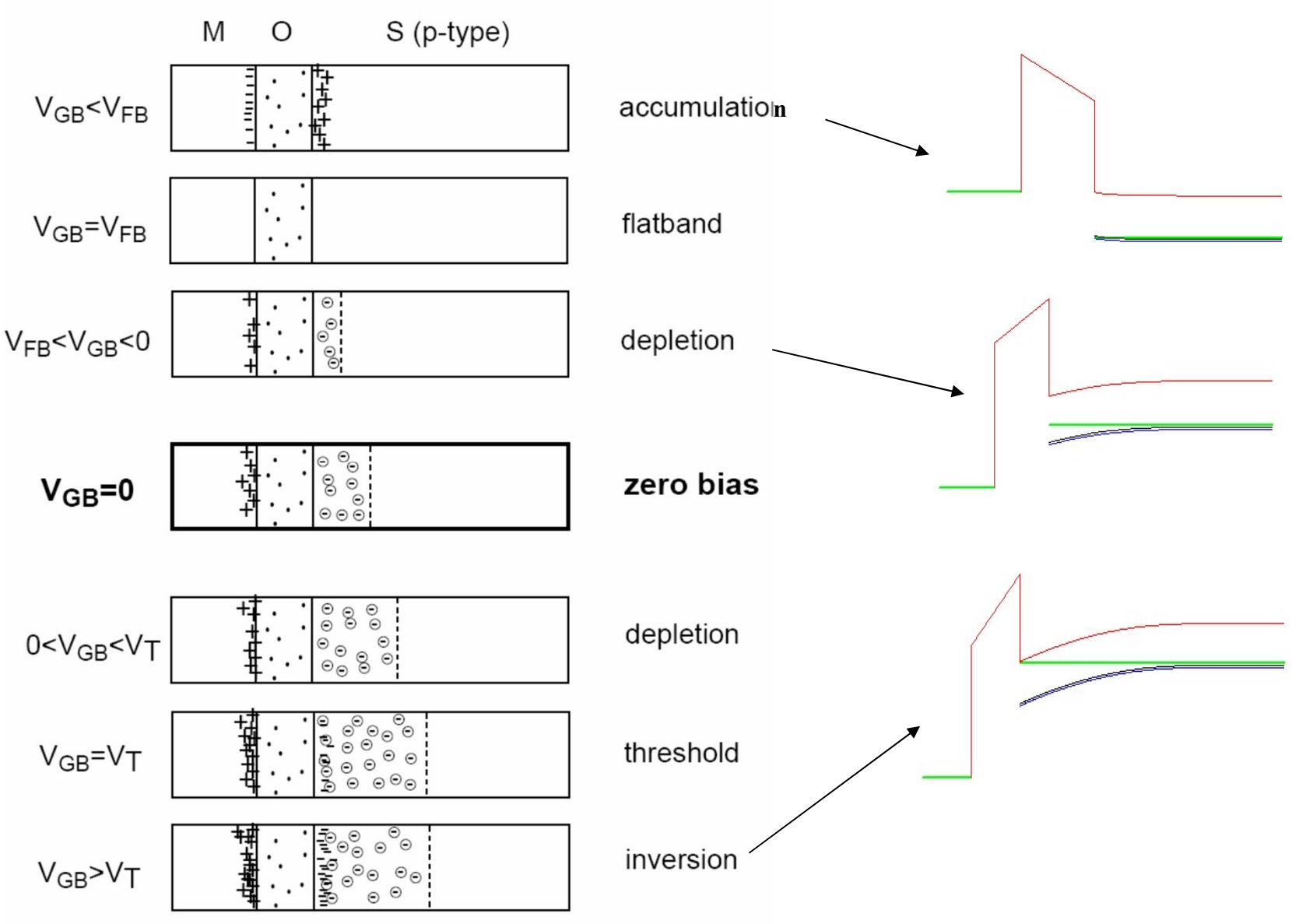
n - channel

functions as a switch
~ 1 billion /chip

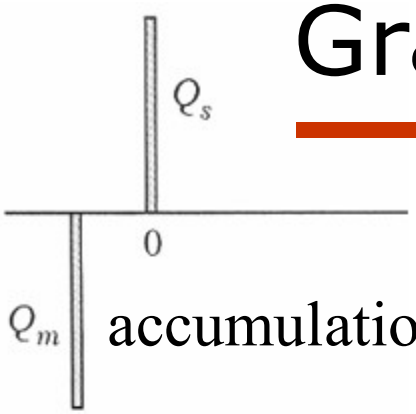


p - channel

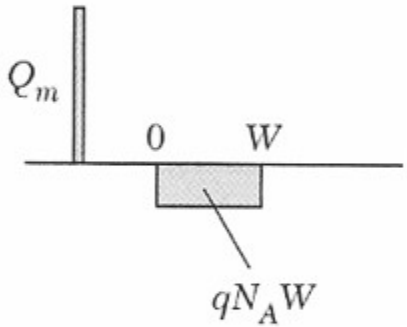
MOS capacitor



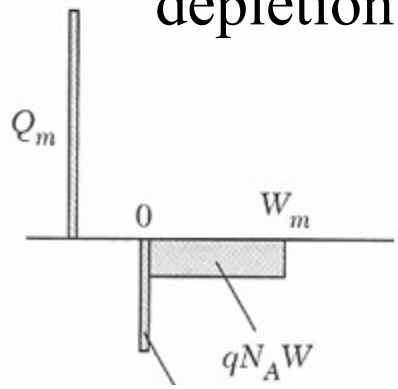
Gradual channel approximation



accumulation



depletion



inversion

$$Q_{\text{mobile}} = \begin{cases} 0, & \text{for } V_G - V_B < V_T \\ -C_{\text{ox}}(V_G - V_B - V_T) & \text{for } V_G - V_B > V_T \end{cases}$$

$$n_s(y) = -\frac{Q(y)}{e} = \frac{C_{ox}(V_G - V_{ch}(y) - V_T)}{e}$$

http://lampx.tugraz.at/~hadley/psd/L10/gradualchannelapprox.php

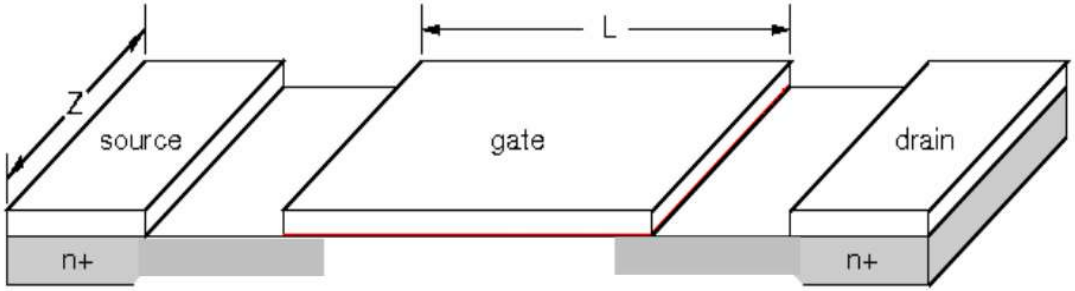
Gradual channel approximation

Field lines are vertical, current flow is horizontal.

Ohm's law $\longrightarrow$ $j = -nev_d = ne\mu_n E_y$

$$I = Ztj = Ze\mu_n n_s E_y$$

$$n = \frac{n_s}{t}$$



$n_s = nt$ is the sheet charge at the interface.

$$n_s(y) = \frac{Q}{e} = \frac{-C_{ox}\left(V_G - V(y) - V_T\right)}{e}$$

Gradual channel approximation

$$I_D = Ztj = Ztne\mu_n E_y$$

$$E_y = -\frac{dV_{ch}}{dy}$$

$$I_D = -Z\mu_n C_{ox}(V_G - V_{ch}(y) - V_T)\frac{dV_{ch}}{dy}$$

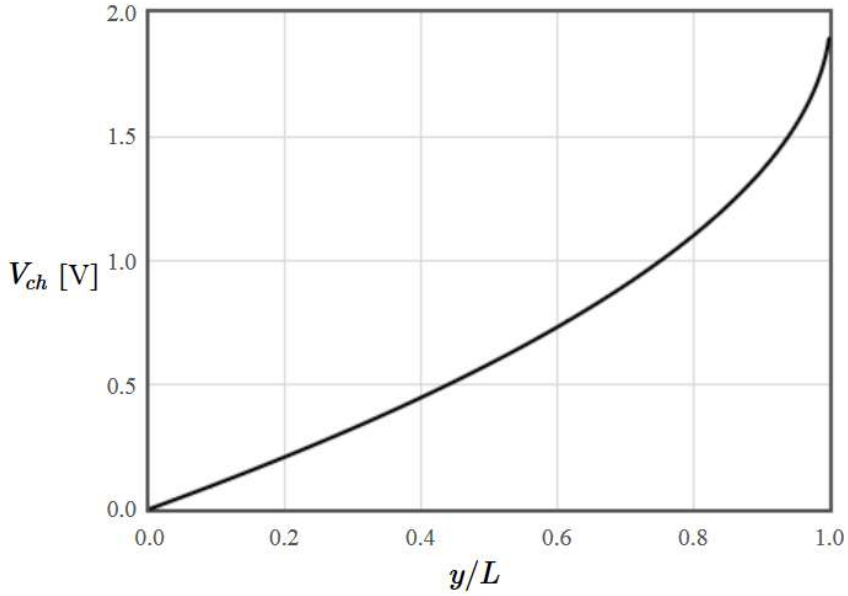
This is a first order differential equation for V_{ch} : Integrate

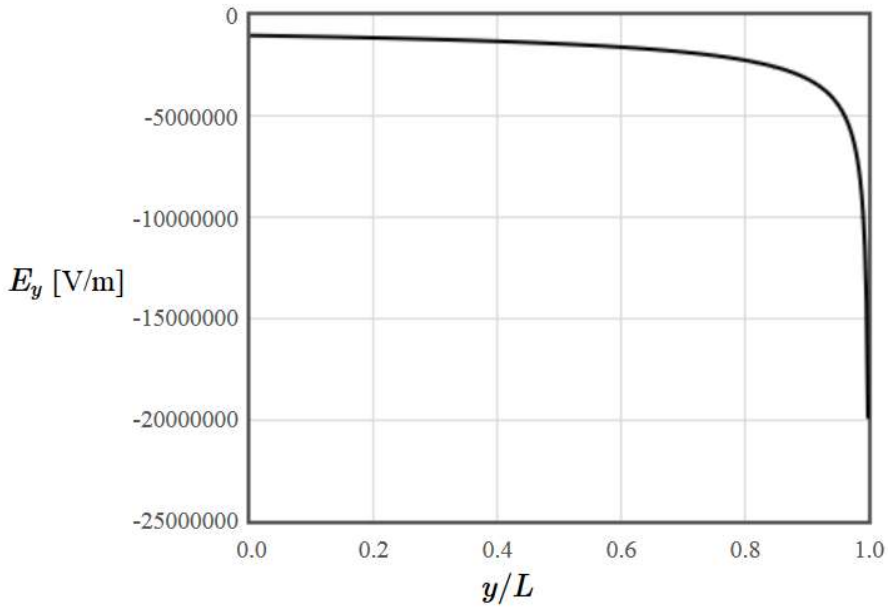
http://lampx.tugraz.at/~hadley/psd/L10/gradualchannelapprox.php

Gradual channel approximation

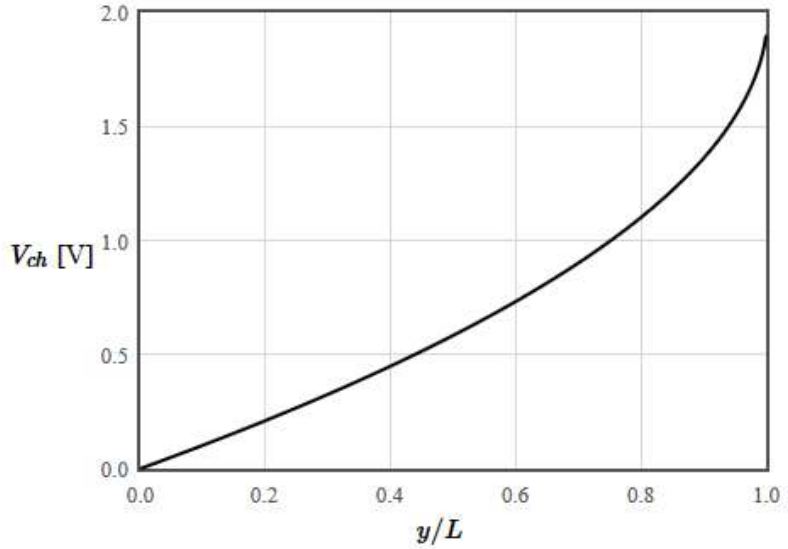
$$V_{ch}(y) = V_G - V_T - \sqrt{(V_G - V_T)^2 - \frac{2I_D y}{Z\mu_n C_{ox}}}$$

$$E_y = -\frac{dV_{ch}}{dy} = -\frac{I_D}{Z\mu_n C_{ox}\sqrt{(V_G - V_T)^2 - \frac{2I_D y}{Z\mu_n C_{ox}}}}$$



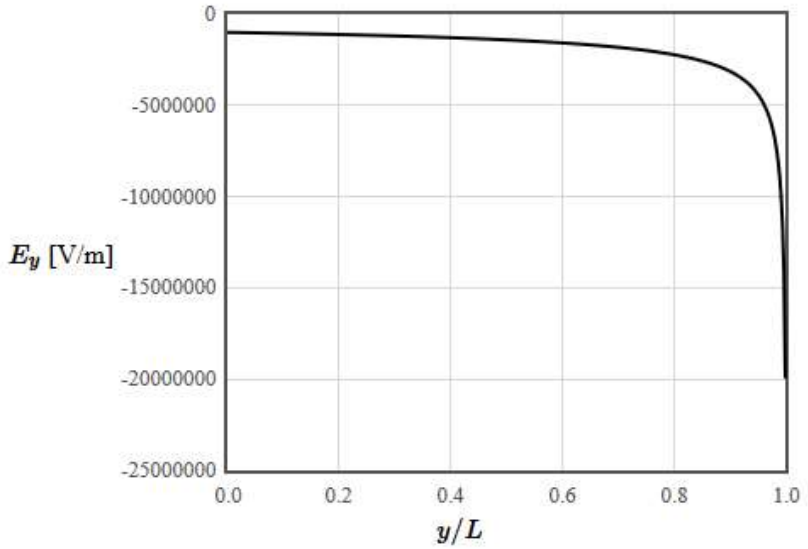


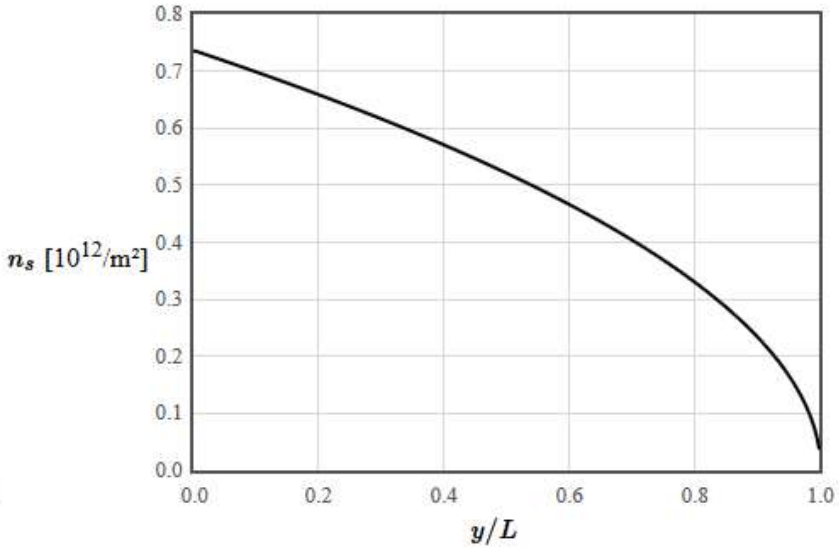
MOSFET Gradual Channel Approximation



$Z =$	1E-5	m
$L =$	1E-6	m
$\mu_n =$	1500	cm²/Vs
$\epsilon_r =$	4	
$t_{ox} =$	3E-9	m
$V_D =$	1.9	V
$V_G =$	3	V
$V_T =$	1	V

Replot





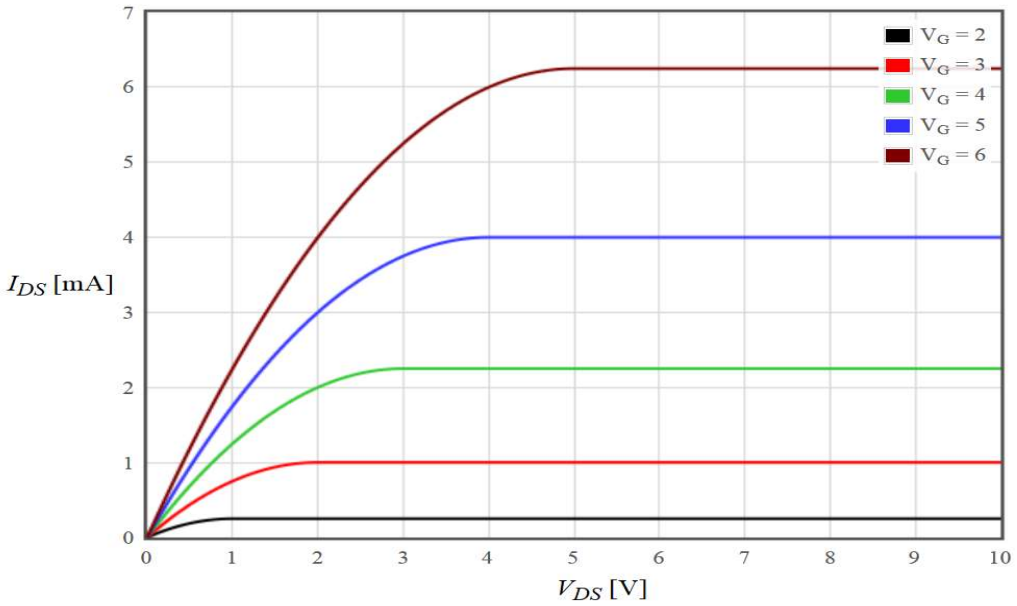
http://lampx.tugraz.at/~hadley/psd/L10/gradualchannelapprox.php

Gradual channel approximation

$$\int_0^L I_D \, \mathrm{d}y = \int_0^{V_D} Z \mu_n C_{ox} (V_G - V_{ch}(y) - V_T) \, \mathrm{d}V$$

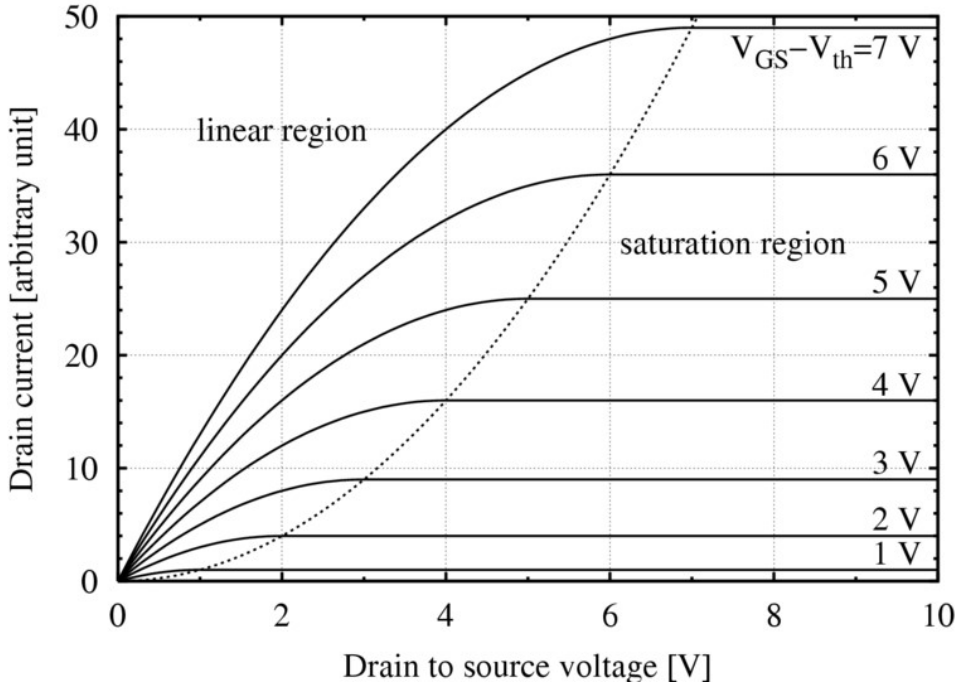
$$\boxed{I_D = \frac{Z}{L} \mu_n C_{ox} \left[(V_G - V_T) V_D - \frac{V_D^2}{2} \right]}$$

Valid in the linear regime (until pinch-off occurs at the drain).



MOSFET-saturation voltage

$$I = \frac{Z}{L}\mu_n C_{ox}\left[\left(V_G - V_T\right)V_D - \frac{V_D^2}{2}\right]$$



At pinch-off, $dI_{ds}/dV_{ds} = 0$

$$\frac{dI}{dV_D} = \frac{Z}{L}\mu_n C_{ox}\left[\left(V_G - V_T\right) - V_D\right] = 0 \qquad V_{sat} = \left(V_G - V_T\right)$$

A MOSFET in saturation is a voltage controlled current source.

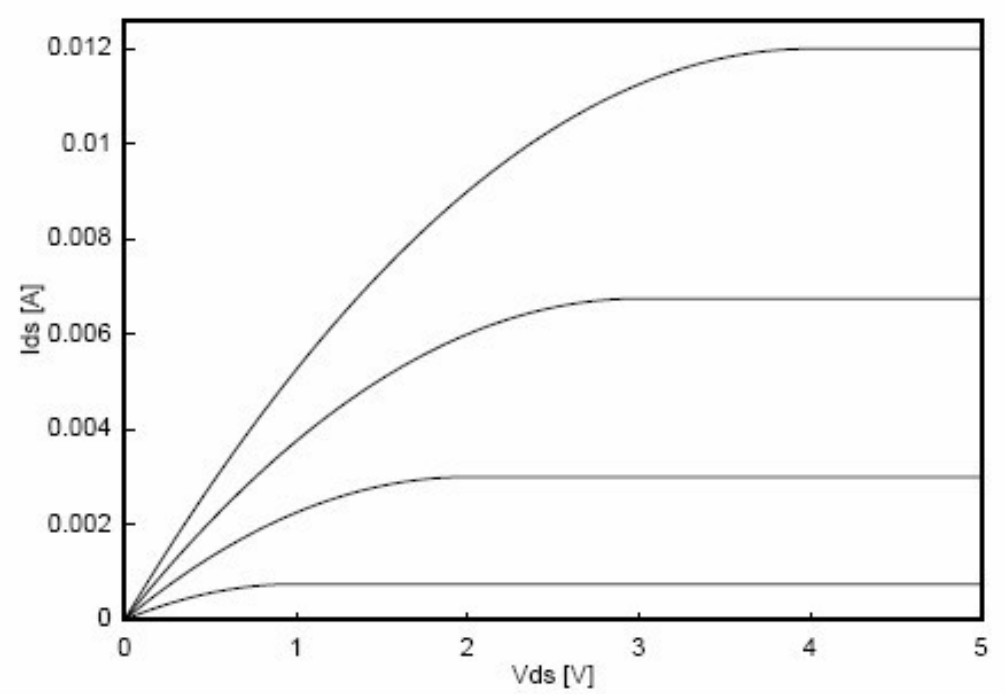
MOSFET - saturation current

Use the saturation voltage at pinch-off to determine the saturation current

$$V_{sat} = \left(V_G - V_T\right)$$

$$I = \frac{Z}{L}\mu_n C_{ox}\left[\left(V_G - V_T\right)V_D - \frac{V_D^2}{2}\right]$$

$$I_{sat} = \frac{Z}{2L}\mu_n C_{ox}\left(V_G - V_T\right)^2$$

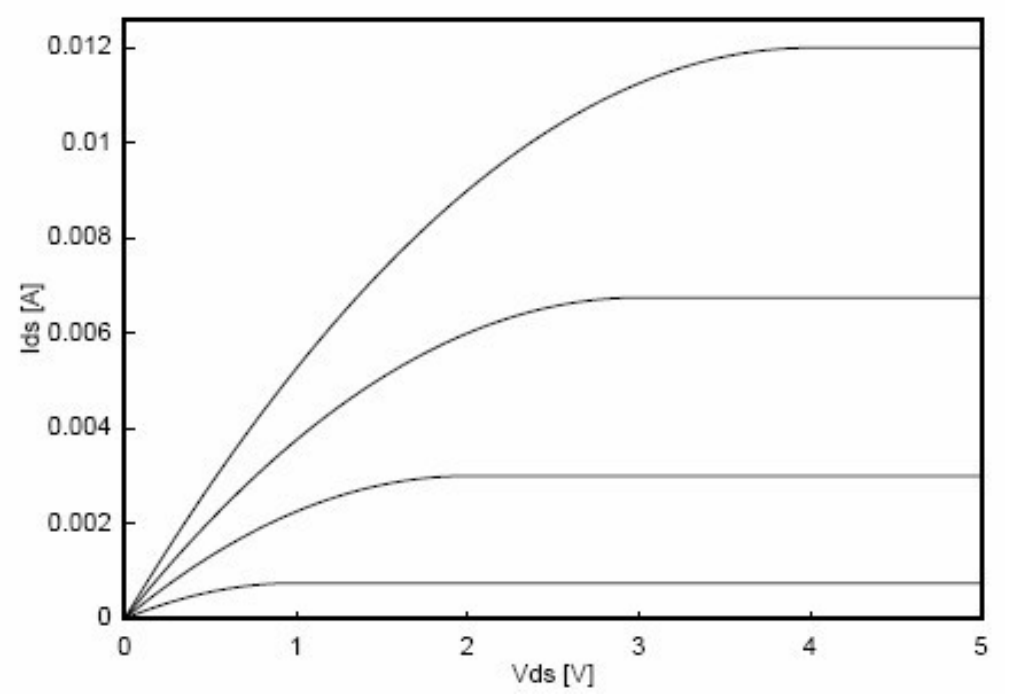


MOSFET (linear regime)

Channel conductance in the linear regime. For small V_D

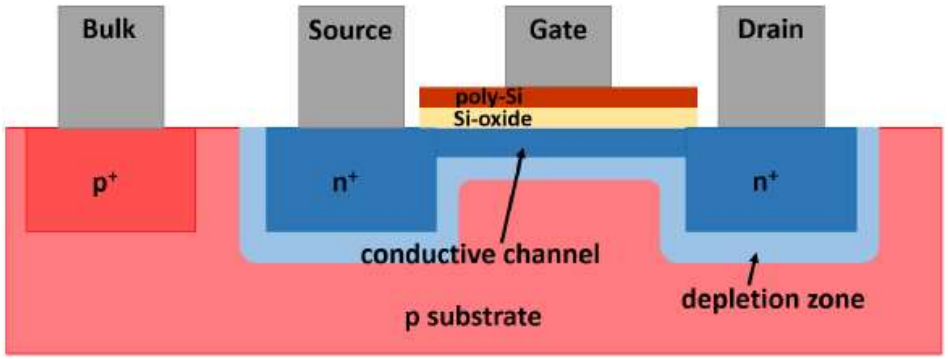
$$I \approx \frac{Z}{L}\mu_n C_{ox}\left[\left(V_G - V_T\right)V_D\right]$$

$$g_D = \frac{dI_D}{dV_D} = \frac{Z}{L}\mu_n C_{ox}\left(V_G - V_T\right)$$

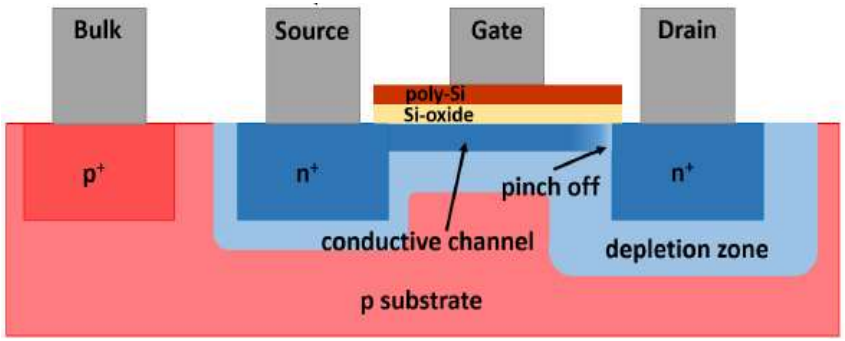


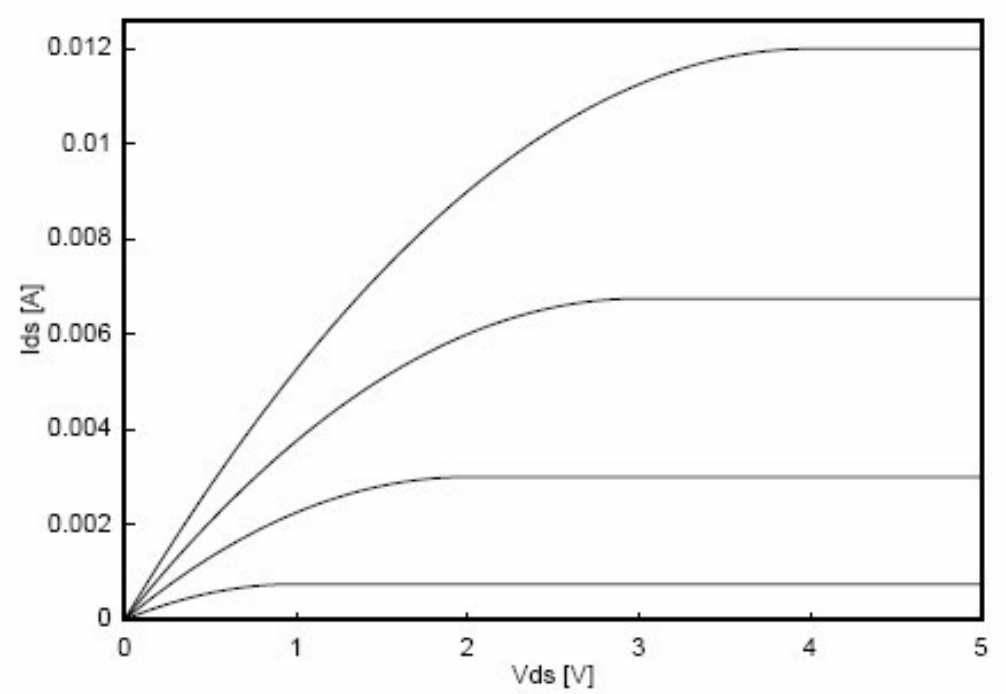
Transconductance

$$g_m = \frac{dI_D}{dV_G} = \frac{Z}{L}\mu_n C_{ox} V_D$$



MOSFET (saturation regime)





$$I_{sat} = \frac{Z}{2L}\mu_n C_{ox}\left(V_G - V_T\right)^2$$

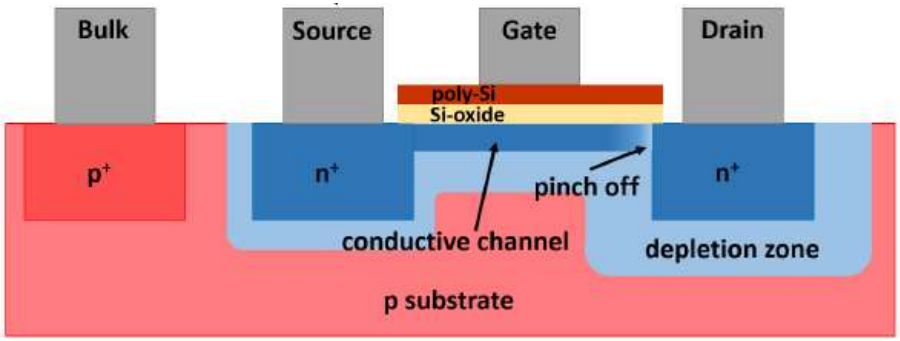
Transconductance

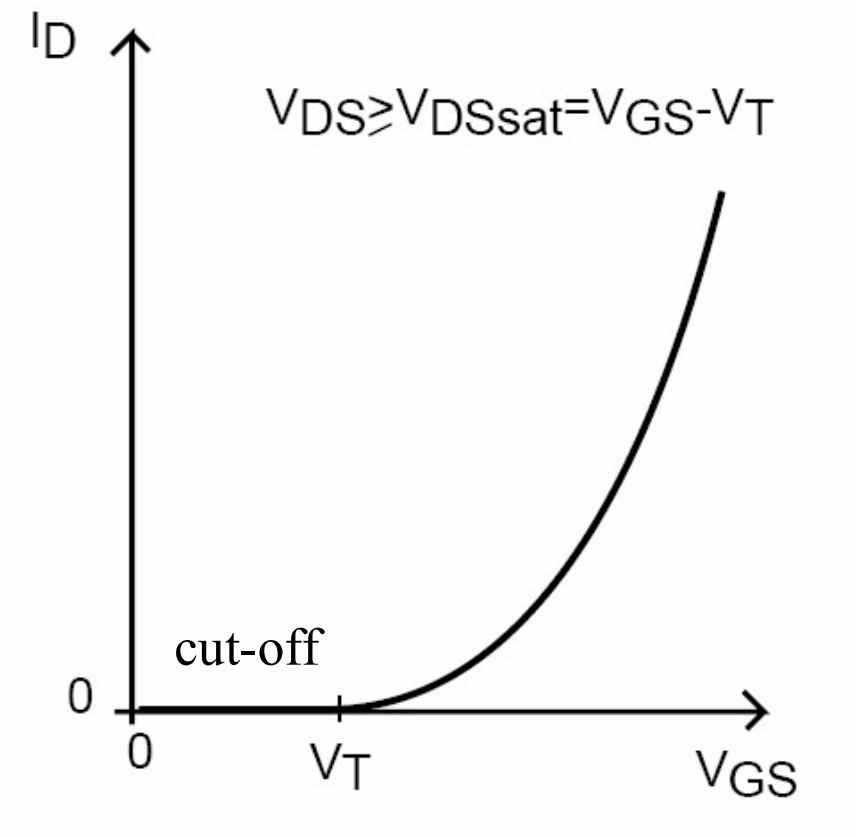
$$g_m = \frac{dI_D}{dV_G} = \frac{Z}{L}\mu_n C_{ox}\left(V_G - V_T\right)$$

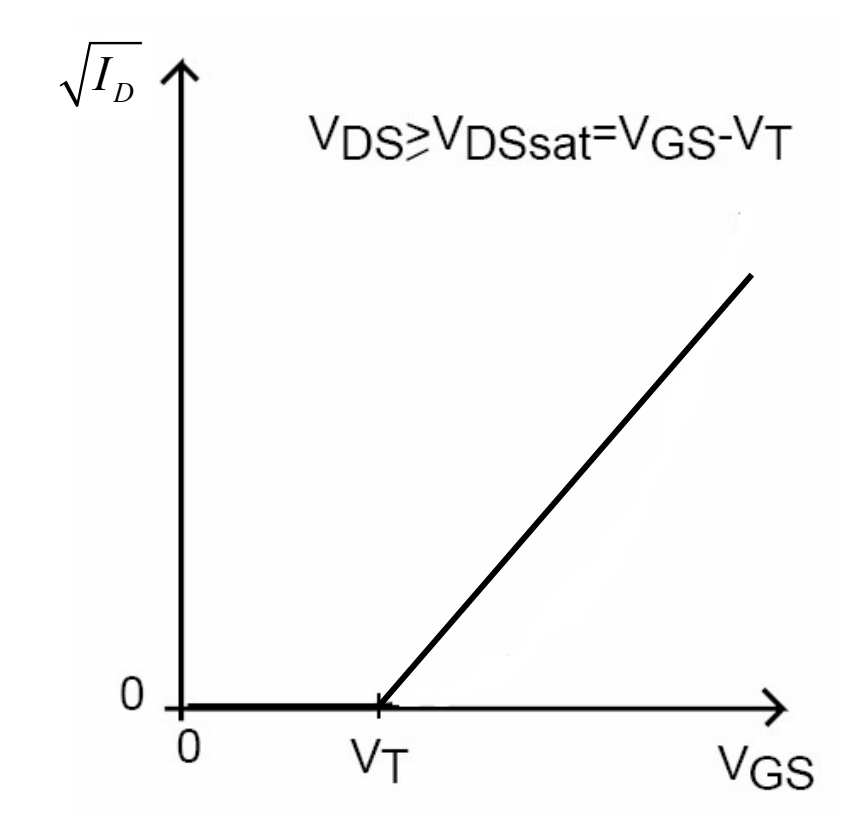
A MOSFET in the saturation regime acts like a voltage controlled current source.

MOSFET (saturation regime)

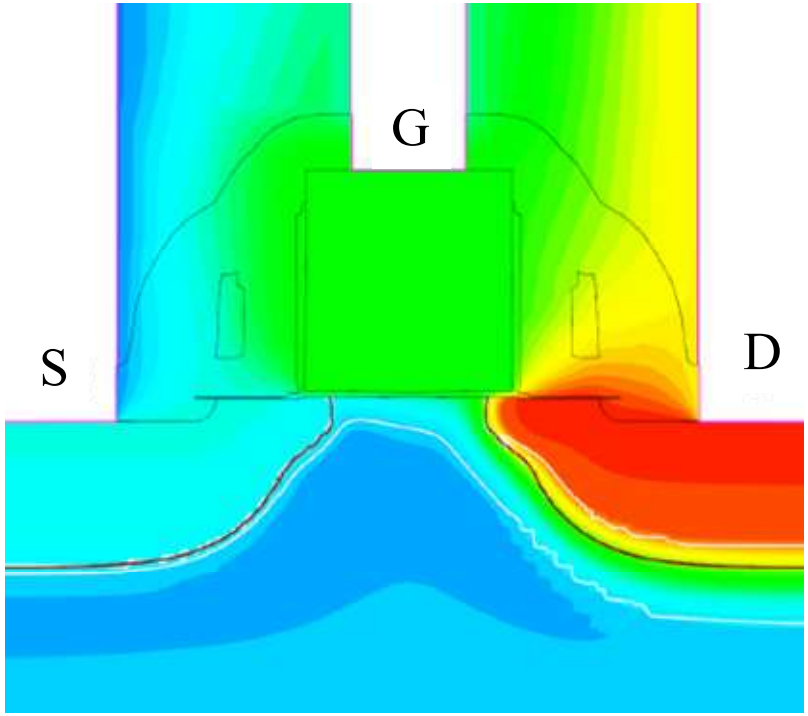
$$I_{sat} = \frac{Z}{2L}\mu_n C_{ox}\left(V_{GS} - V_T\right)^2$$



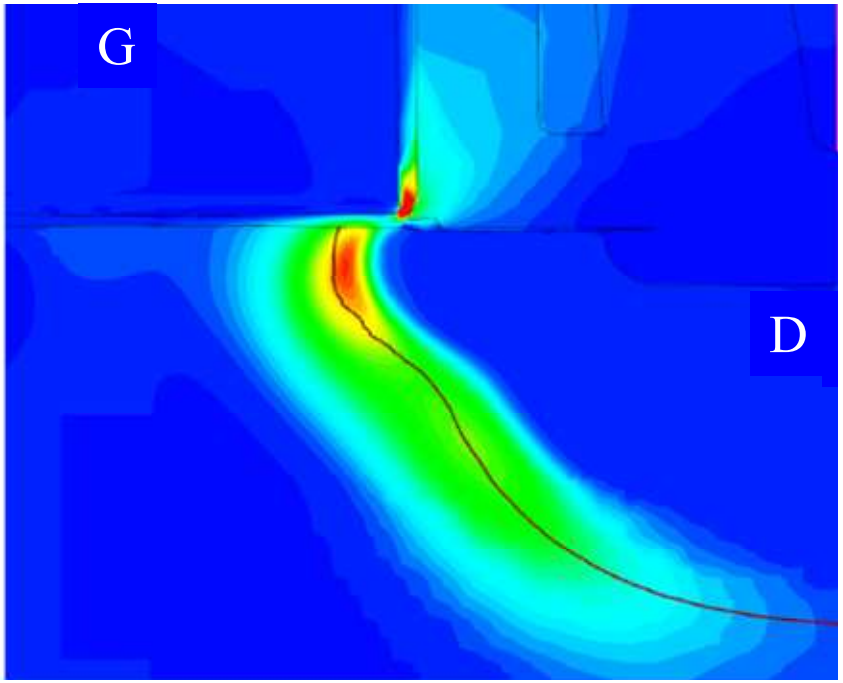




Saturation



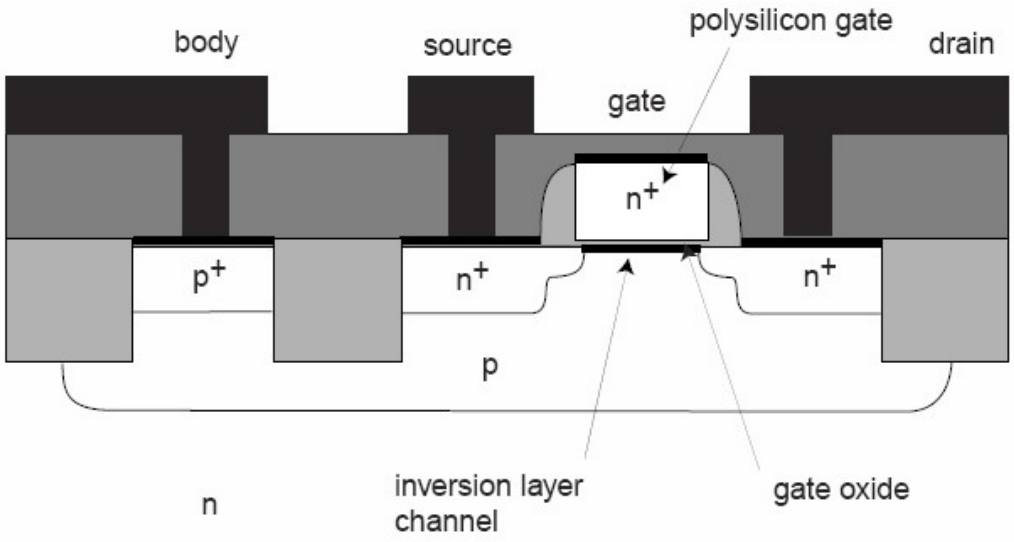
Potential



Electric field strength

Alexander Schiffmann, Master Thesis (2016)

Constant E-field Scaling



Gate length L, transistor width Z, oxide thickness t_{ox} are scaled down.

V_{ds}, V_{gs}, and V_T are reduced to keep the electric field constant.

Power density remains constant.

$$L \sim 45\ t_{ox}$$

1975 - 1990: "Days of happy scaling"

Constant E-field scaling

$$I_{sat} = \frac{Z}{2L}\mu_n \frac{\varepsilon_{ox}}{t_{ox}}\left(V_G - V_T\right)^2$$

$$L \Rightarrow sL, \qquad Z \Rightarrow sZ, \qquad t_{ox} \Rightarrow st_{ox}, \qquad V_{th} \Rightarrow sV_{th}$$

$$I_{sat} \Rightarrow sI_{sat} \quad \longleftarrow \quad I_{sat} \text{ gets smaller}$$

$$g_m = \frac{dI_D}{dV_G} = \frac{Z}{L}\mu_n \frac{\varepsilon_{ox}}{t_{ox}}\left(V_G - V_T\right) \quad \longleftarrow \quad \text{Transconductance stays the same.}$$

Power per transistor decreases like L^2. Power per unit area remains constant.

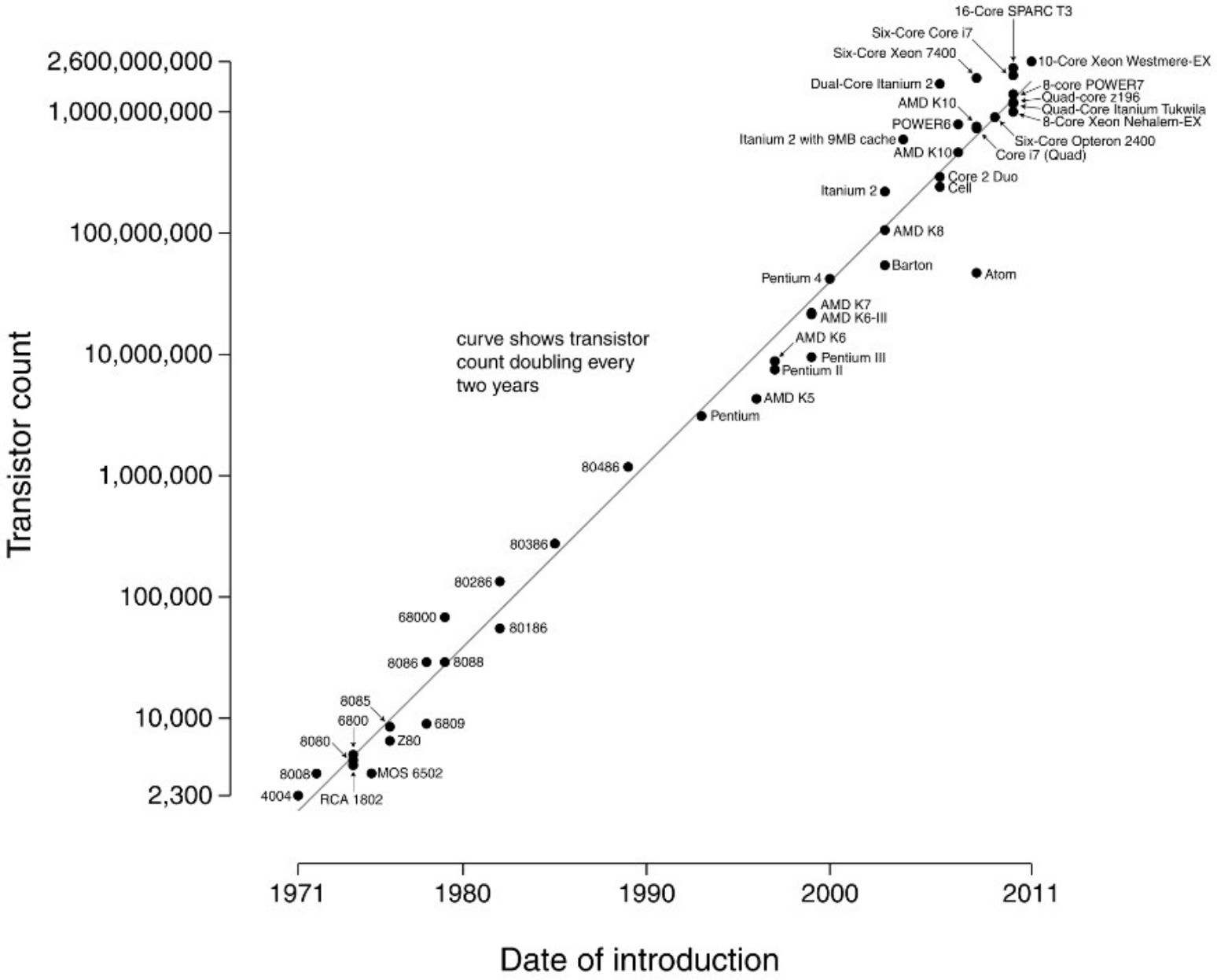
The heat dissipation problem

Microprocessors are hot ~ 100 C
Hotter operation will cause dopants to diffuse

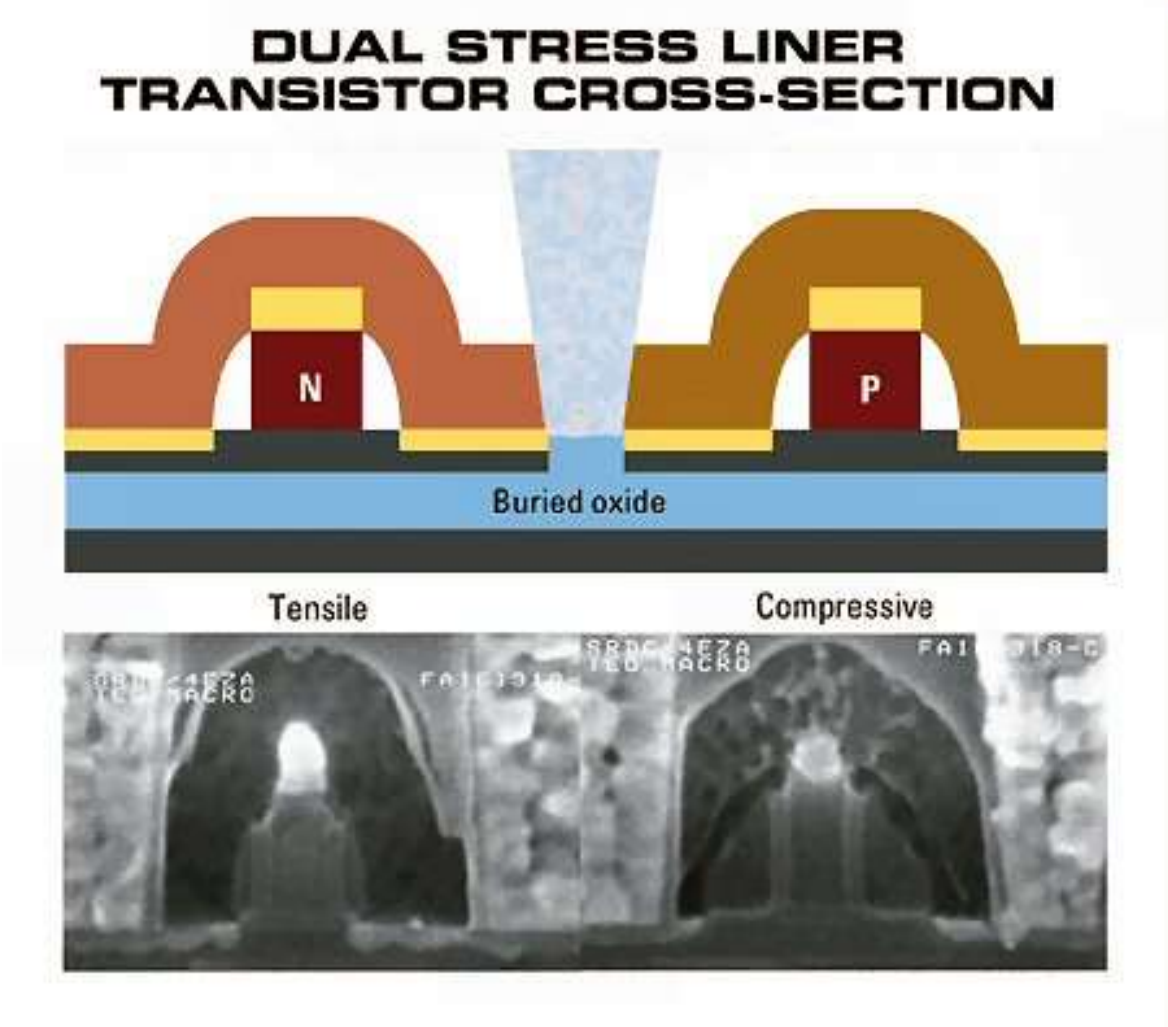
When more transistors are put on a chip they must dissipate less power.

Power per transistor decreases like L^2.

Microprocessor Transistor Counts 1971-2011 & Moore's Law



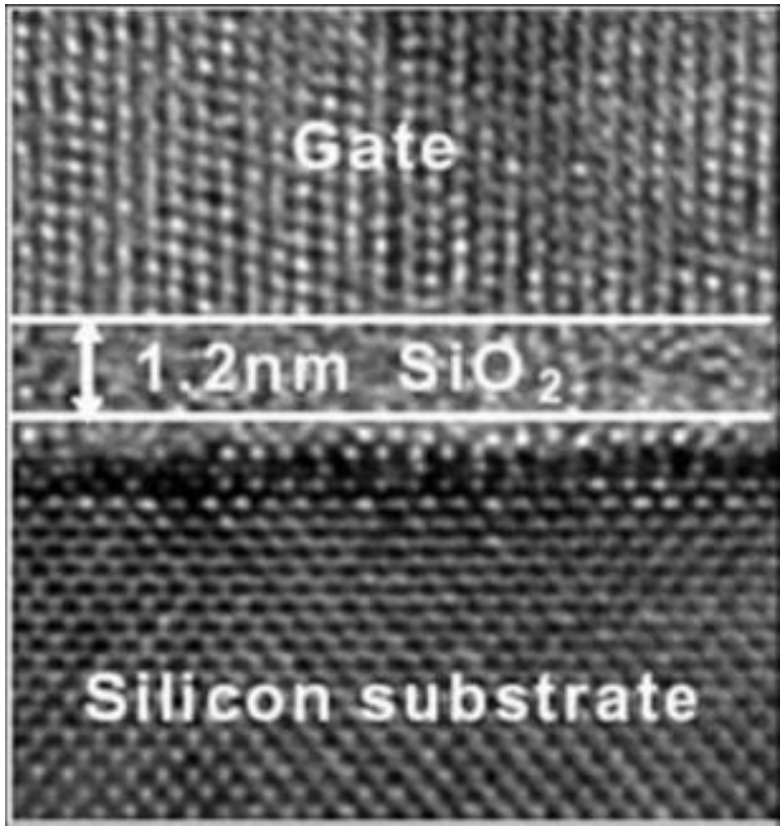
Dual stress liners



Tensile silicon nitride film over the NMOS and a compressive silicon nitride film over the PMOS improves the mobility.

http://www.xbitlabs.com/articles/cpu/display/athlon64-venice_2.html

Gate dielectric



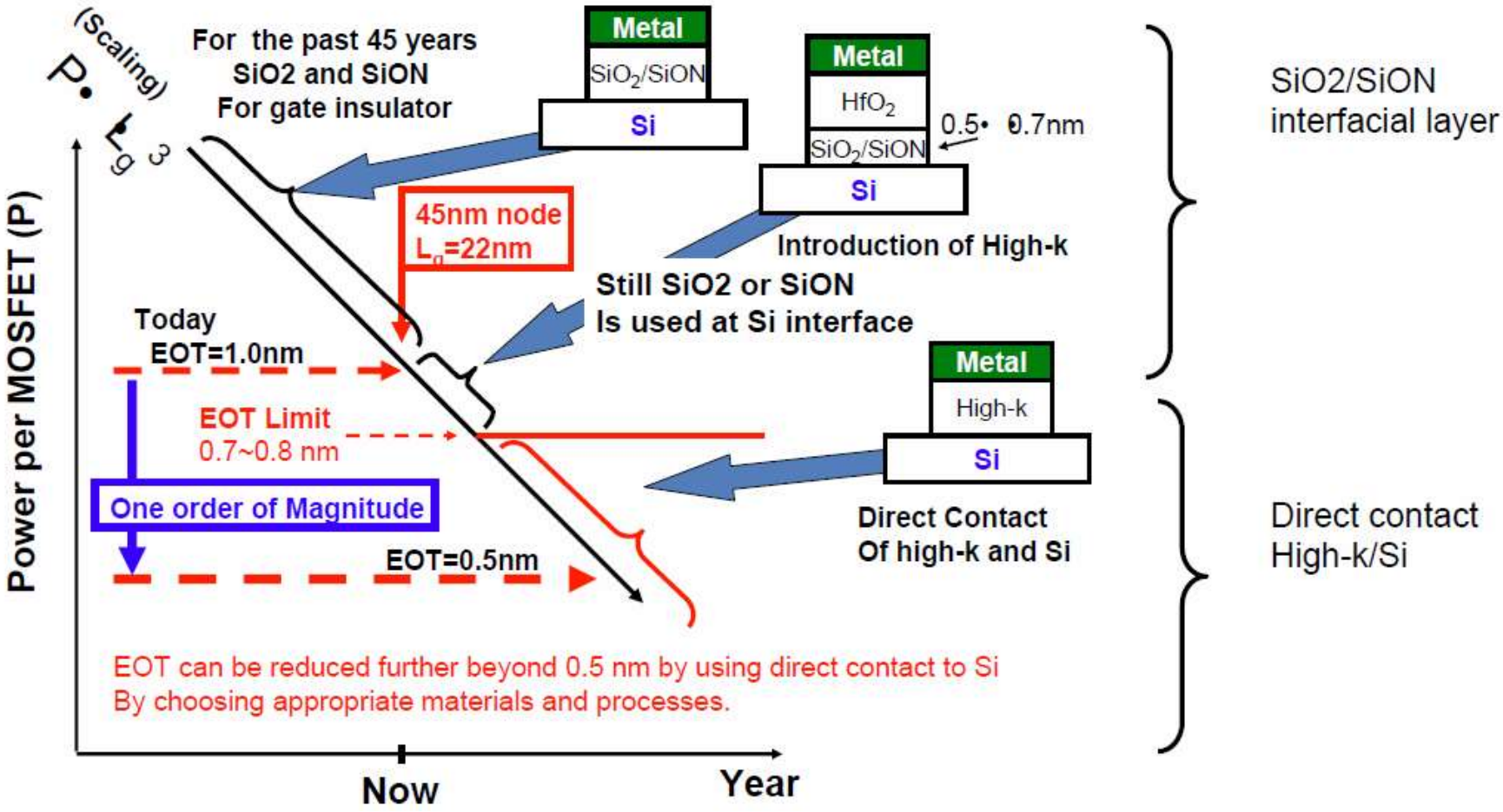
Thinner than 1 nm: electrons tunnel

Large dielectric constant desirable

$\varepsilon_r(SiO_2) \sim 4$

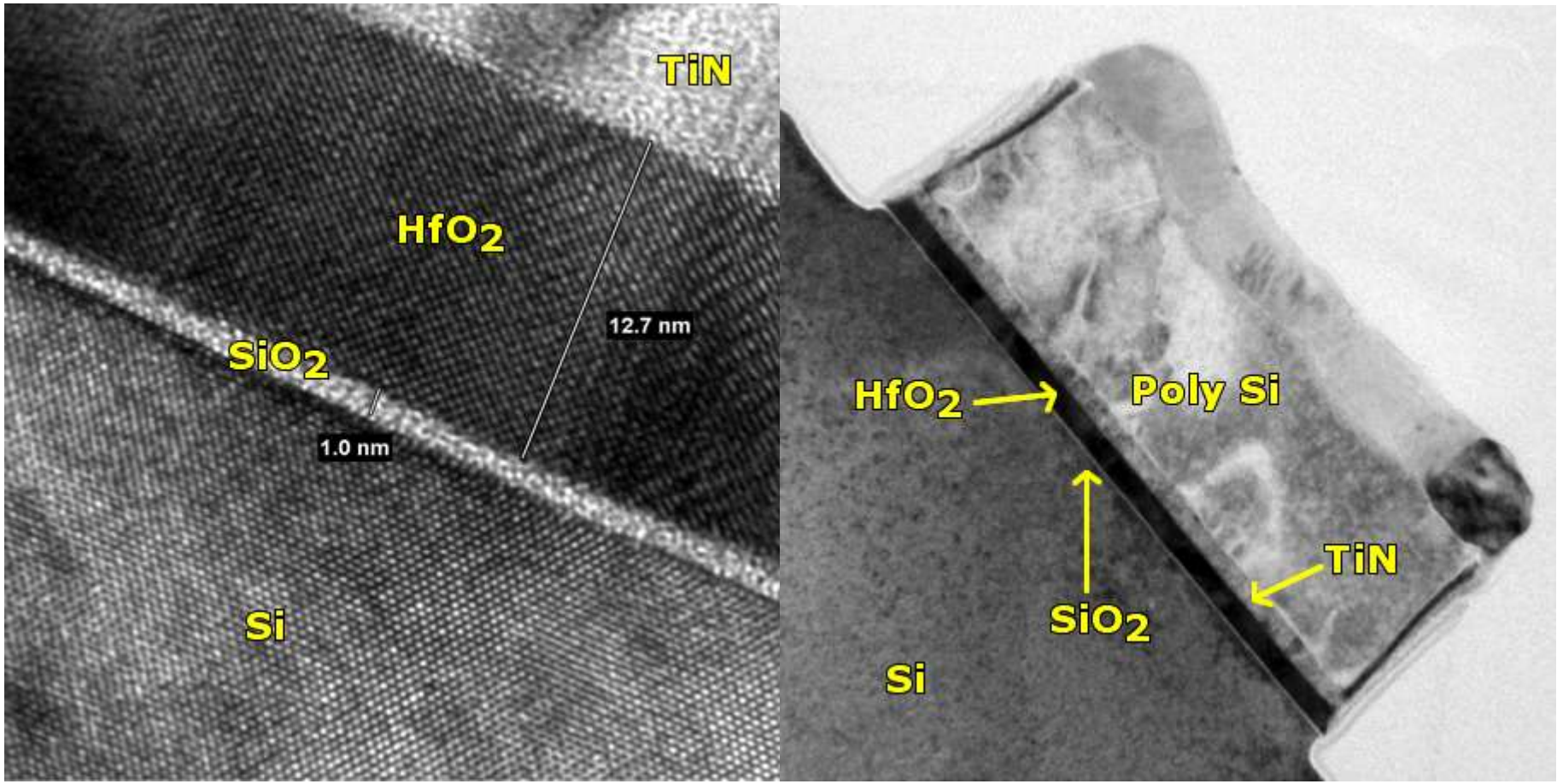
$\varepsilon_r(Si_3N_4) \sim 7$

Direct contact technology of high-k to Si



www.iwailab.ep.titech.ac.jp

High-k dielectrics



http://nano.boisestate.edu/research-areas/gate-oxide-studies/

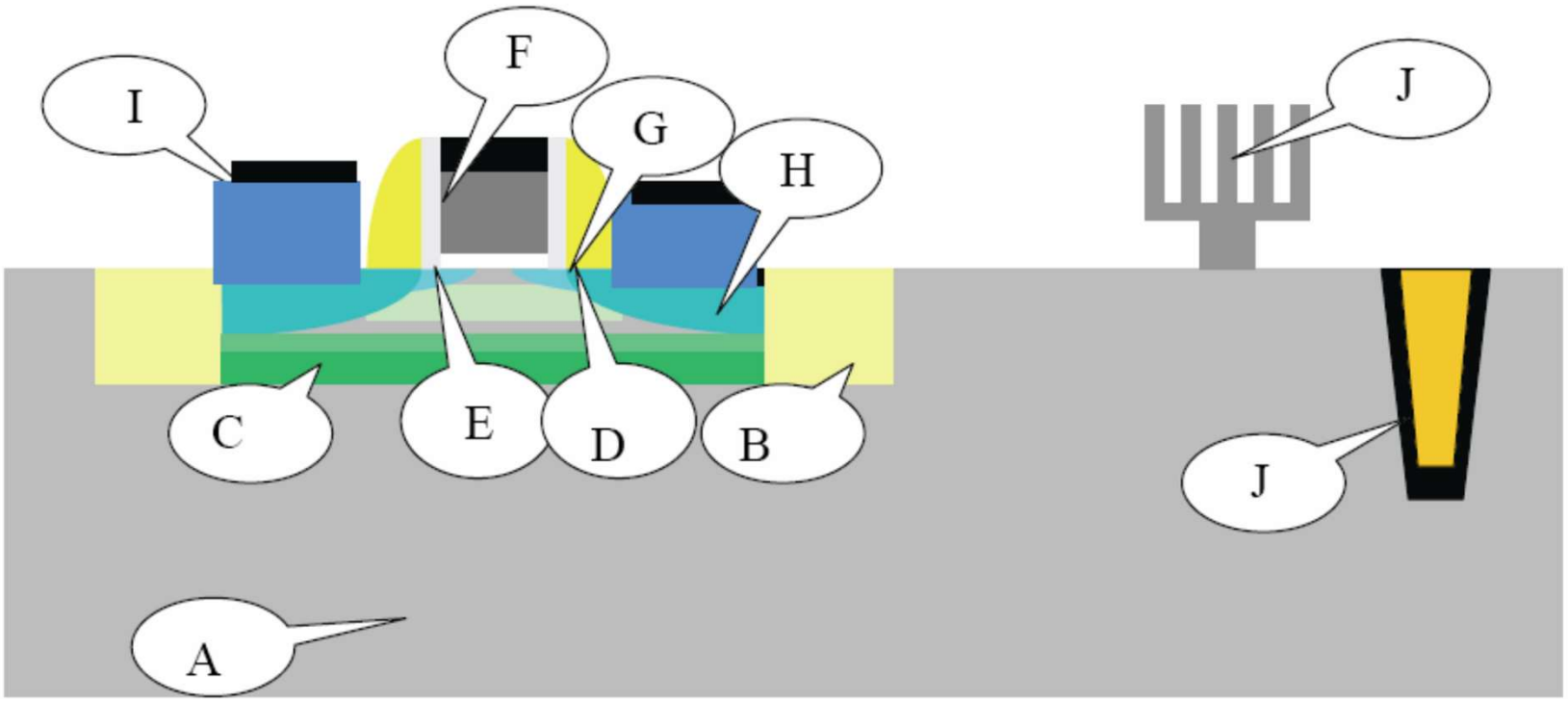
International Technology Roadmap for Semiconductors

Table PIDS2a High-performance (HP) Logic Technology Requirements - TCAD																
Year of Production	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028
Logic Industry "Node Range" Labeling (nm) [based on 0.7 'k reduction per "Node Range" ("Node" = '2x Nk)]	"16/14"		"11/10"		"8/7"		"6/5"		"4/3"		"3/2.5"		"2/1.5"		"1/0.75"	
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (contacted)	40	32	32	28.3	25.3	22.5	20.0	17.9	15.9	14.2	12.6	11.3	10.0	8.9	8	7.1
L_g : Physical Gate Length for HP Logic (nm)	20	18	16.7	15.2	13.9	12.7	11.6	10.6	9.7	8.8	8.0	7.3	6.7	6.1	5.6	5.1
L_{ch} : Effective Channel Length (nm) [3]	16.0	14.4	13.4	12.2	11.1	10.2	9.3	8.5	7.8	7.0	6.4	5.8	5.4	4.9	4.5	4.1
V_{dd} : Power Supply Voltage (V)																
Bulk/SOI/MG	0.86	0.85	0.83	0.81	0.80	0.78	0.77	0.75	0.74	0.72	0.71	0.69	0.68	0.66	0.65	0.64
EOT: Equivalent Oxide Thickness																
Bulk/SOI/MG (nm)	0.80	0.77	0.73	0.70	0.67	0.64	0.61	0.59	0.56	0.54	0.51	0.49	0.47	0.45	0.43	0.41
Dielectric constant (K) of gate dielectrics	12.5	13.0	13.5	14.0	14.5	15.0	15.5	16.0	16.5	17.0	17.5	18.0	18.5	19.0	19.5	20.0
Physical gate oxide thickness (nm)	2.56	2.57	2.53	2.51	2.49	2.46	2.42	2.42	2.37	2.35	2.29	2.26	2.23	2.19	2.15	2.10
Channel Doping (10^{18} /cm^3) [4]																
Bulk	6.0	7.0	7.7	8.4	9.0											
SOI/MG	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1
Body Thickness (nm) [5]																
SOI																
MG	6.4	5.8	5.3	4.9	4.4	4.1	3.7	3.4	3.1	2.8	2.6	2.3	2.1	2.0	1.8	1.6
T_{BOX} : Buried Oxide Thickness for SOI (nm) [6]																
SOI																
CET: Capacitance Equivalent Thickness (nm) [7]																
Bulk/SOI/MG	1.10	1.07	1.03	1.00	0.97	0.94	0.91	0.89	0.86	0.84	0.81	0.79	0.77	0.75	0.73	0.71
C_{ch} intrinsic (fF/μm) [8]																
Bulk/SOI/MG	0.502	0.465	0.448	0.420	0.396	0.373	0.352	0.329	0.311	0.289	0.273	0.255	0.240	0.225	0.212	0.198
Mobility (cm^2 /V-s)																
Bulk	400	400	400	400	400											
SOI																
MG	250	250	250	250	250	250	200	200	200	200	200	150	150	150	150	150
I_{off} (nA/μm) [9]																
Bulk/SOI/MG	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100
$I_{d,sat}$: NMOS Drive Current (μA/μm) [10]																
Bulk	1,348	1,355	1,340	1,295	1,267											
SOI																
MG	1670	1,680	1,700	1,660	1,660	1,610	1,600	1,480	1,450	1,350	1,330	1,170	1,100	1,030	970	900
$V_{t,lin}$ (V) [11]																
Bulk	0.306	0.327	0.324	0.357	0.378											

Equivalent oxide thickness (EOT)

$$\mathrm{EOT} = \frac{\varepsilon_{\mathrm{Si0_2}}}{\varepsilon} t_{\text{high-k}} + t_{\mathrm{Si0_2}}$$

Scaling can continue using oxides too thick to tunnel if they have a higher dielectric constant.



A: Starting Material
C: Well Doping
E: Channel Doping and Channel Strain
G: Extension Junction and Halo
I: Elevated Junction and Contacts

B: Isolation
D: Channel Surface (Preparation)
F: Gate Stack (Including Flash) and Spacer
H: Contacting Source/Drain Junction
J: DRAM Stack/Trench Cap. & FeRAM Storage

High frequencies

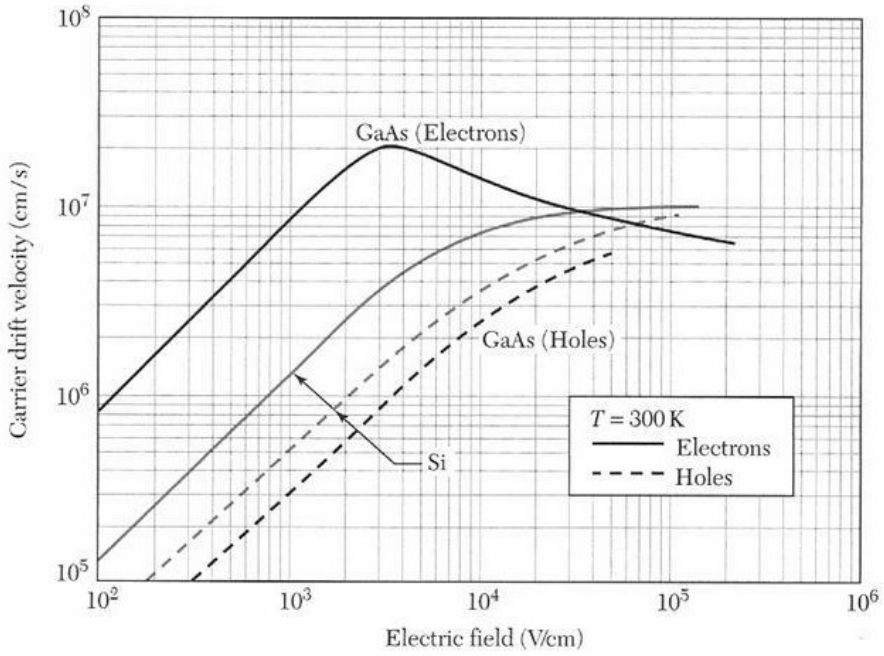
$$\tilde{i}_{in} = 2\pi f C_G \tilde{v}_G \qquad \tilde{i}_{out} = g_m \tilde{v}_G$$

$$\tilde{i}_{in} < \tilde{i}_{out}$$

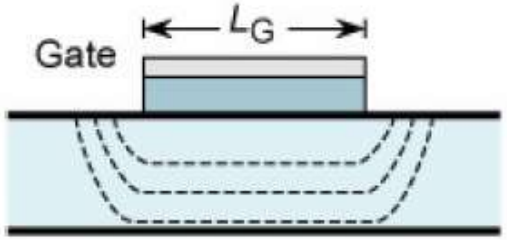
$$f < \frac{g_m}{2\pi C_G} \propto \frac{1}{s^2} = f_T$$

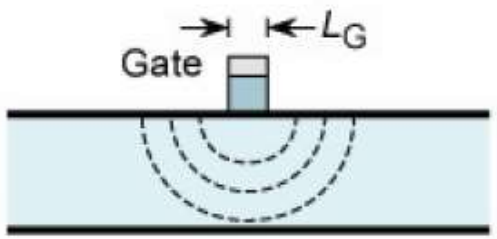
For large E, Ohm's law ($j = ne\mu E$) is not valid. The electron velocity saturates. For velocity saturation:

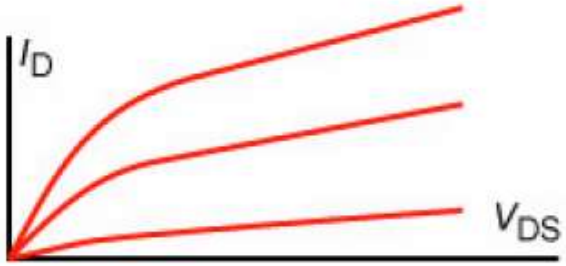
$$f_T \approx \frac{v_s}{L}$$



Short channel effects







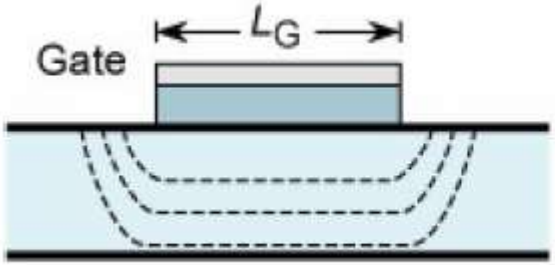
Short-channel effects:

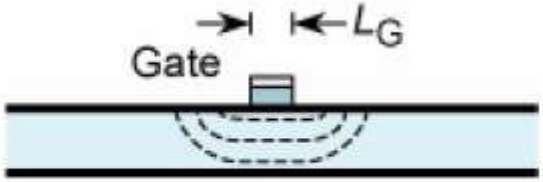
Threshold-voltage shift

Lack of pinch-off

Increased leakage current

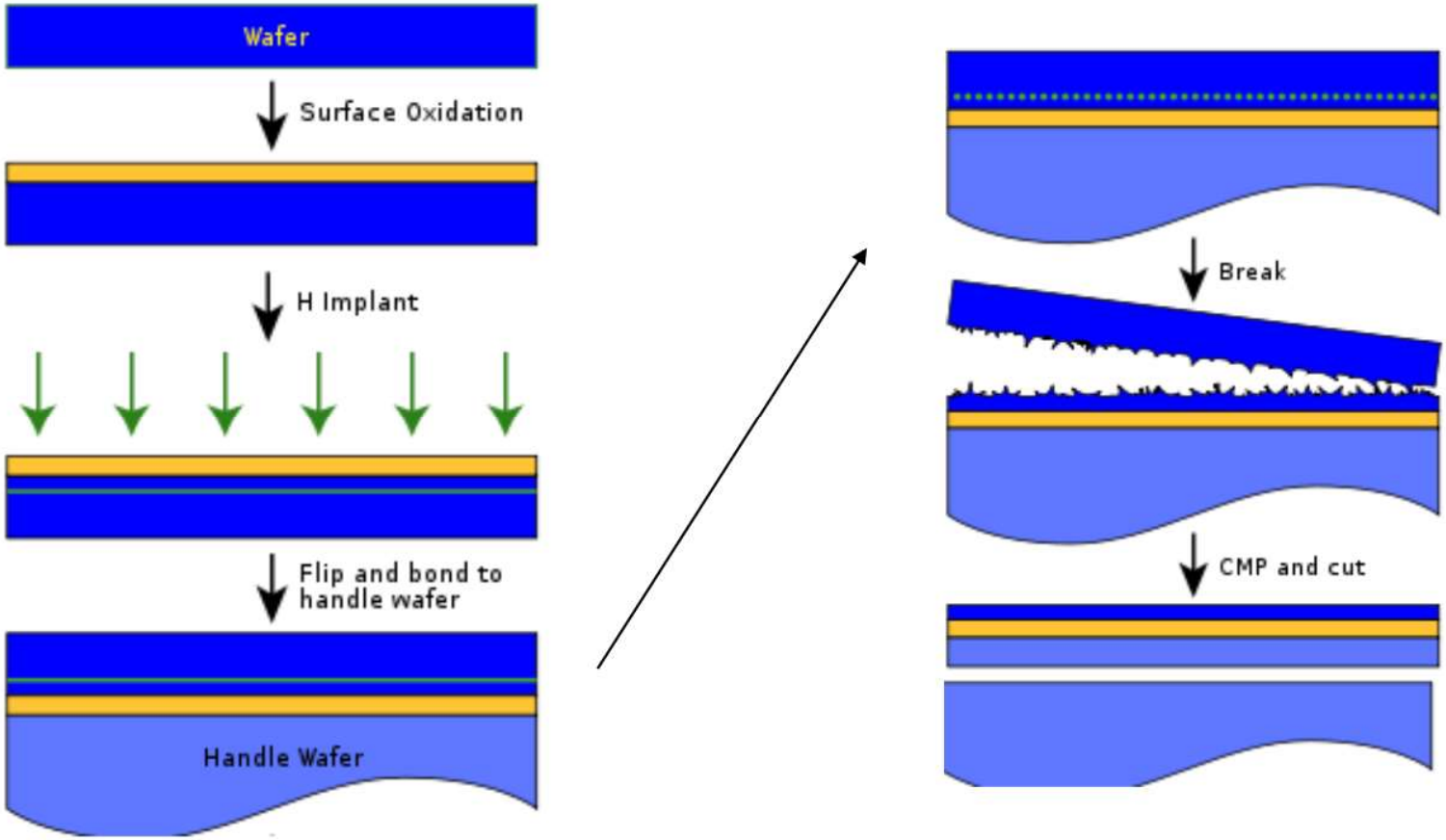
Increase of output conductance





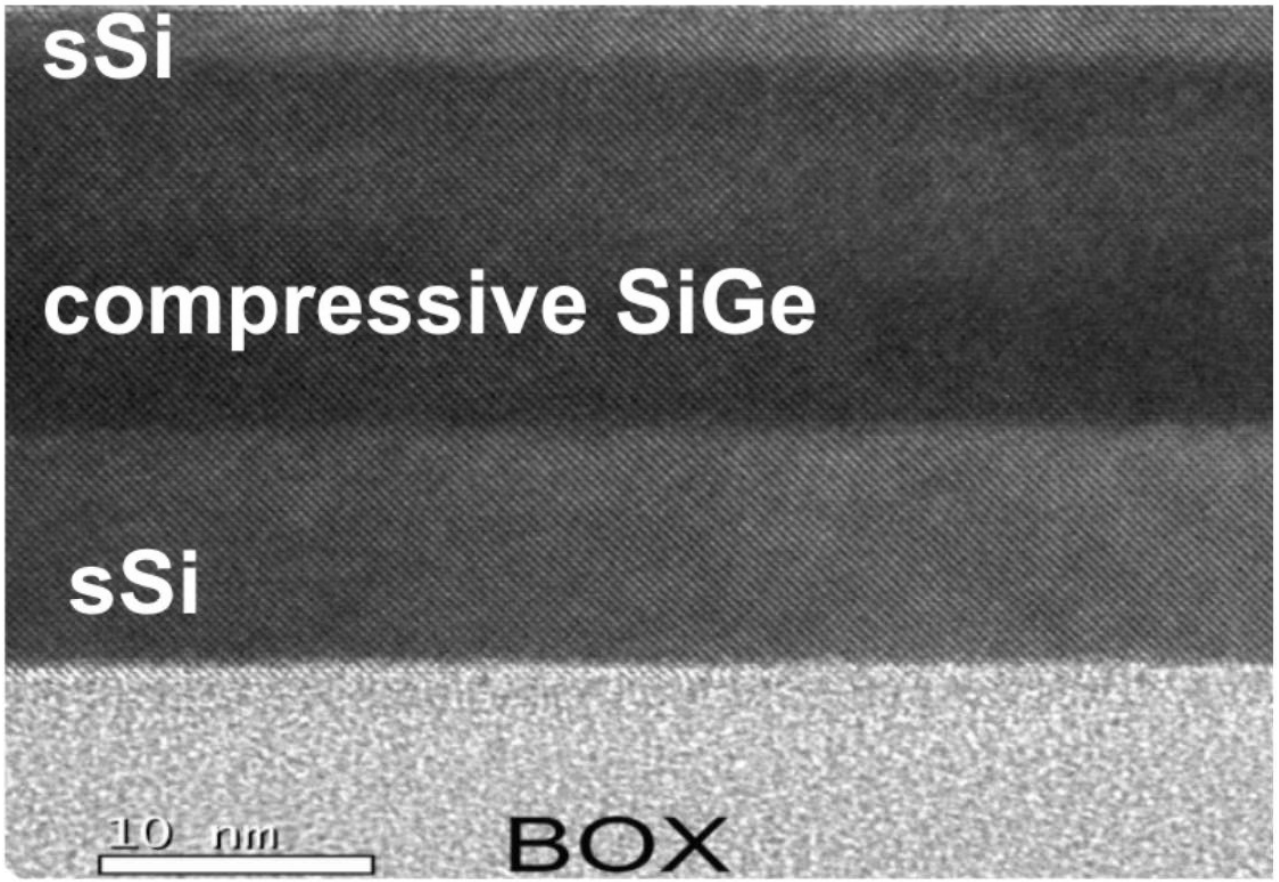
SOI: silicon on insulator

Smart Cut



http://en.wikipedia.org/wiki/Silicon_on_insulator

Buried Oxide

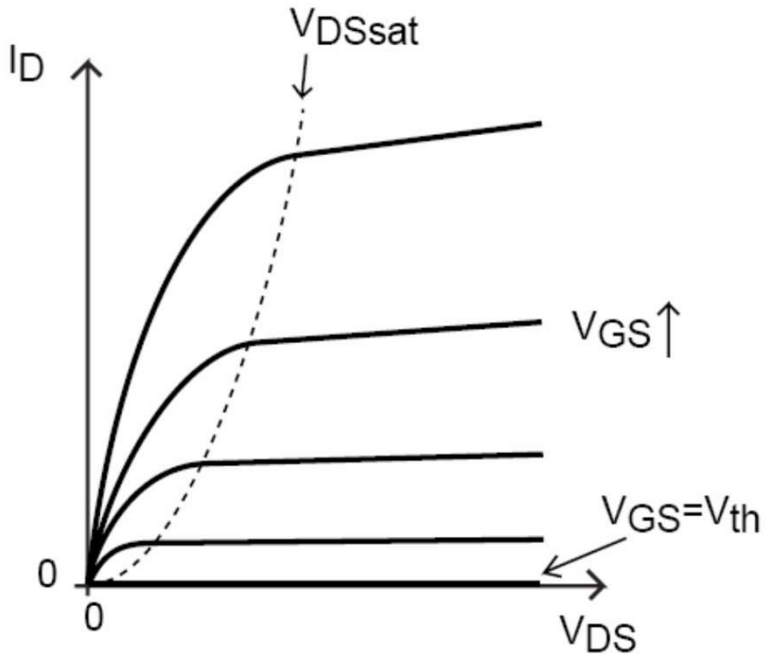


TEM image of a 3 nm Si cap/ 15 nm SiGe 50% /10 nm strained SOI structure grown at CEA-Leti and used for p-SiGe MOSFET fabrication.

http://www.fz-juelich.de/pgi/pgi-9/EN/Forschung/08-strained%20silicon/04_Biaxially%20strained%20Si_SiGe_%28S%29SOI%20heterostructure/_node.html

MOSFET (saturation regime)

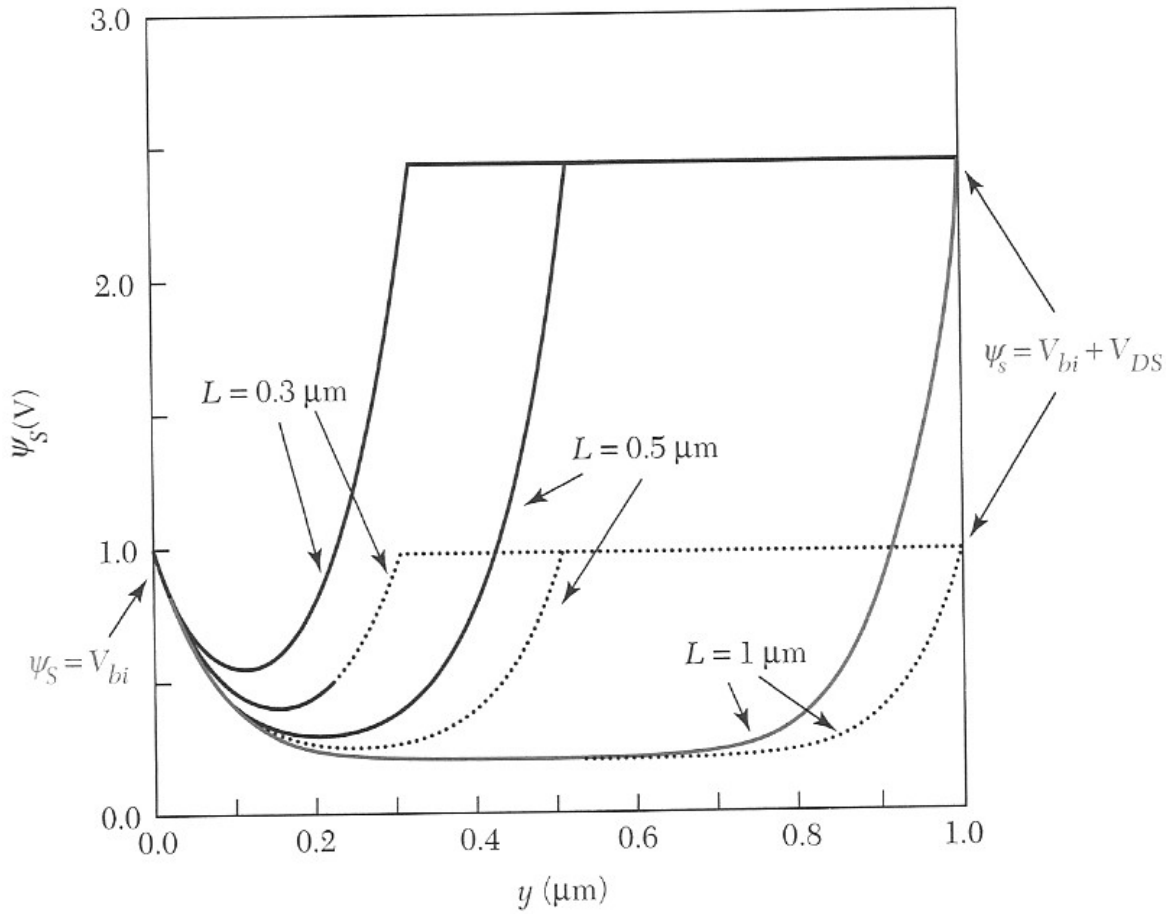
$$I_{sat} = \frac{Z}{2L}\mu_n C_{ox}\left(V_G - V_T\right)^2\left(1-\lambda\left(V_D - V_{sat}\right)\right)$$



Experimentally: channel length modulation

$$\lambda \propto \frac{1}{L}$$

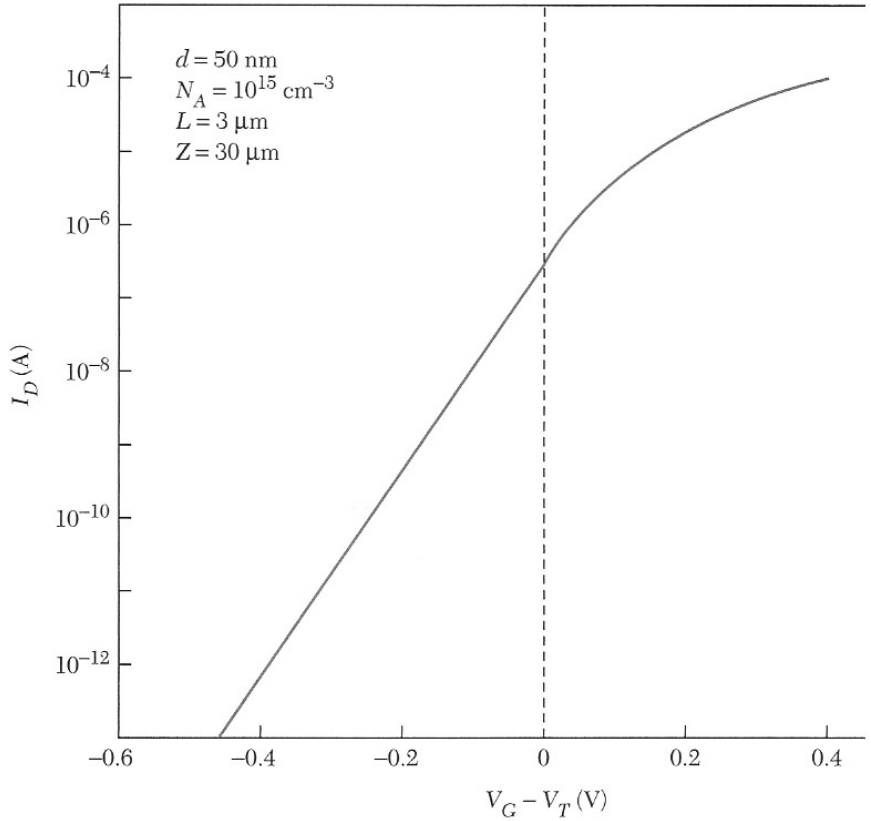
Drain-induced barrier lowering (DIBL)



In cut-off $V_G < V_T$, there should be a barrier that prevents current flow. This barrier is reduced in a short channel device.

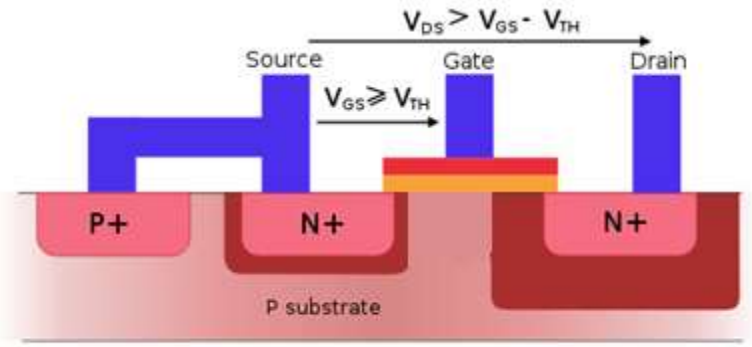
Subthreshold current

For $V_G < V_T$ the transistor should switch off but there is a diffusion current. The current is not really off until ~ 0.5 V below the threshold voltage.



Weak inversion

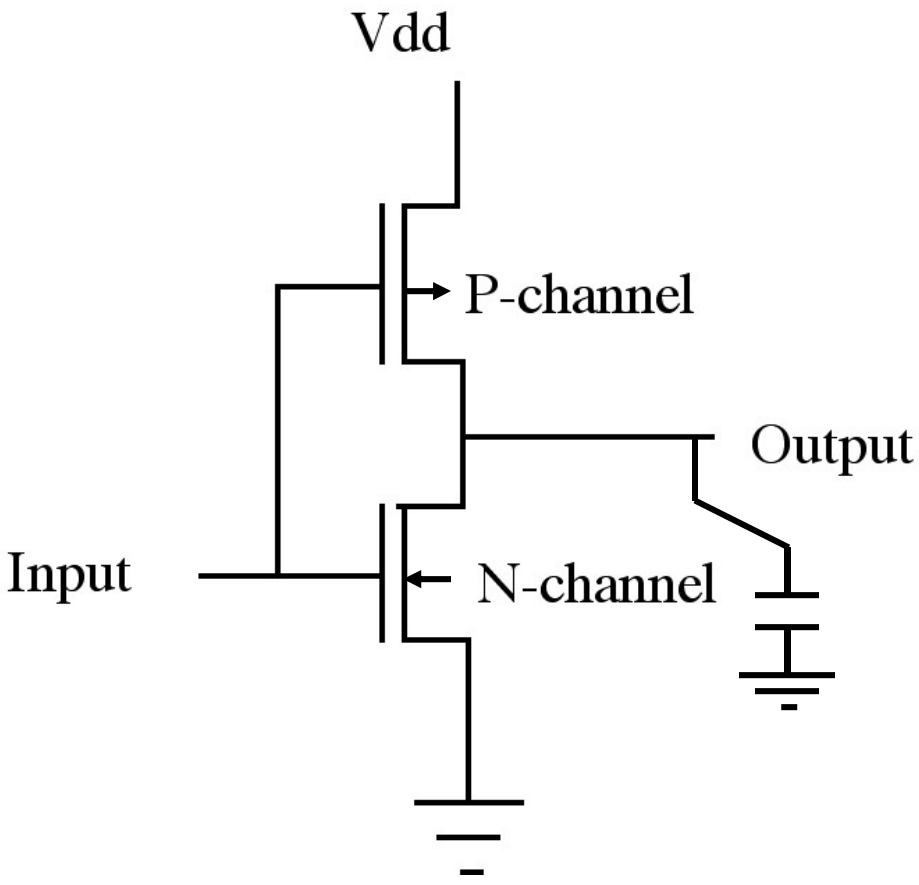
$$I_D \propto \exp\left(\frac{e(V_G - V_T)}{k_B T}\right)$$

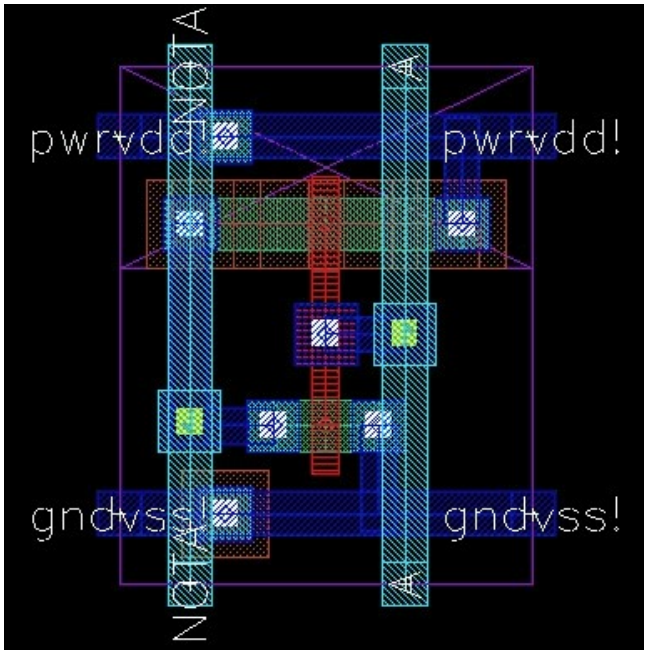


Subthreshold swing: 70-100 mV/decade

CMOS inverter

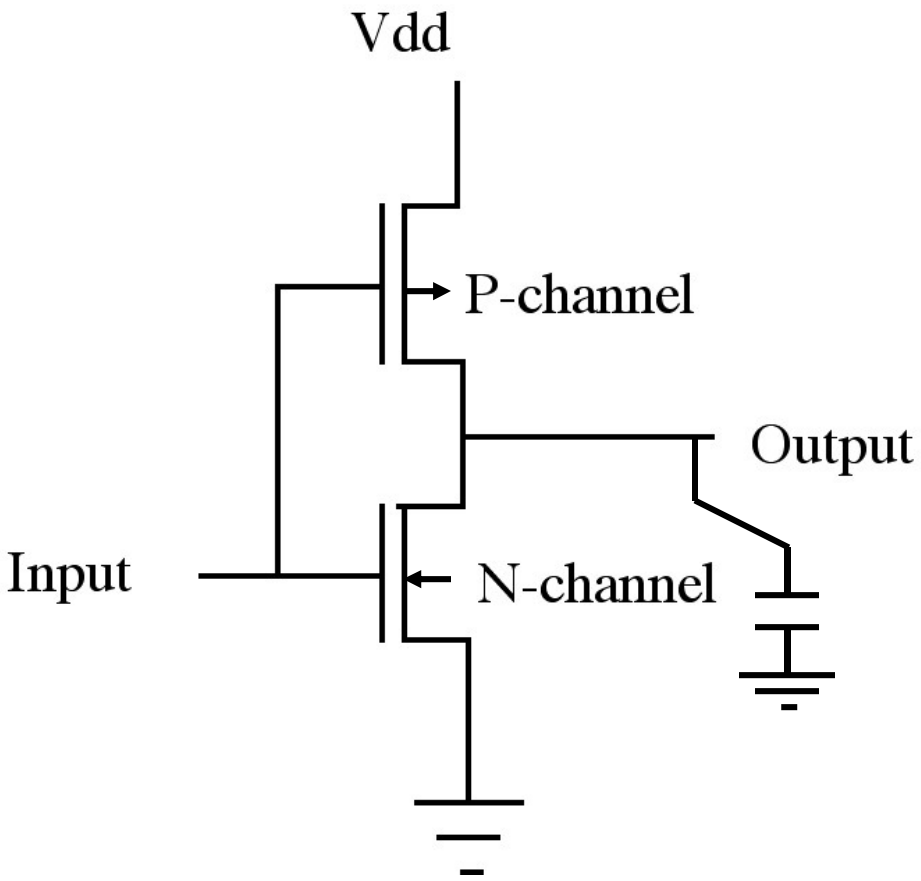
Complementary Metal Oxide Semiconductor



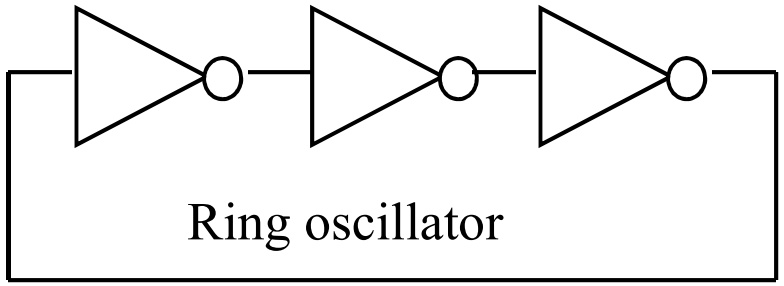


$$E = QV_{dd} = CV_{dd}^2$$

Gate delay

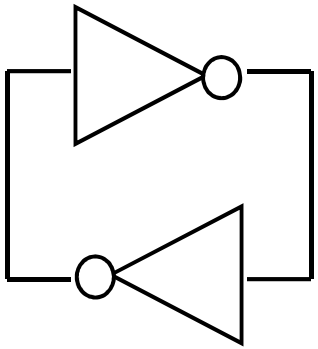


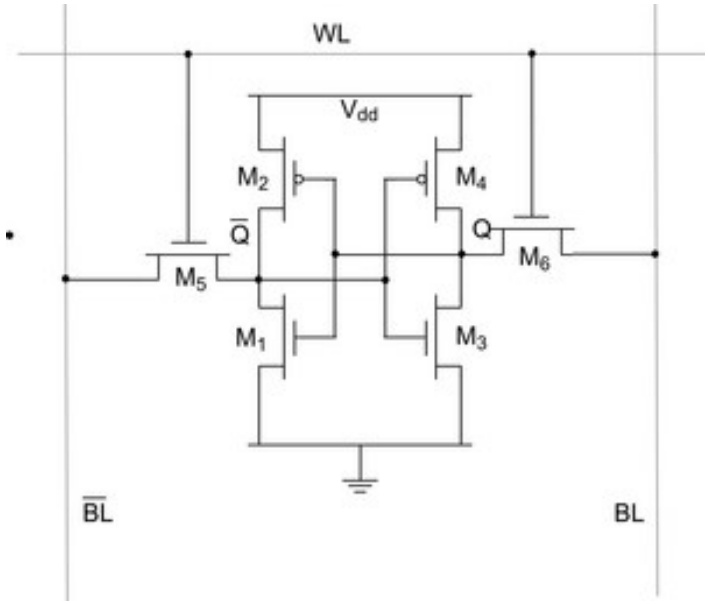
Gate delay is limited by $C_{gate}V_{dd}/I$.



SRAM

Static random access memory

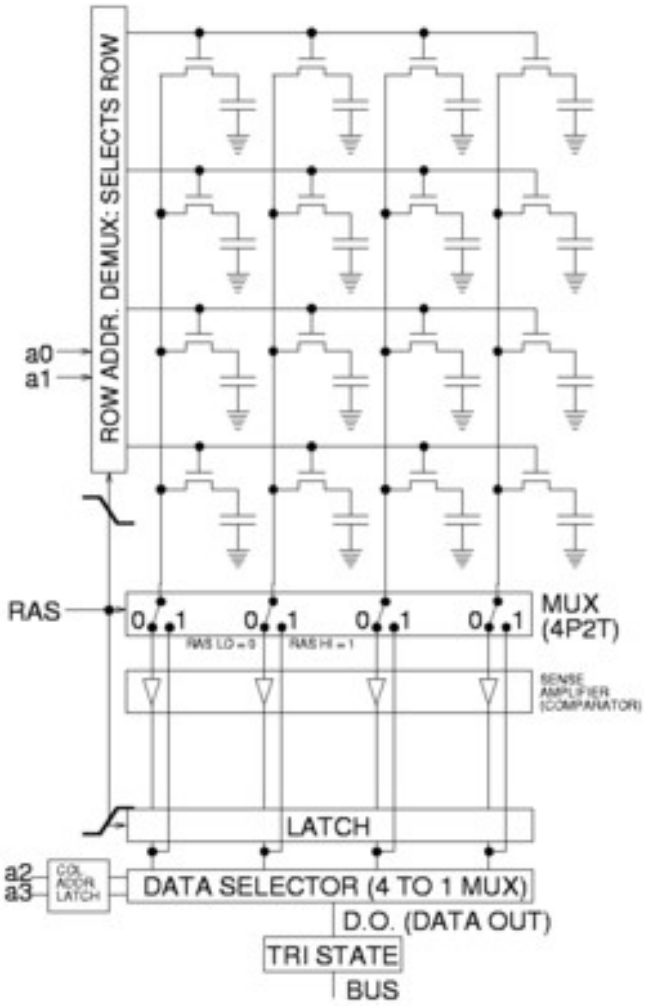




No refresh circuitry needed.

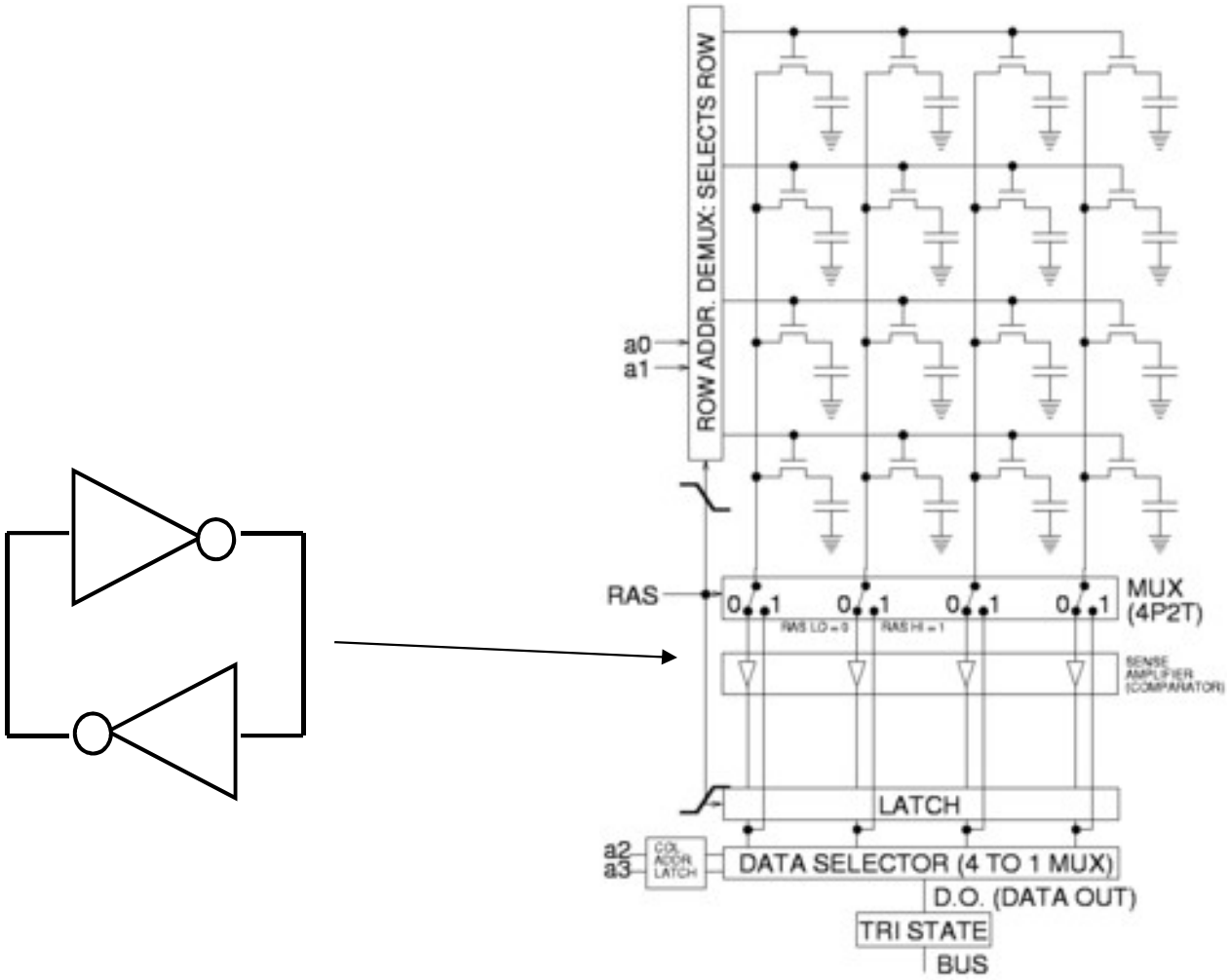
DRAM

Dynamic random access memory

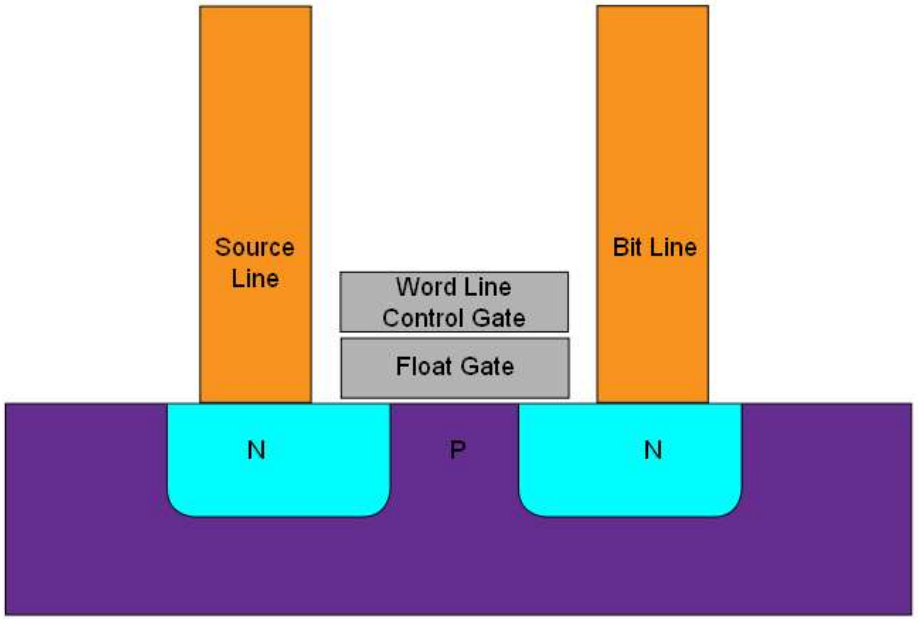


DRAM

Read and refresh DRAM with a SRAM cell



Flash memory



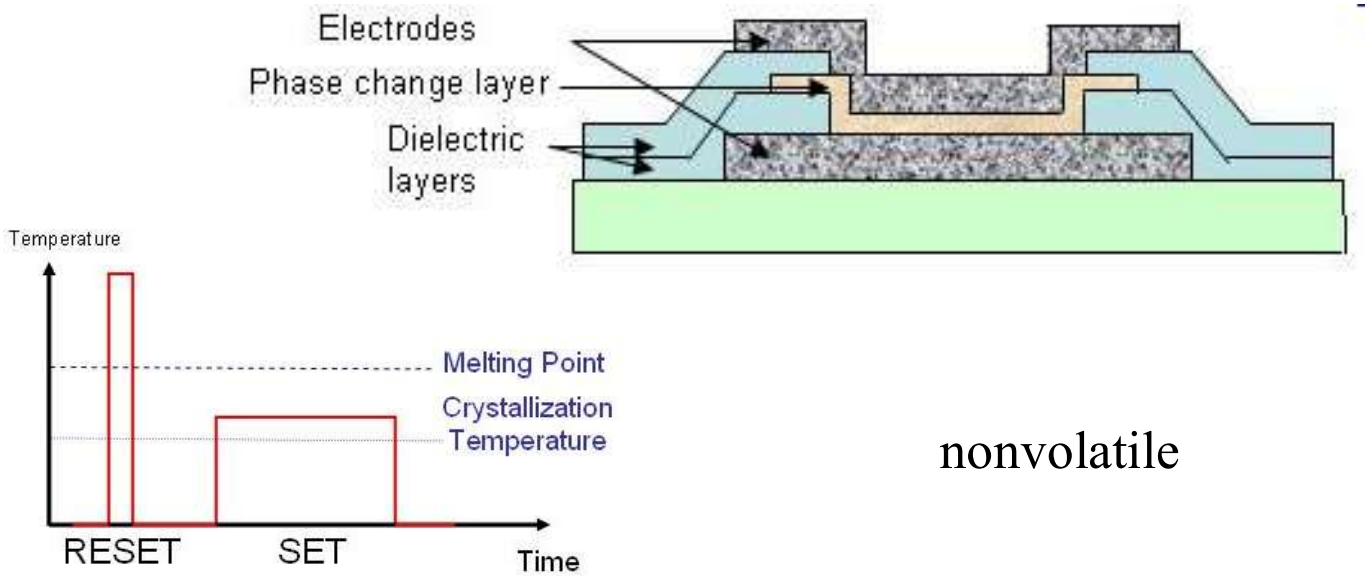
Charge is stored on a floating gate

nonvolatile

Phase change memory

Phase-change memory (PRAM) uses chalcogenide materials. These can be switched between a low resistance crystalline state and a high resistance amorphous state.

GeSbTe is melted by a laser in rewritable DVDs and by a current in PRAM.



nonvolatile