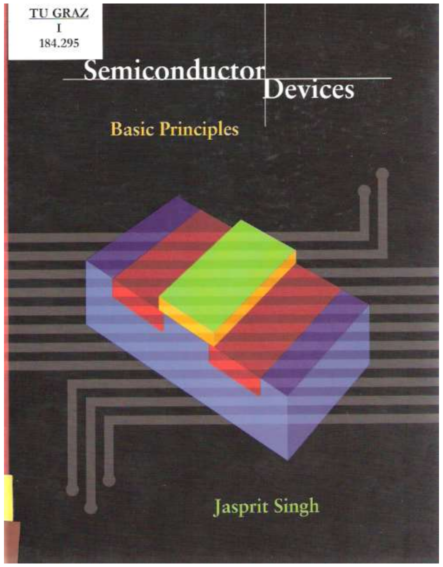
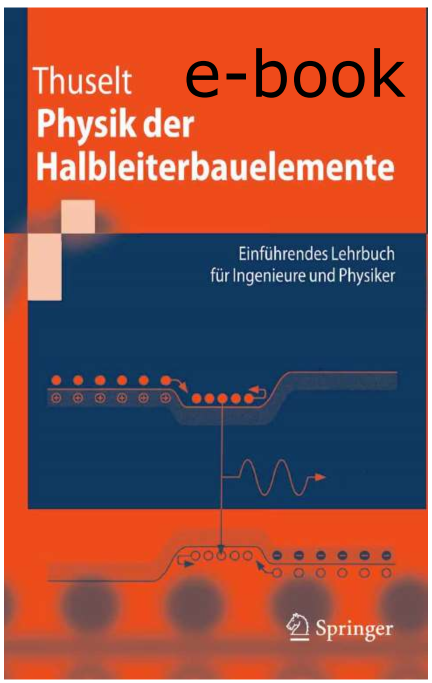
Physics of Semiconductor Devices

- Devices: diodes, solid state lasers, transistors
- Applications: computing, communications, controllers
- Energy: efficient lighting, solar cells

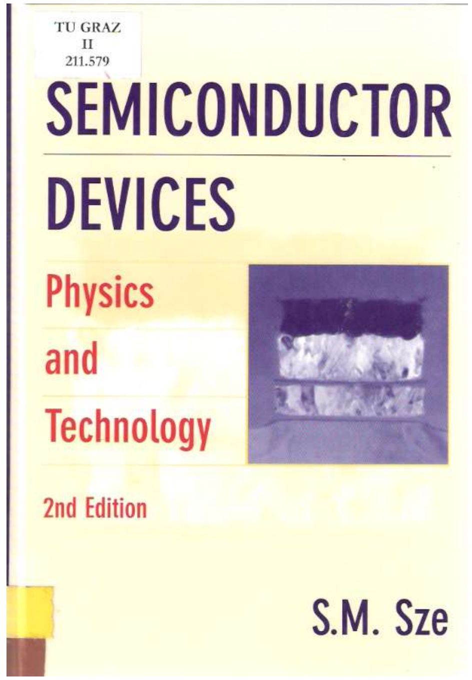
Peter Hadley

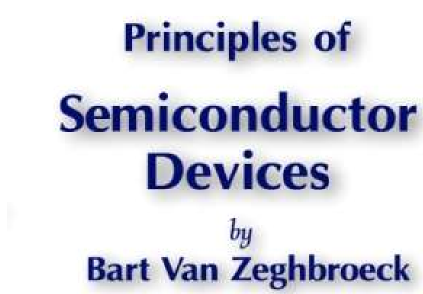
Books



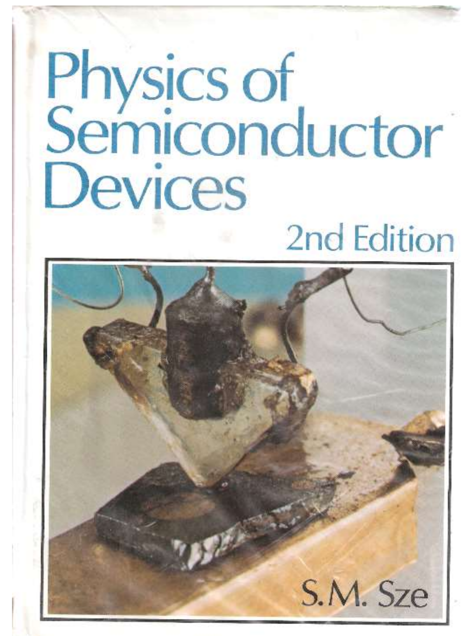


e-book



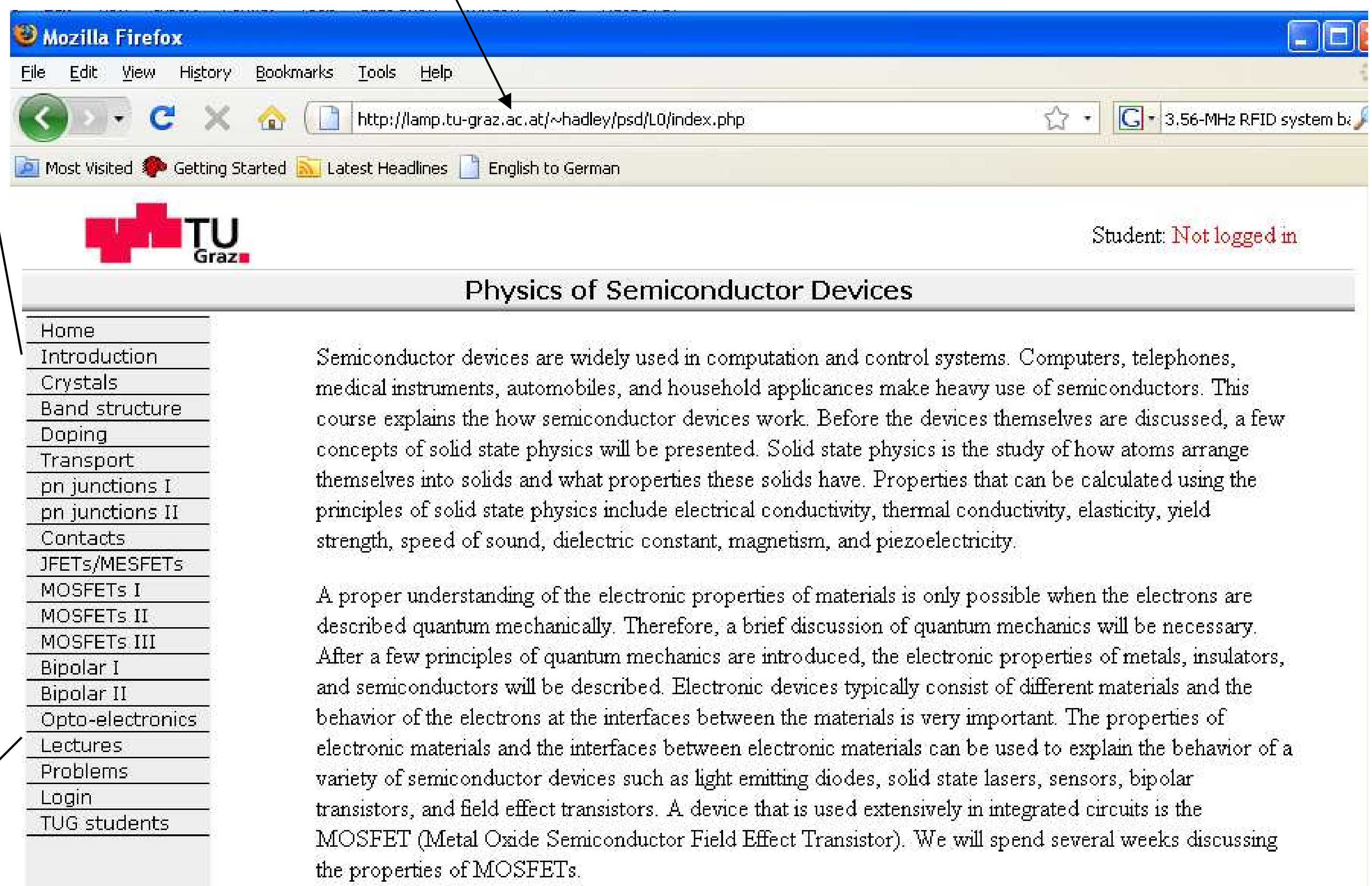


e-book



- Home
- Outline
- Introduction
- Crystals
- Intrinsic Semiconductors
- Extrinsic Semiconductors
- Transport
- pn junctions
- Contacts
- JFETs/MESFETs
- MOSFETs
- Bipolar transistors
- Opto-electronics
- Lectures
- Exam questions
- Making presentations
- TUG students
- Student projects

http://www.if.tugraz.at/psd.html



Examination

1 hour written exam

- 2 of the problems come from the old exam questions

1 Contribution to improve the course

- Solutions to exam questions
- Simulations

Oral exam

The first point contact transistor

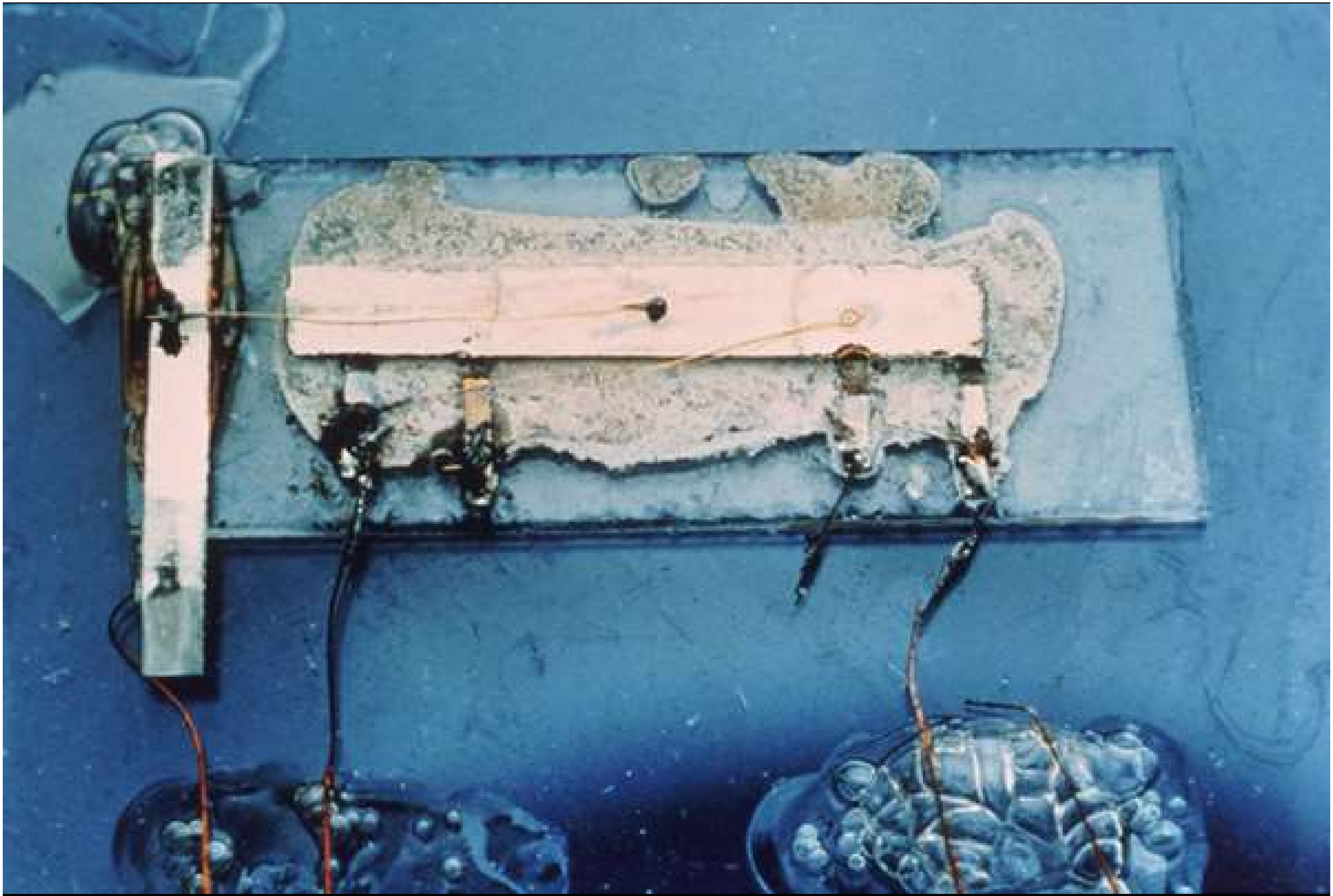
William Shockley, John Bardeen, and Walter Brattain

Bell Laboratories, Murray Hill, New Jersey (1947)

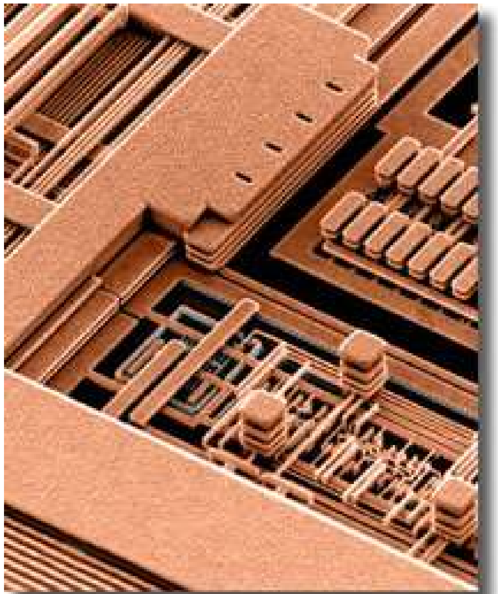
Bardeen *Brattain*

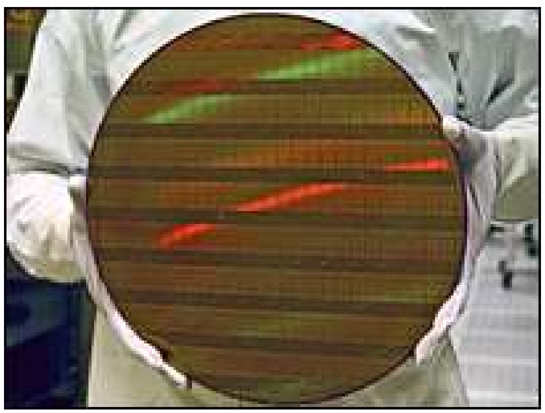
Shockley

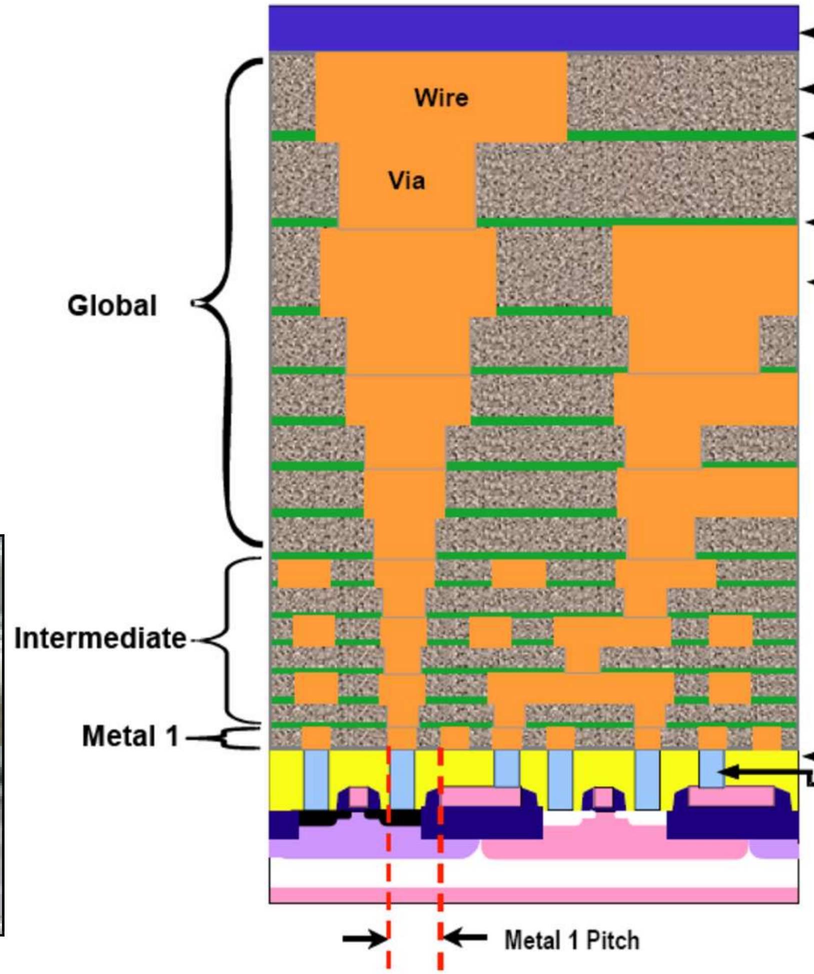

VALVO
EZ80

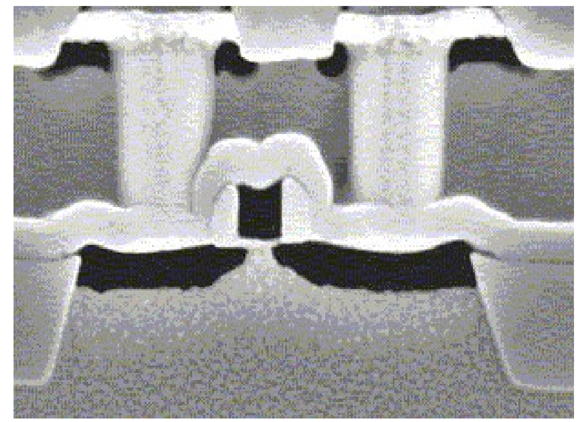


Jack Kilby's first integrated circuit 1958









$10^9 \sim 100$ €

Table PIDS2a High-performance (HP) Logic Technology Requirements

	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028
node	"16/14"		"11/10"		"8/7"		"6/5"		"4/3"		"3/2.5"		"2/1.5"		"1/0.75"	
metal 1/2 pitch	40	32	32	28.3	25.3	22.5	20.0	17.9	15.9	14.2	12.6	11.3	10.0	8.9	8	7.1
gate length	20	18	16.7	15.2	13.9	12.7	11.6	10.6	9.7	8.8	8.0	7.3	6.7	6.1	5.6	5.1

International Technology Roadmap for Semiconductors

ITRS 2009 Edition

http://www.itrs.net/reports.html

Table PIDS2a High-performance (HP) Logic Technology Requirements - TCAD

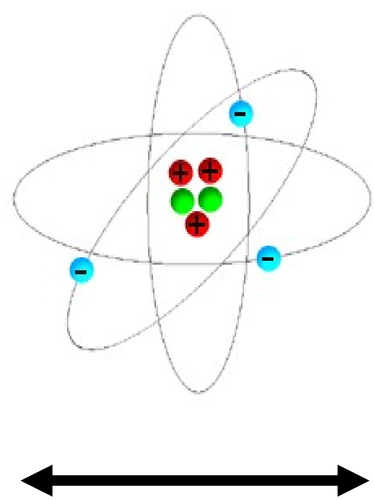
Year of Production	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028
Logic Industry "Node Range" Labeling (nm) [based on 0.71x reduction per "Node Range" ("Node" = 2x Mx)]	"16/14"		"11/10"		"8/7"		"6/5"		"4/3"		"3/2.5"		"2/1.5"		"1/0.75"	
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (contacted)	40	32	32	28.3	25.3	22.5	20.0	17.9	15.9	14.2	12.6	11.3	10.0	8.9	8	7.1
L_g : Physical Gate Length for HP Logic (nm)	20	18	16.7	15.2	13.9	12.7	11.6	10.6	9.7	8.8	8.0	7.3	6.7	6.1	5.6	5.1
L_{ch} : Effective Channel Length (nm) [3]	16.0	14.4	13.4	12.2	11.1	10.2	9.3	8.5	7.8	7.0	6.4	5.8	5.4	4.9	4.5	4.1
V_{dd} : Power Supply Voltage (V)																
Bulk/SOI/MG	0.86	0.85	0.83	0.81	0.80	0.78	0.77	0.75	0.74	0.72	0.71	0.69	0.68	0.66	0.65	0.64
EOT: Equivalent Oxide Thickness																
Bulk/SOI/MG (nm)	0.80	0.77	0.73	0.70	0.67	0.64	0.61	0.59	0.56	0.54	0.51	0.49	0.47	0.45	0.43	0.41
Dielectric constant (K) of gate dielectrics	12.5	13.0	13.5	14.0	14.5	15.0	15.5	16.0	16.5	17.0	17.5	18.0	18.5	19.0	19.5	20.0
Physical gate oxide thickness (nm)	2.56	2.57	2.53	2.51	2.49	2.46	2.42	2.42	2.37	2.35	2.29	2.26	2.23	2.19	2.15	2.10
Channel Doping (10^{18} /cm^3) [4]																
Bulk	6.0	7.0	7.7	8.4	9.0											
SOI/MG	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1
Body Thickness (nm) [5]																
SOI																
MG	6.4	5.8	5.3	4.9	4.4	4.1	3.7	3.4	3.1	2.8	2.6	2.3	2.1	2.0	1.8	1.6
T_{BOX} : Buried Oxide Thickness for SOI (nm) [6]																
SOI																
CET: Capacitance Equivalent Thickness (nm) [7]																
Bulk/SOI/MG	1.10	1.07	1.03	1.00	0.97	0.94	0.91	0.89	0.86	0.84	0.81	0.79	0.77	0.75	0.73	0.71
C_{ch} intrinsic (fF/µm) [8]																
Bulk/SOI/MG	0.502	0.465	0.448	0.420	0.396	0.373	0.352	0.329	0.311	0.289	0.273	0.255	0.240	0.225	0.212	0.198
Mobility (cm^2 /V-s)																
Bulk	400	400	400	400	400											
SOI																
MG	250	250	250	250	250	250	200	200	200	200	200	150	150	150	150	150
I_{off} (nA/µm) [9]																
Bulk/SOI/MG	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100
$I_{d,sat}$: NMOS Drive Current (µA/µm) [10]																
Bulk	1,348	1,355	1,340	1,295	1,267											
SOI																
MG	1670	1,680	1,700	1,660	1,660	1,610	1,600	1,480	1,450	1,350	1,330	1,170	1,100	1,030	970	900
$V_{t,lin}$ (V) [11]																
Bulk	0.306	0.327	0.334	0.357	0.378											
SOI																
MG	0.219	0.225	0.231	0.239	0.264	0.266	0.265	0.276	0.295	0.303	0.306	0.319	0.334	0.340	0.354	0.364

Electrons

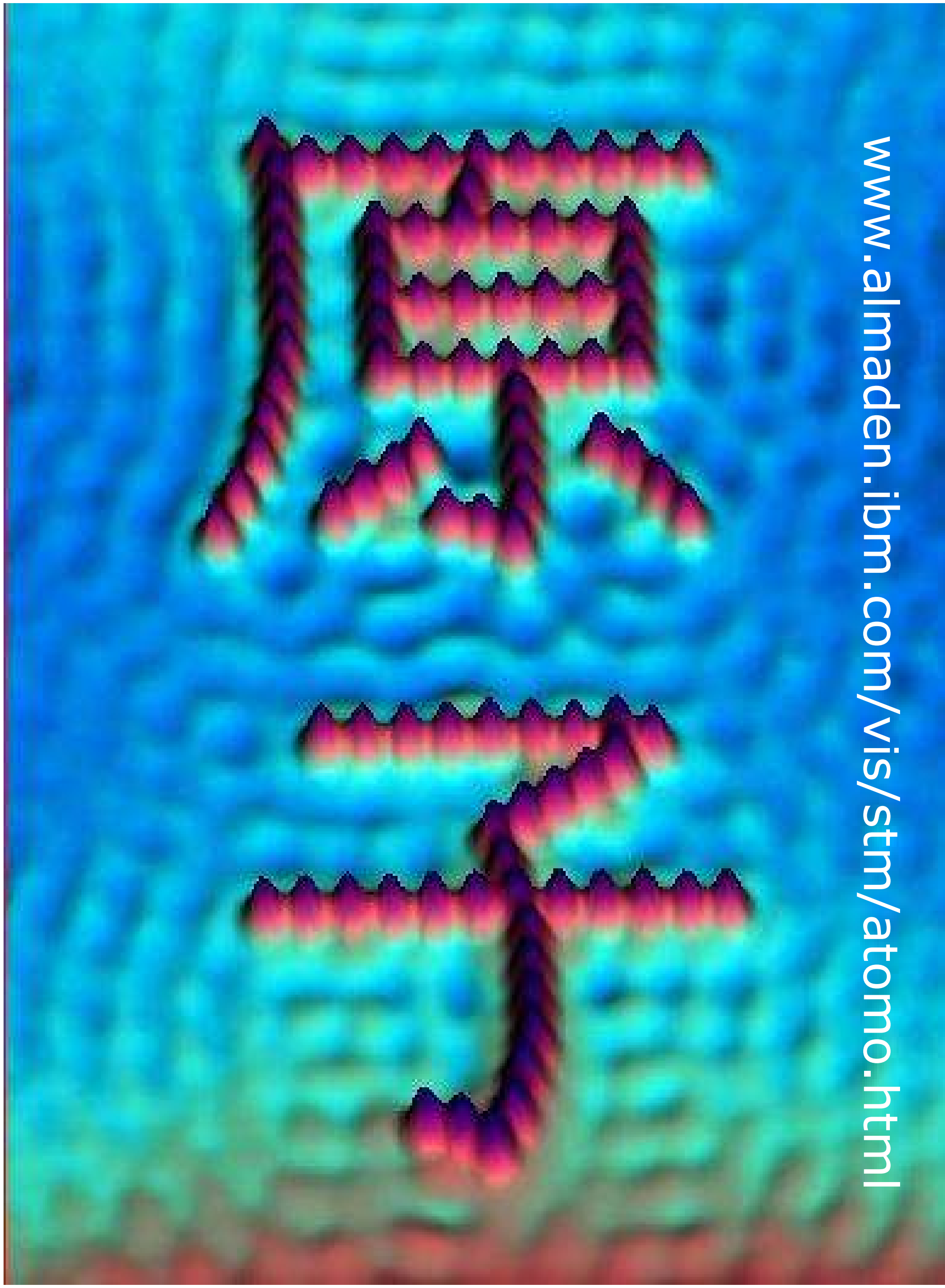
Charge = -1.6022×10^{-19} C

Mass = 9.11×10^{-31} kg

Radius = ?



0.15 nm



Quantum Mechanics

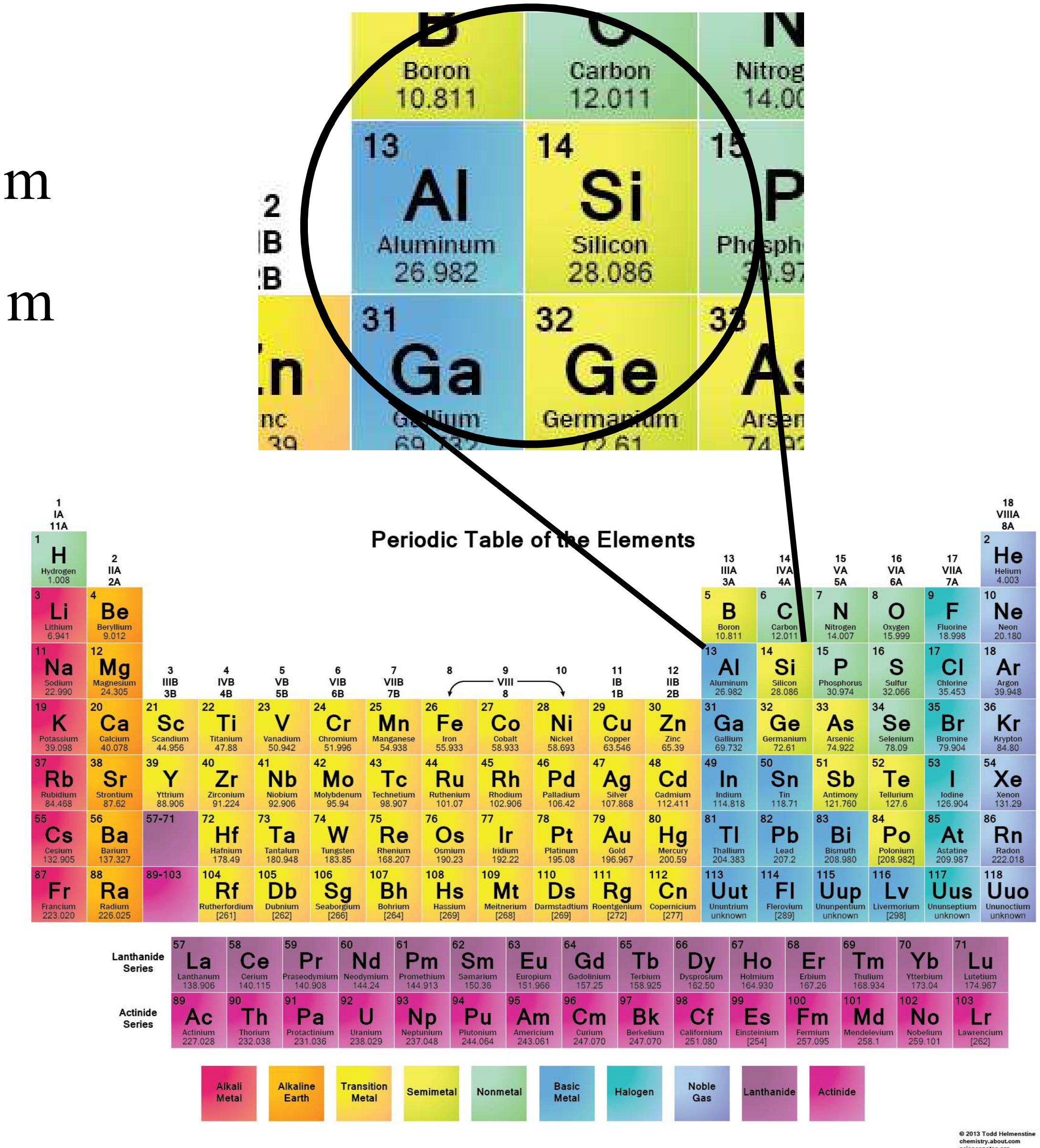
Everything moves like a wave but exchanges energy and momentum like a particle.

Everything moves like a wave but exchanges energy and momentum like a particle.

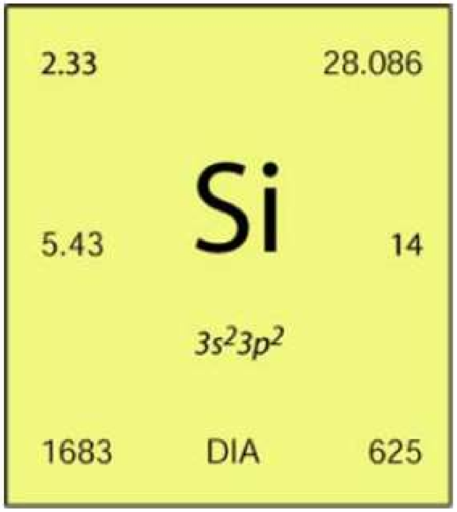
Conductivity

Al: $\sigma = 3.5 \times 10^{7}\ 1/\Omega\cdot m$

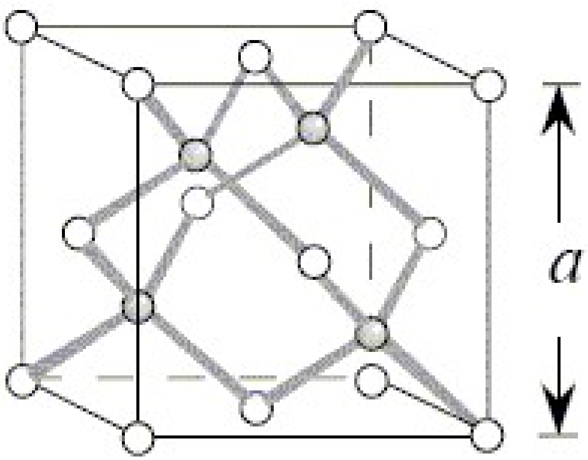
Si: $\sigma = 4.3 \times 10^{-4}\ 1/\Omega\cdot m$



Silicon



- Important semiconducting material
- 2nd most common element on earths crust (rocks, sand, glass, concrete)
- Often doped with other elements
- Oxide SiO_2 is a good insulator

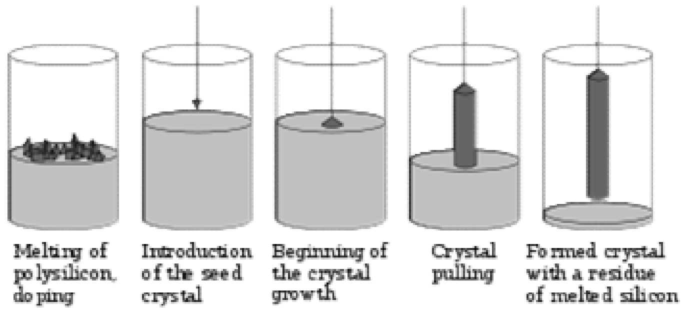


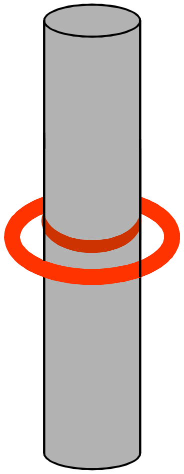
silicon crystal = diamond crystal structure

Silicon

Large (2 m) single crystals are grown

Czochralski process



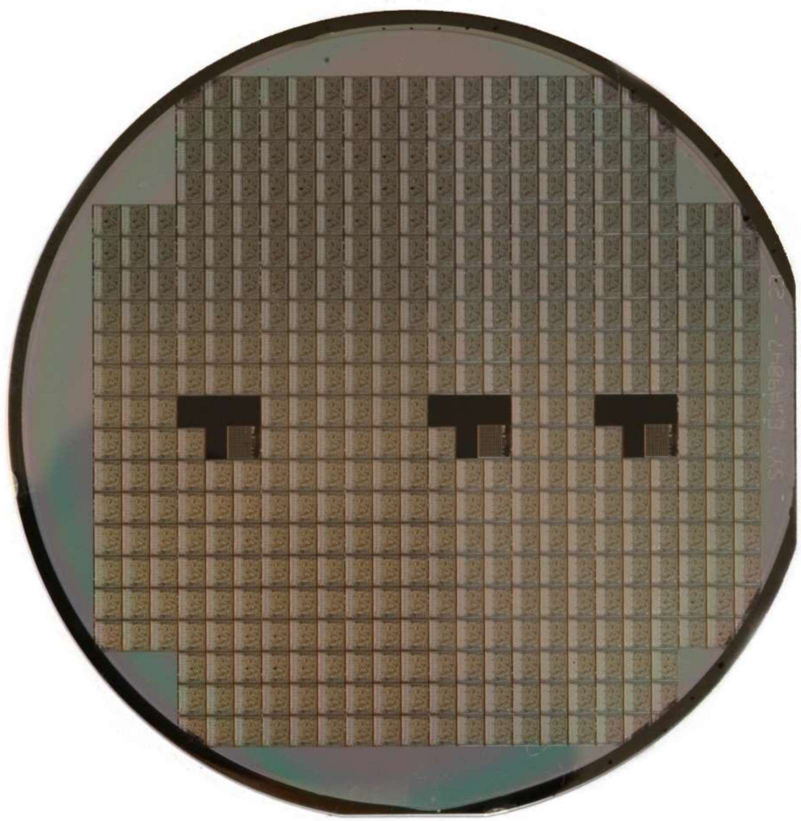


Float zone

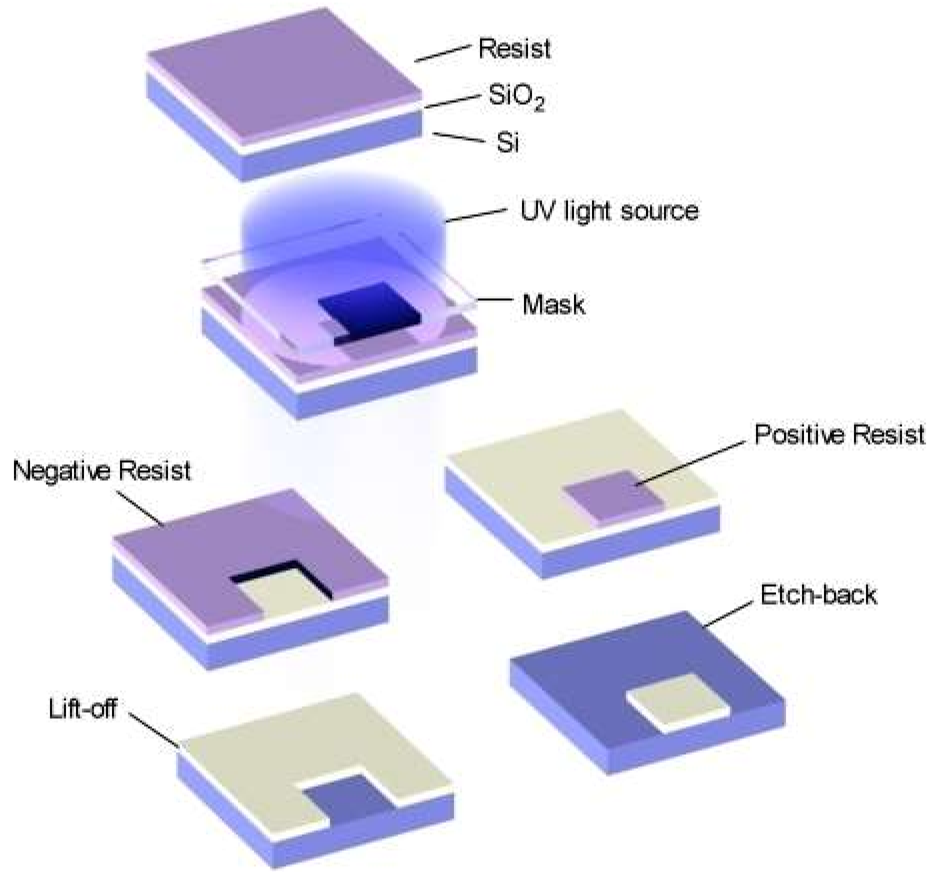
http://en.wikipedia.org/wiki/Czochralski_process

Silicon wafers

50 μm - 0.5 mm thick



Photolithography



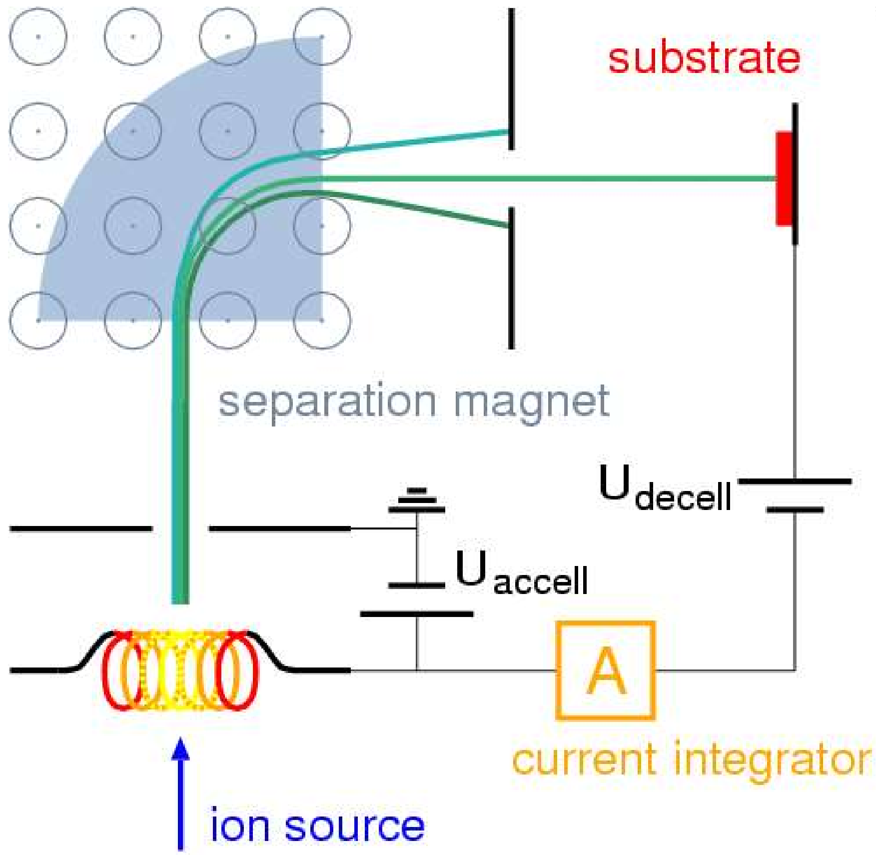
http://britneyspears.ac/physics/fabrication/photolithography.htm

http://cleanroom.byu.edu/lithography.parts/Lithography.html

EBPG (Electron beam pattern generator)

100 kV $\rightarrow \lambda = 0.12$ nm

Ion implantation



Implant at 7º to avoid channeling

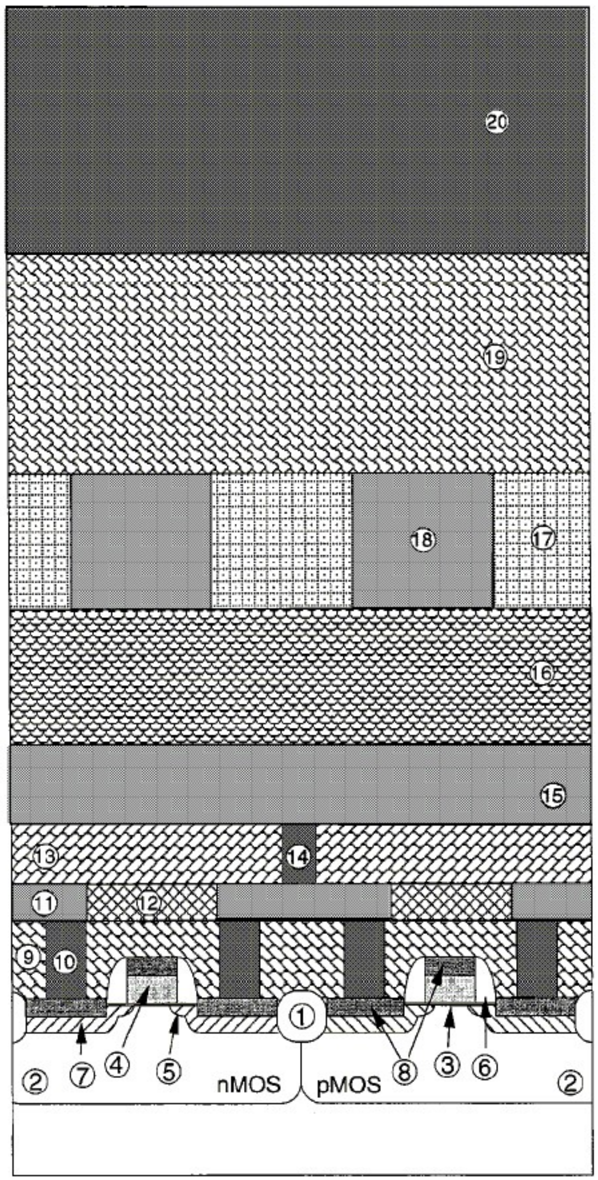
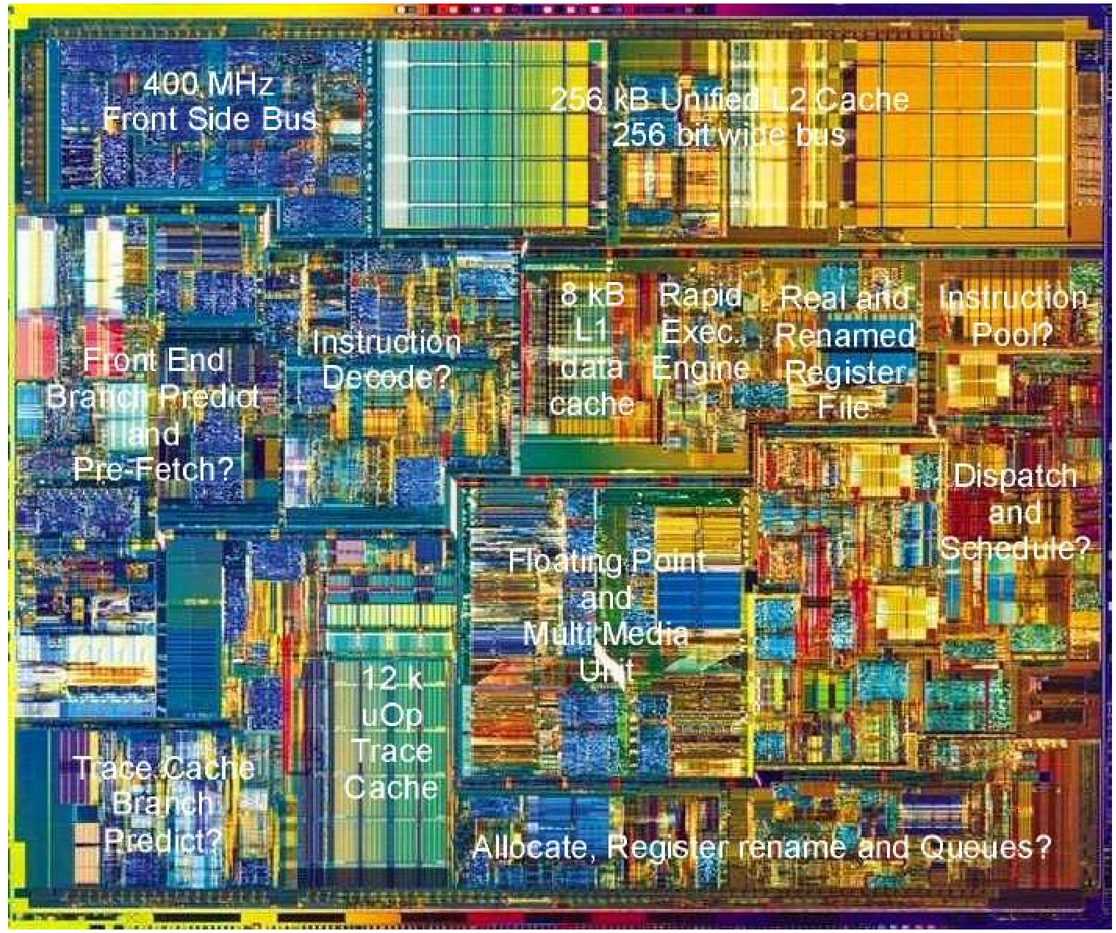
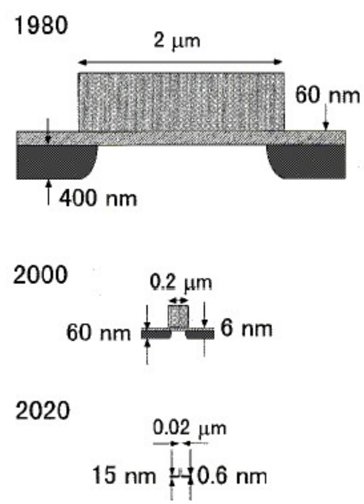


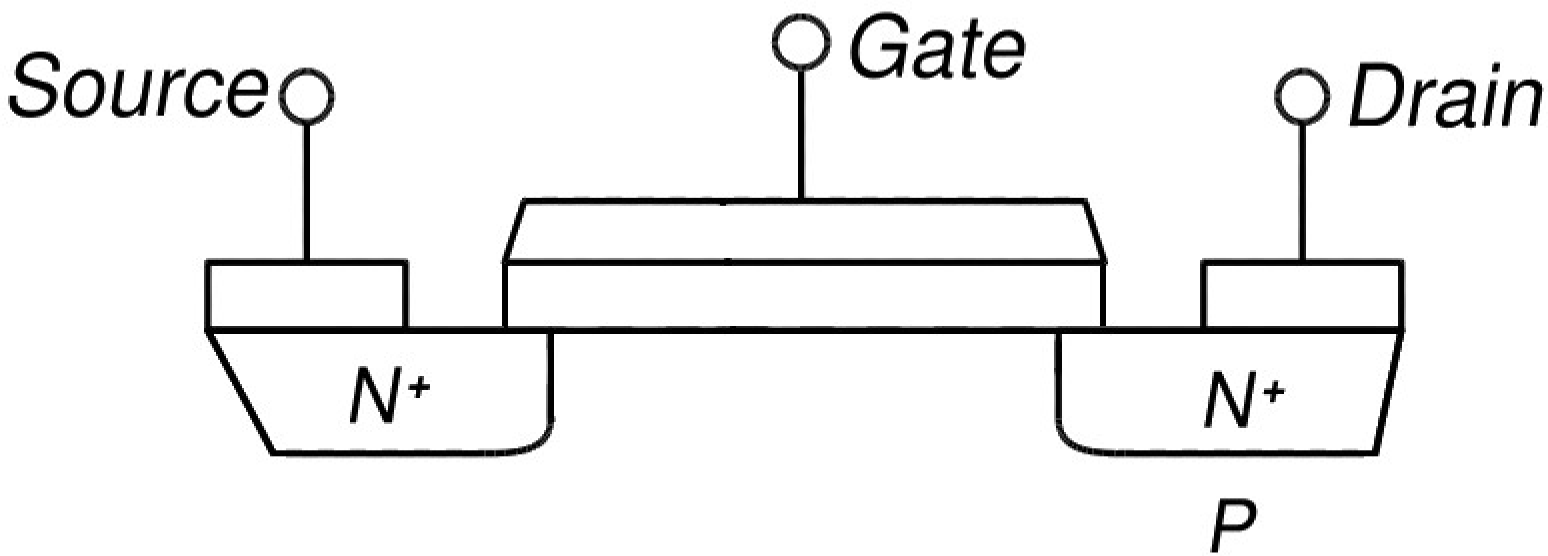
Fig. 2 Schematic cross section of present CMOS FETs with multilayered wiring.





MOSFET

Metal Oxide Semiconductor Field Effect Transistor

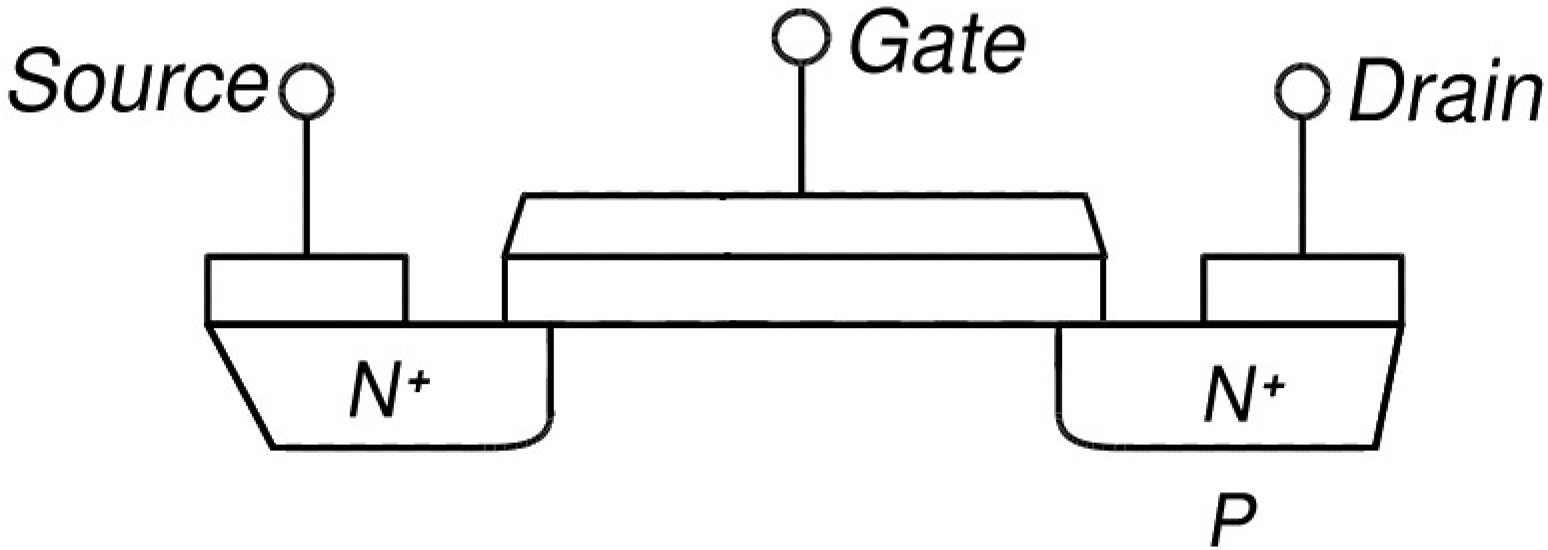


functions as a switch

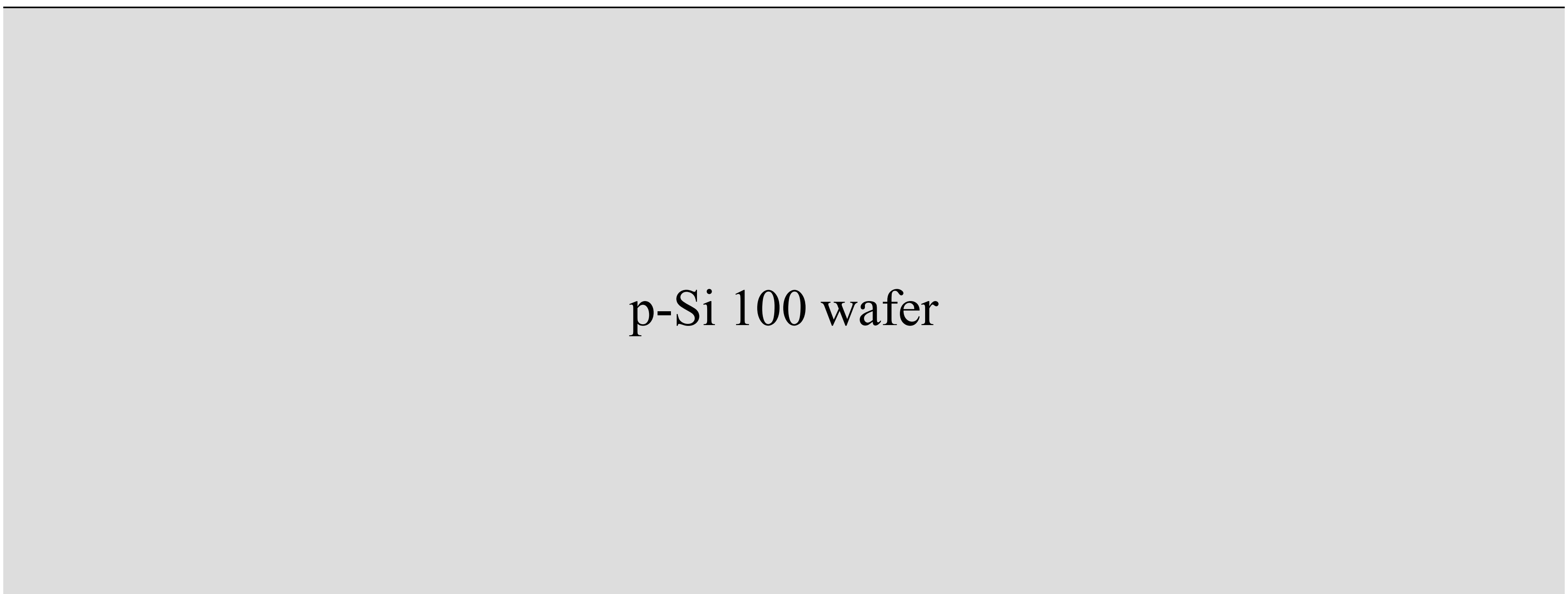
~ 1 billion /chip

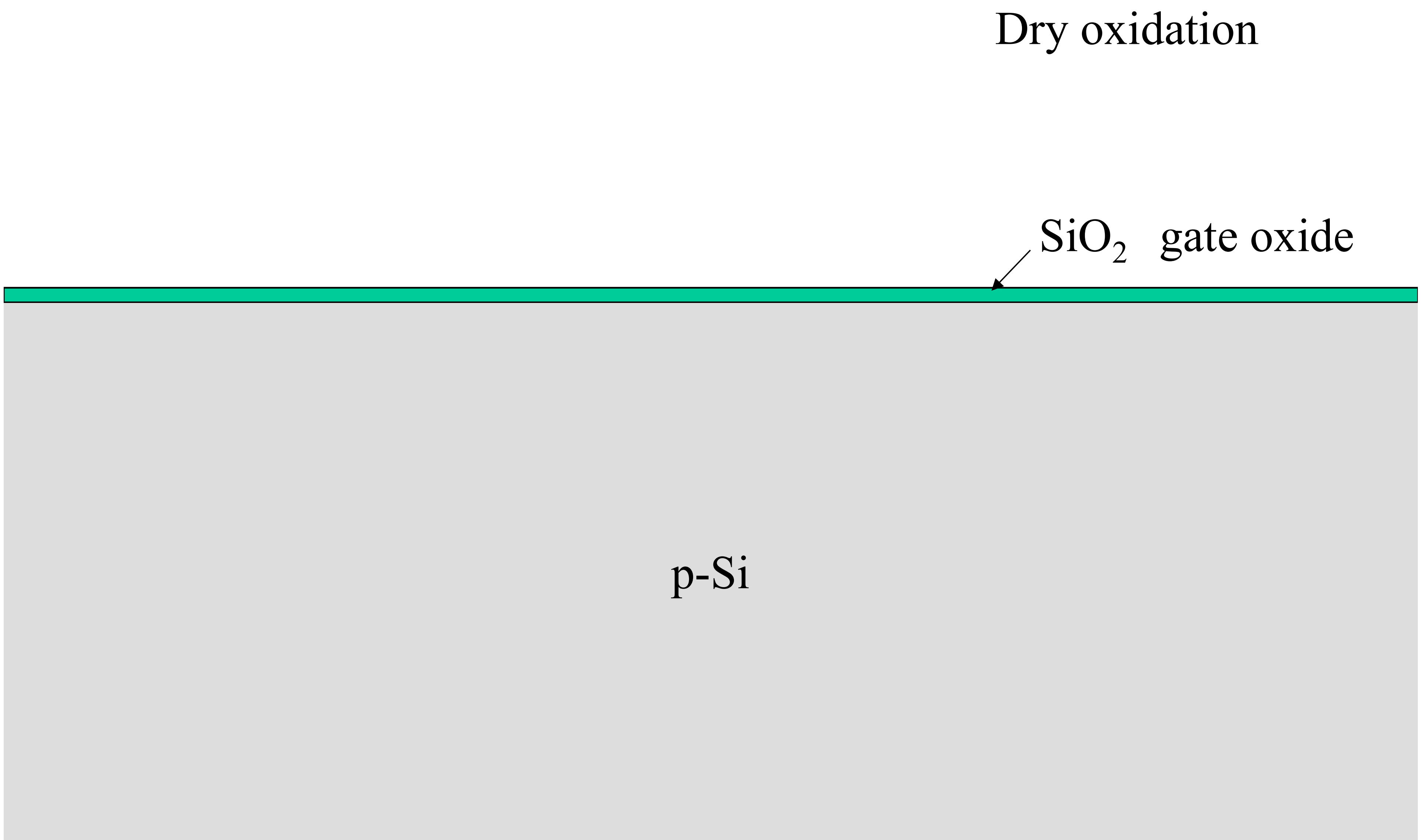
http://en.wikipedia.org/wiki/Image:Mosfet_linear.svg

Self-aligned gate

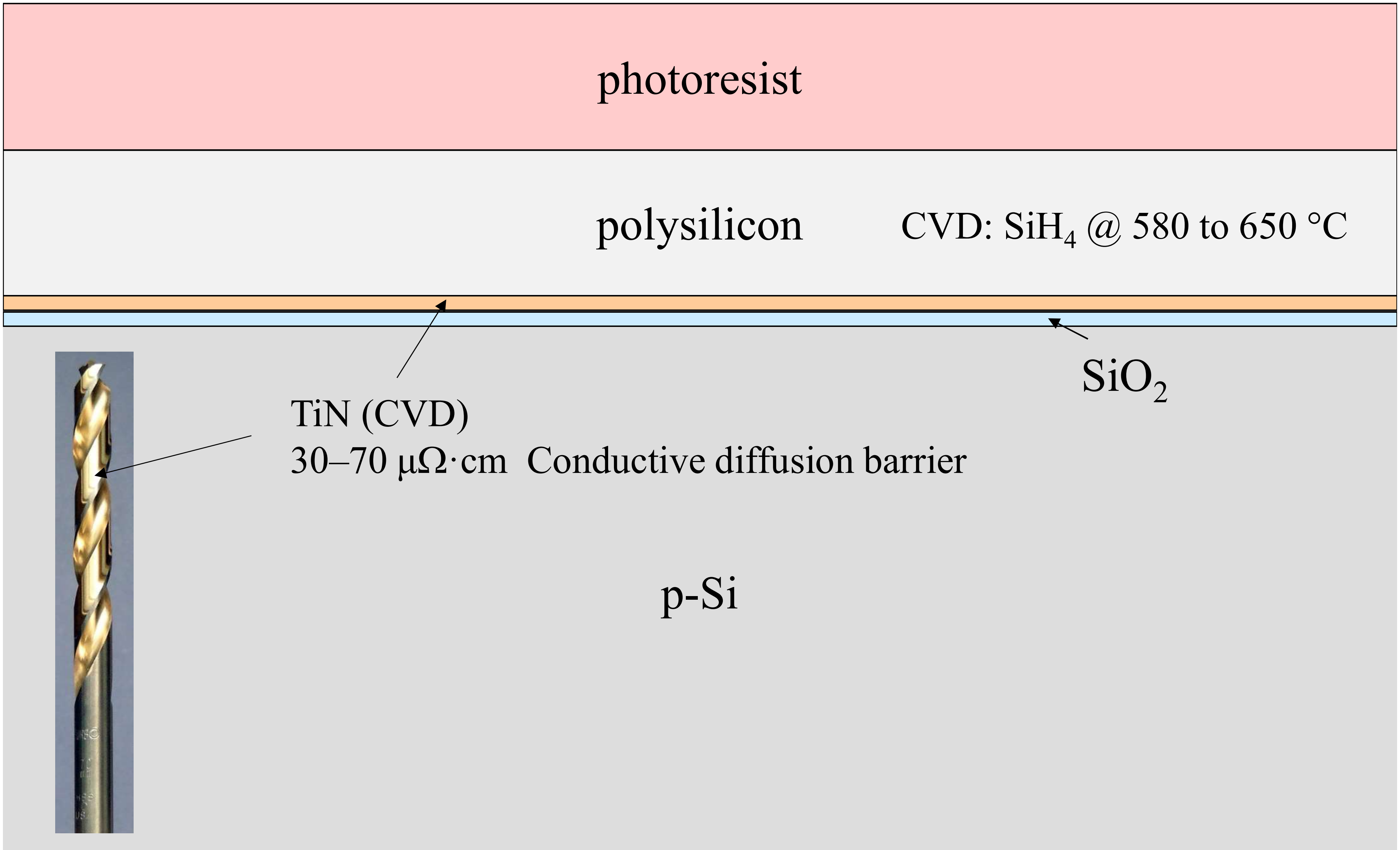


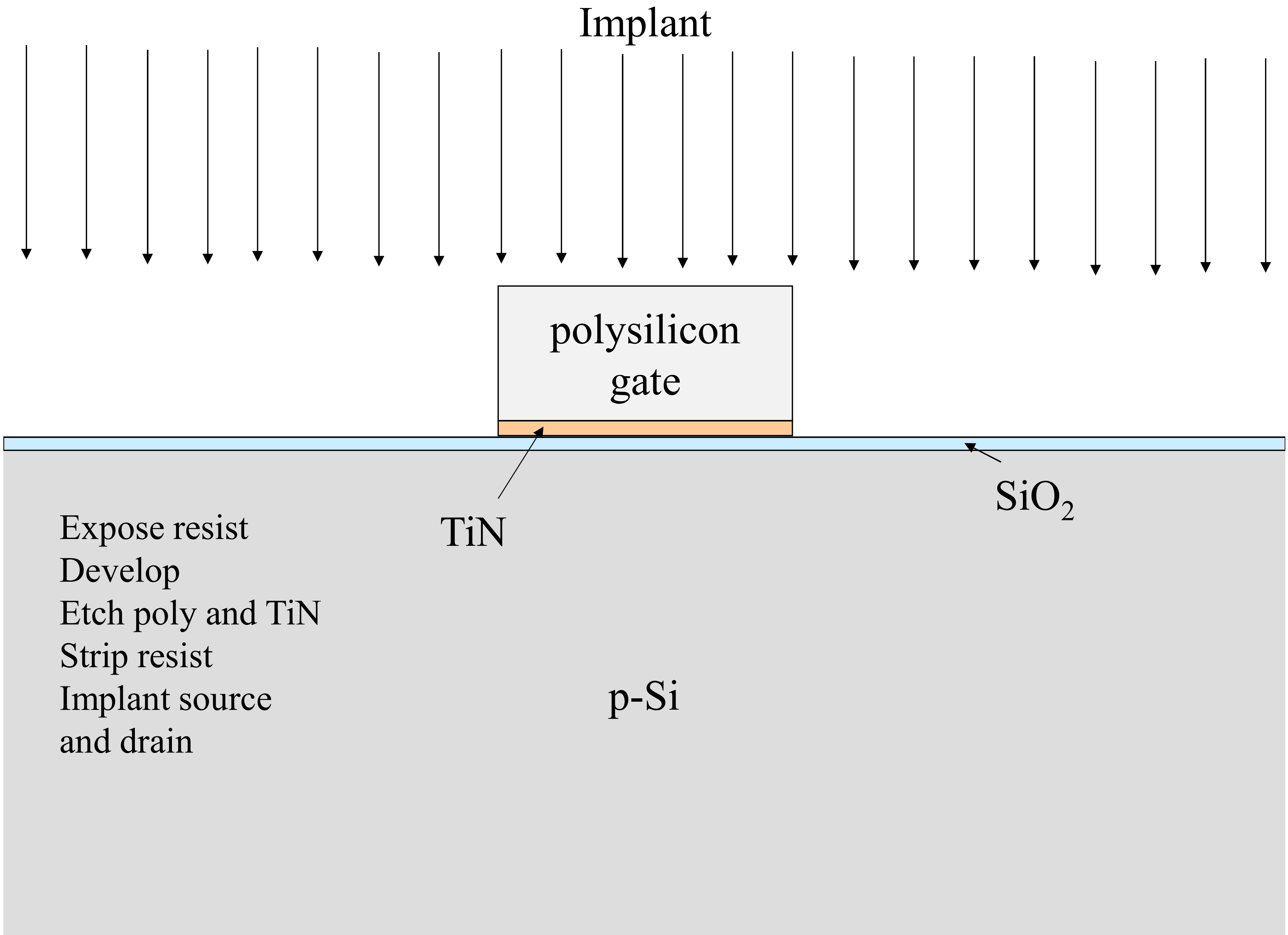
Self-aligned fabrication



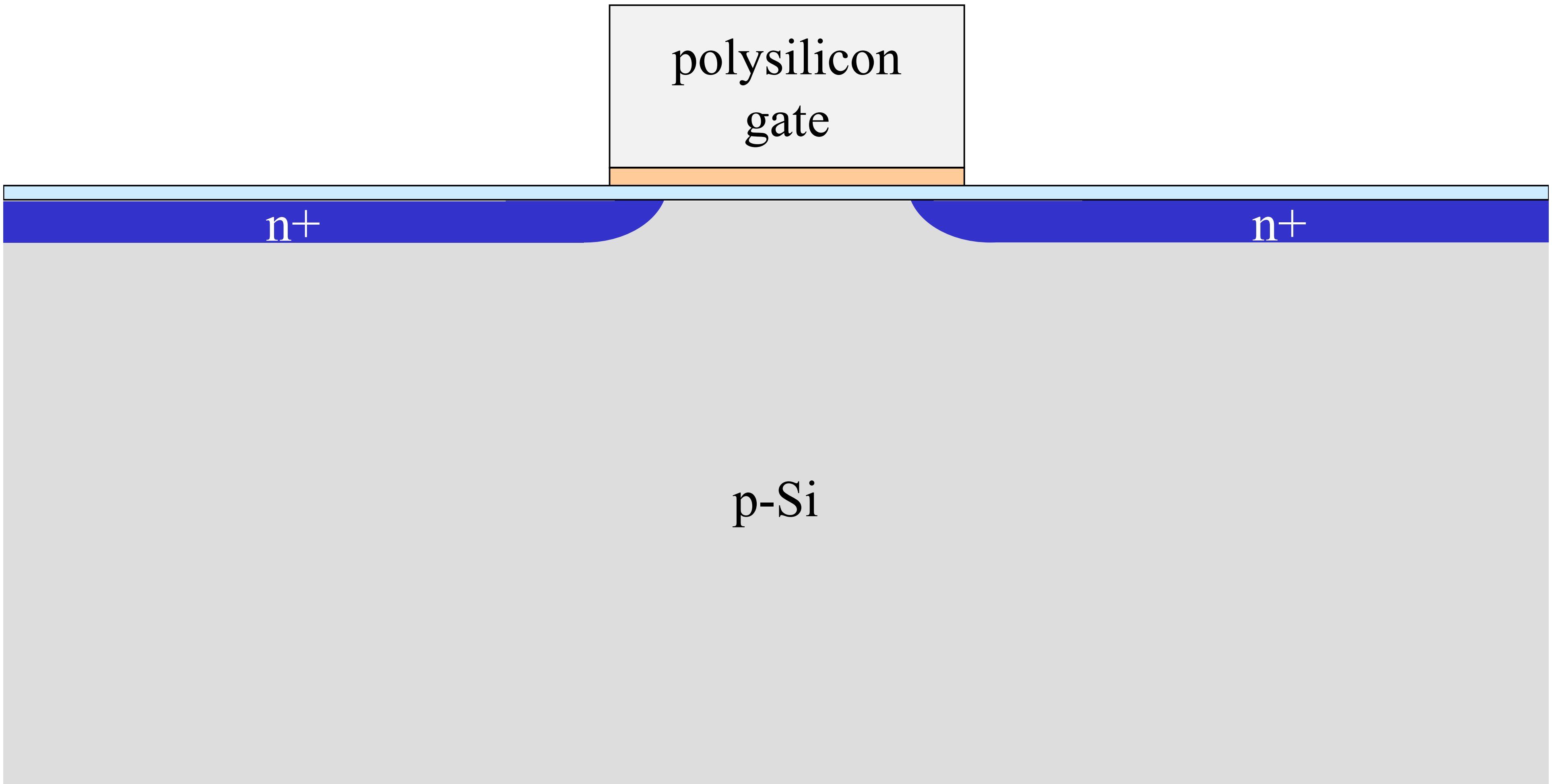


Dry oxidation
SiO2 gate oxide
p-Si


photoresist
polysilicon
CVD: SiH_4 @ 580 to 650 °C
SiO_2
TiN (CVD)
30–70 μΩ·cm Conductive diffusion barrier
p-Si

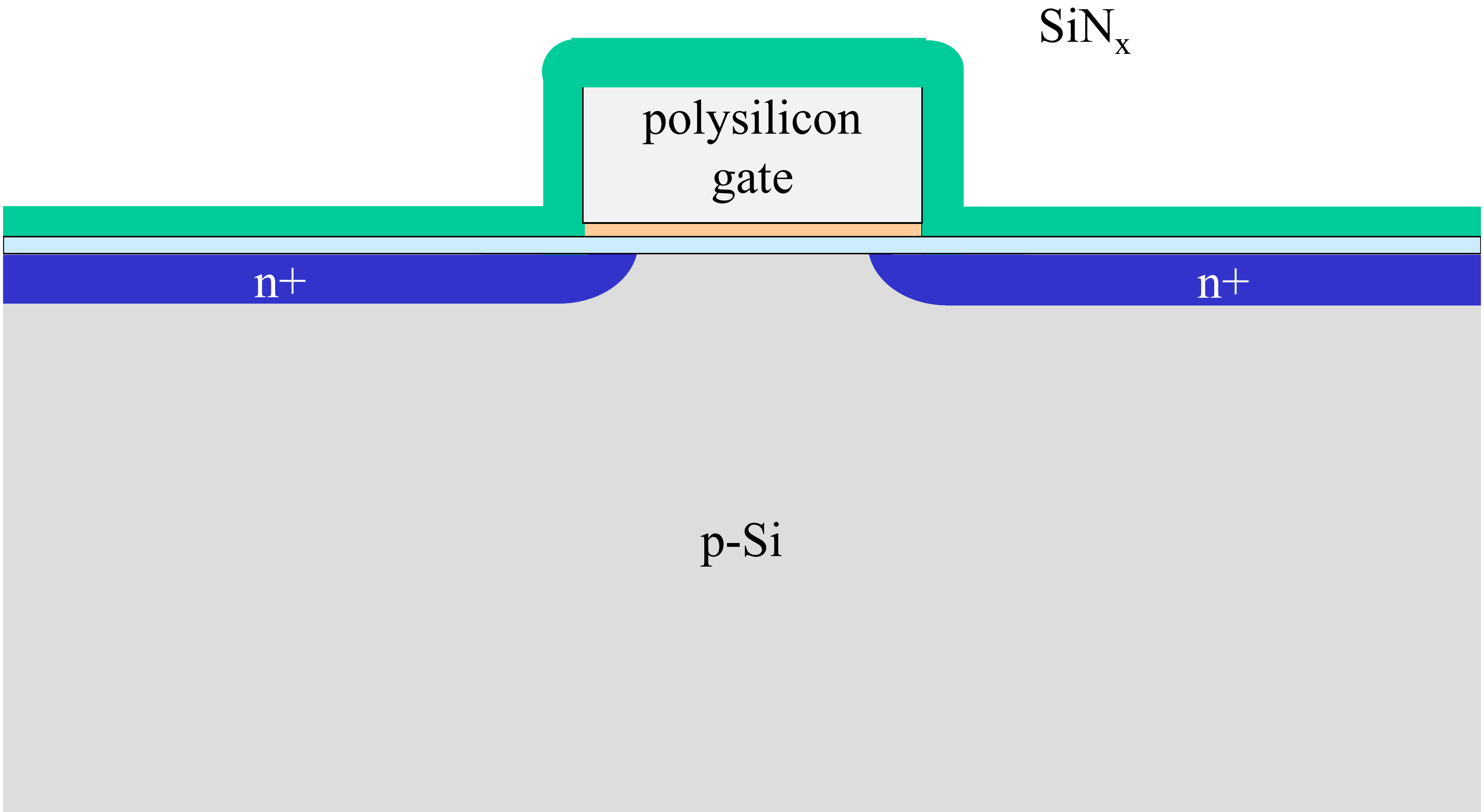

Implant
polysilicon gate
TiN
SiO2
Expose resist
Develop
Etch poly and TiN
Strip resist
Implant source
and drain
p-Si

Self-aligned fabrication



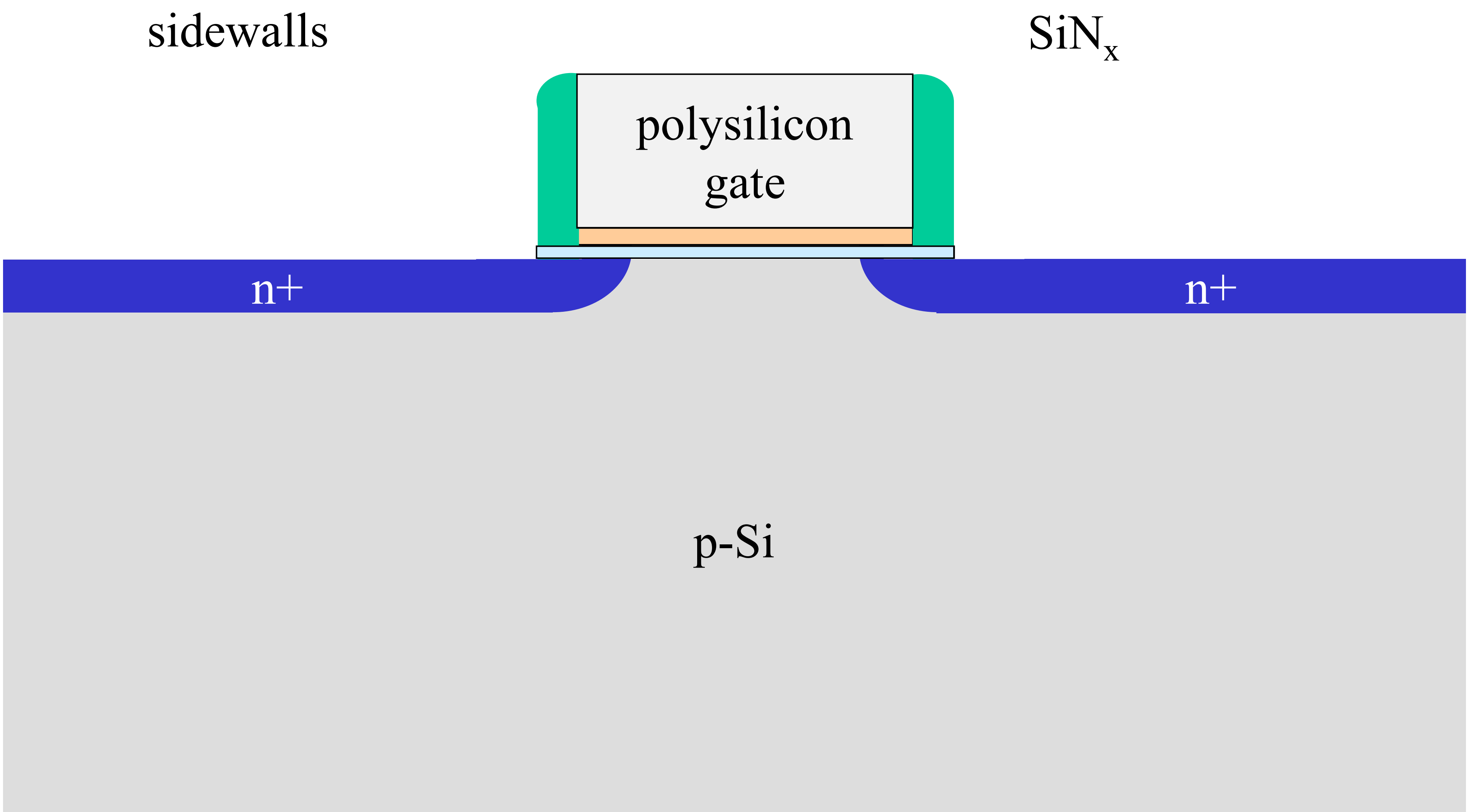
Spacer

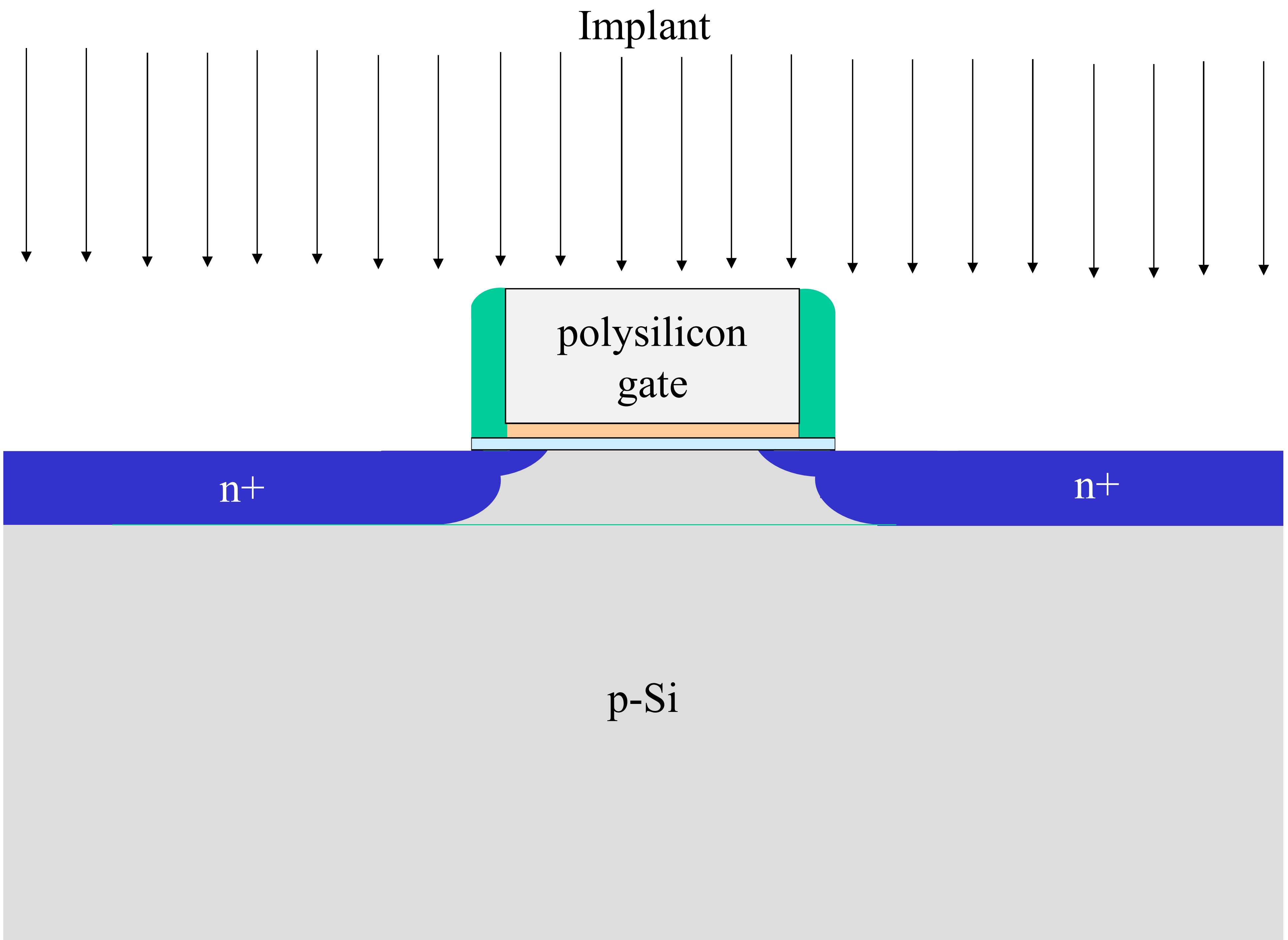
PECVD SiN_x



Spacer

Etch back to leave only sidewalls




Implant
polysilicon
gate
n+
n+
p-Si

Salicide (Self-aligned silicide)

Transition metal (Ti, Co,W) is deposited (CVD). During a high temperature step is reacts to a silicide ($TiSi_2$). Not silicide is formed on nitride or oxide.