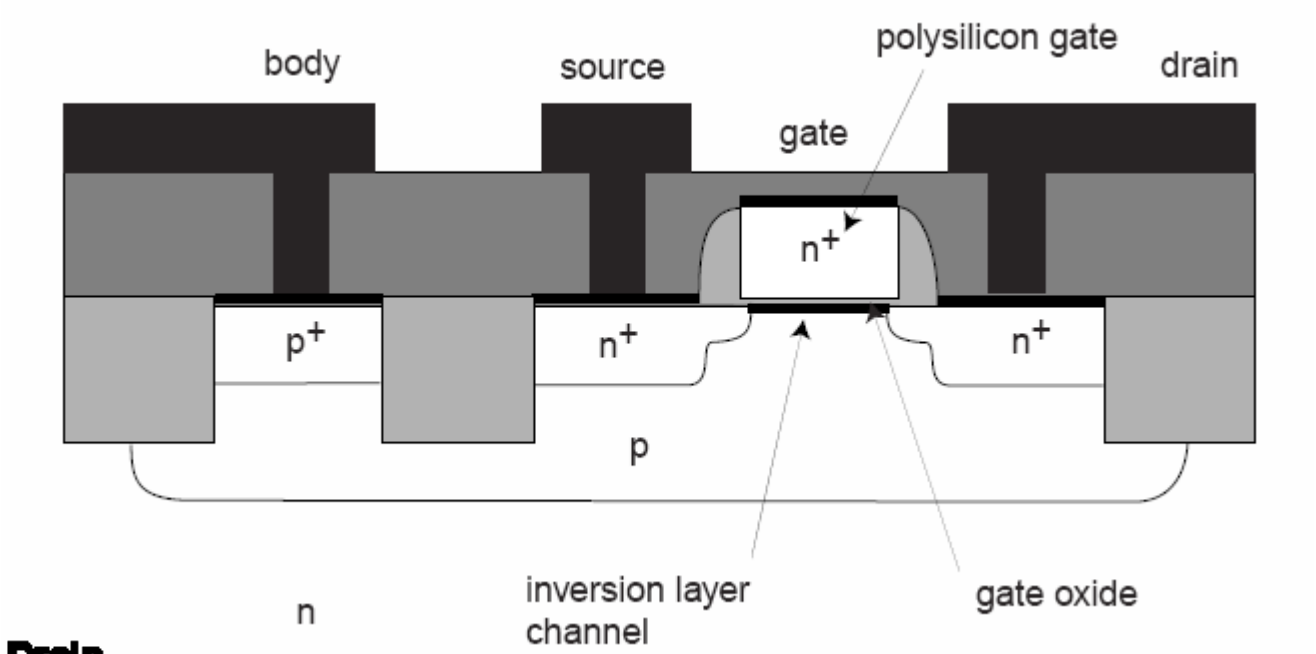
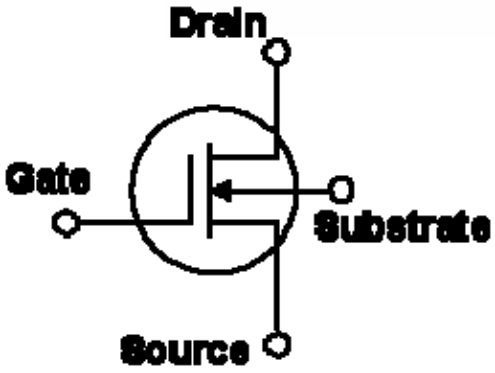
MOSFETs

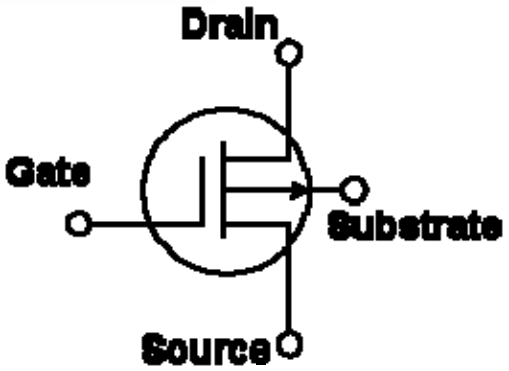
MOSFETs





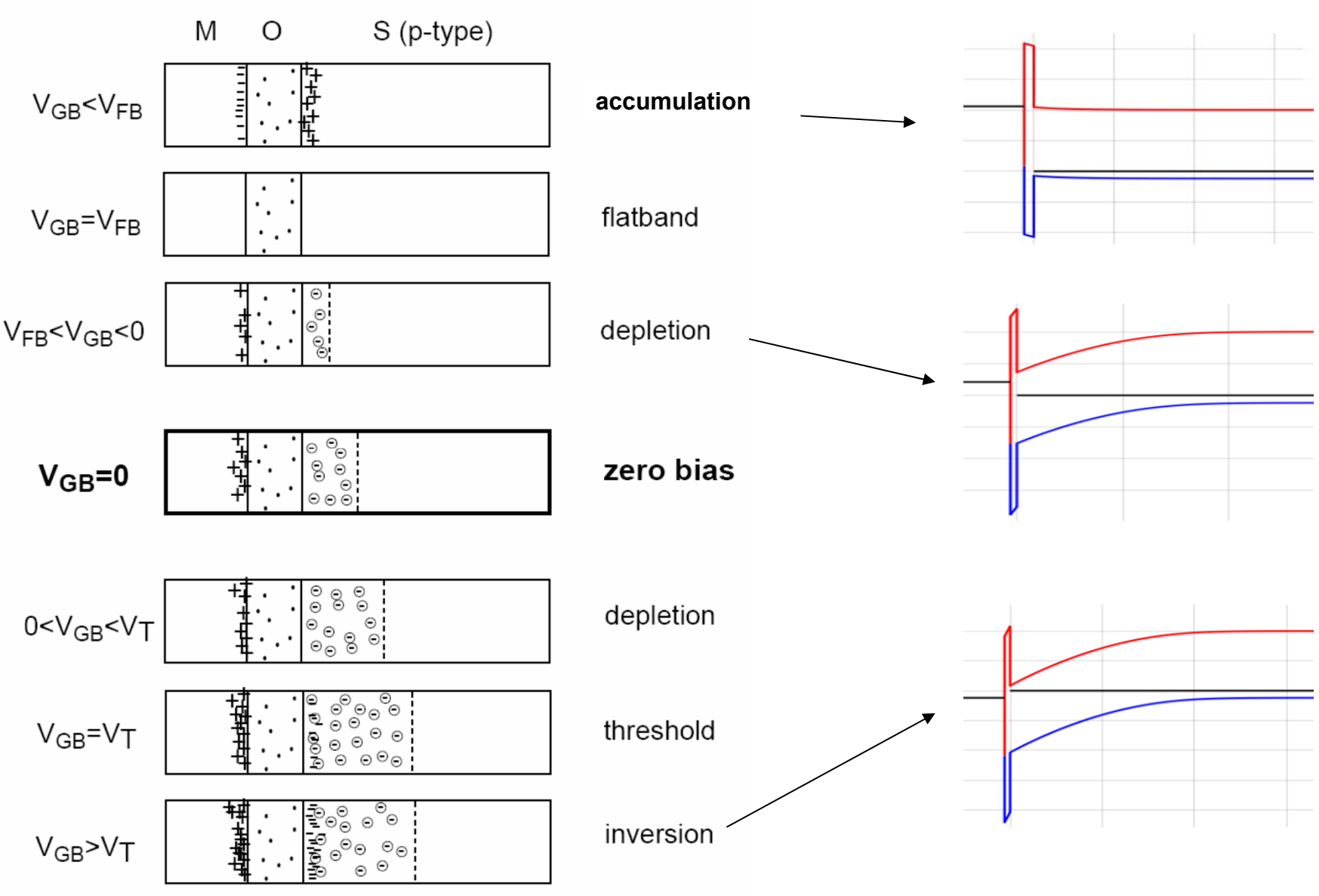
n - channel

functions as a switch
~ 1 billion /chip



p - channel

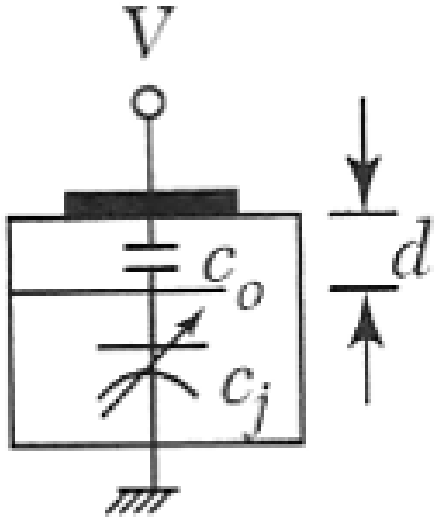
MOS capacitor

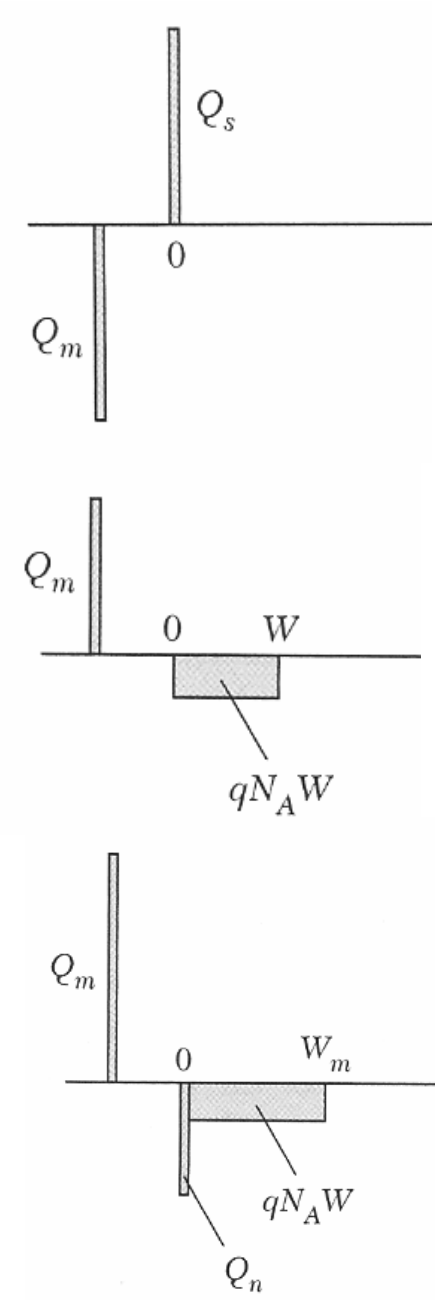


MOS capacitance

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \qquad C_j = \frac{\varepsilon}{x_p}$$

$$C = \left(\frac{1}{C_{ox}} + \frac{1}{C_j} \right)^{-1}$$





MOS Capacitor - Capacitance voltage

In capacitance-voltage profiling, the capacitance of a MOS capacitor is measured as a function of the bias voltage. The app below solves the Poisson equation to determine the charge-voltage and capacitance voltage characteristics of a MOS capacitor with a p-type substrate. This is the low-frequency result. At high frequencies, the charge at the oxide interface does not change fast enough and the characteristics take on another form.

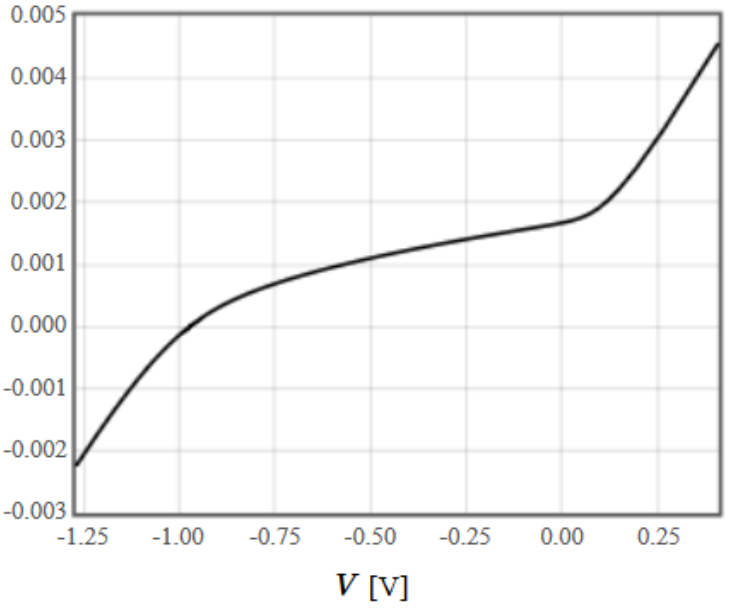
ϕ_m = 4.08 eV χ_s = 4.05 eV

t_{ox} = 3 nm ϵ_{ox} = 4 $N_c(300)$ = 2.78E19 1/cm³ T = 300 K

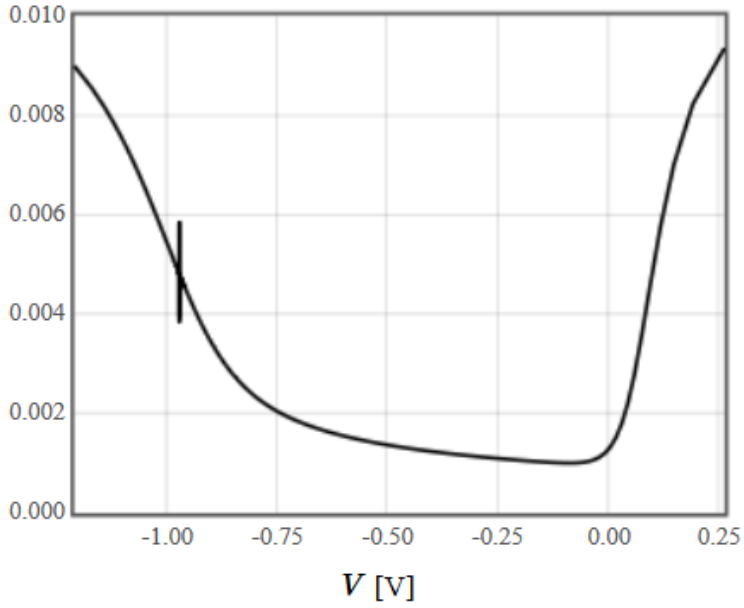
E_g = 1.166-4.73E-4*T*T/(T+636) eV ϵ_{semi} = 12 $N_v(300)$ = 9.84E18 1/cm³ N_A = 1E17 1/cm³

Submit Si Ge GaAs

Q - V



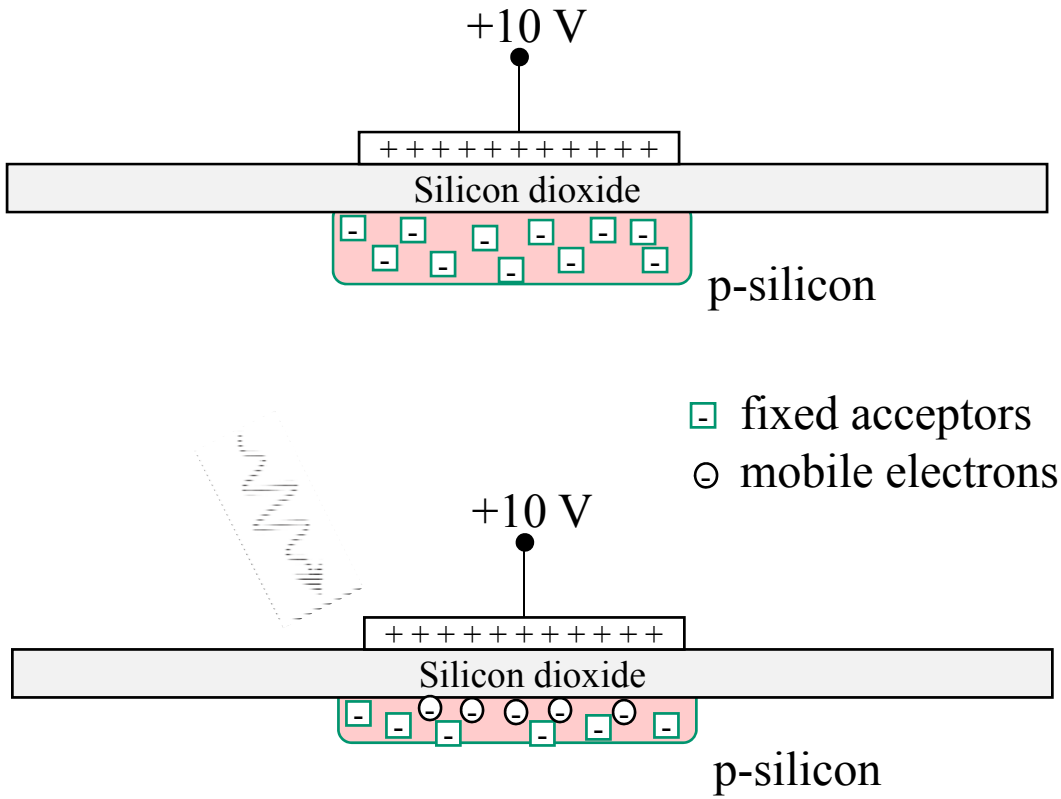
C - V

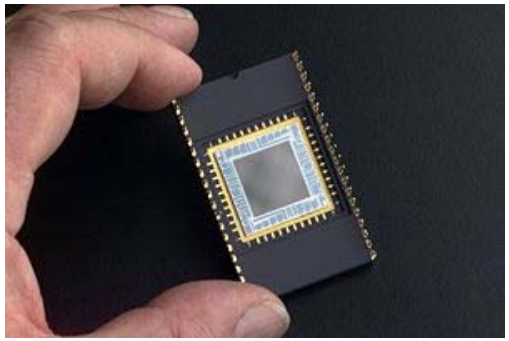


$E_g = 1.12$ eV $n_i = 6.40e+9$ 1/cm³ $\phi_s = 5.05$ eV $V_{fb} = \phi_m - \phi_s = -0.972$ V

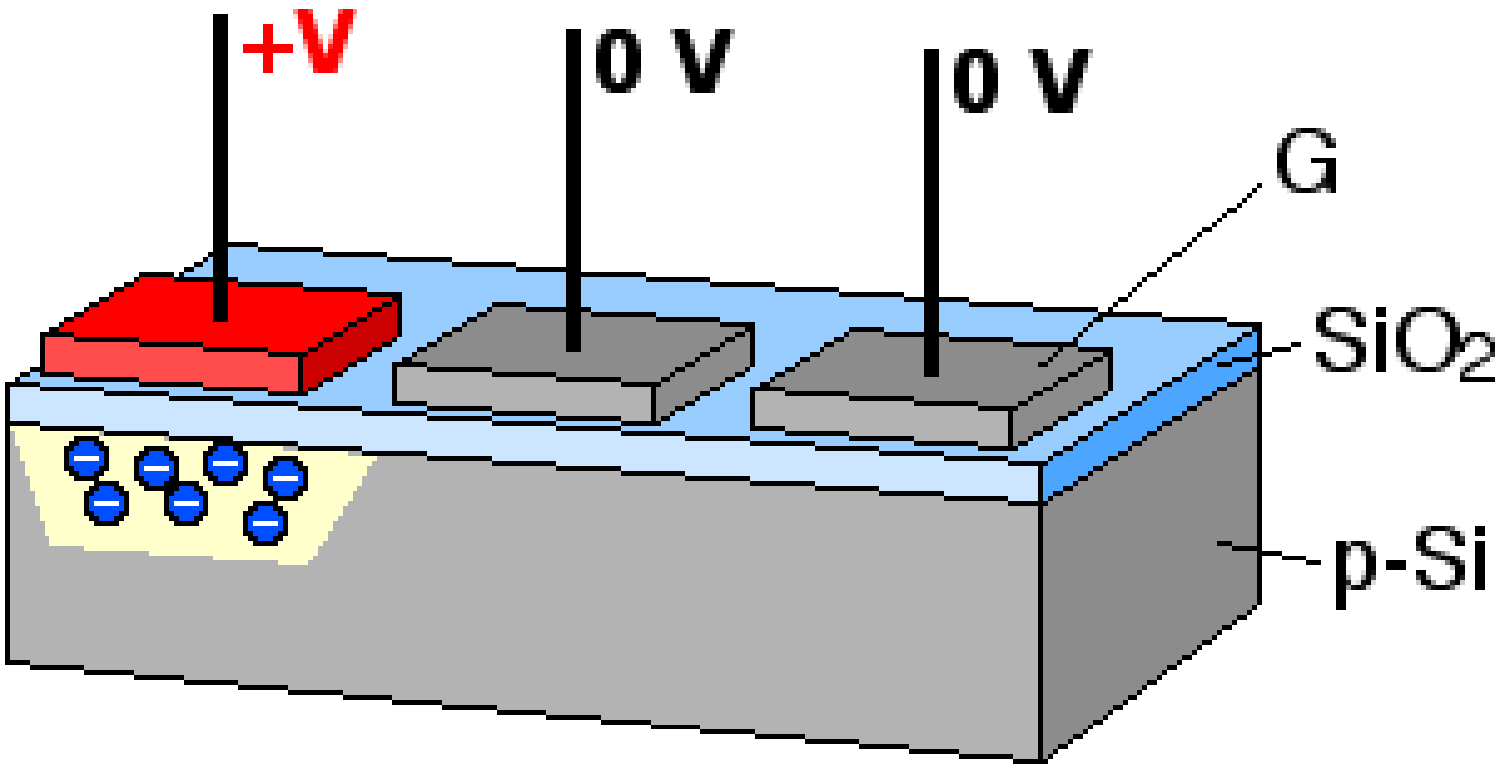
$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = 0.0118$ F/m² $V_T = 0.0292$ V

CCD devices


+10 V
+ + + + + + + + + + +
Silicon dioxide
p-silicon
fixed acceptors
mobile electrons
+10 V
+ + + + + + + + + + +
Silicon dioxide
p-silicon

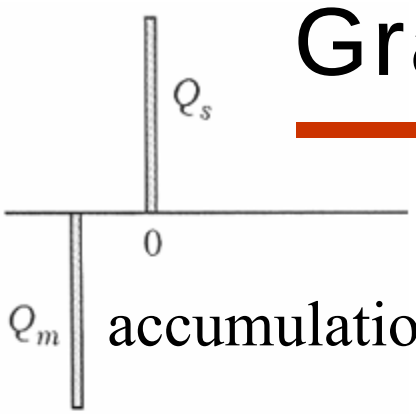


CCD devices

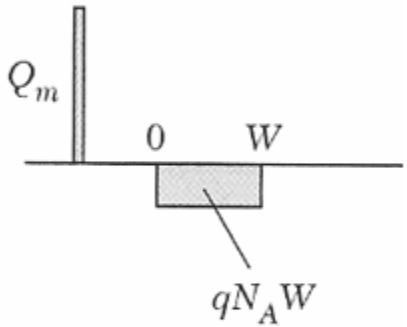


https://en.wikipedia.org/wiki/Charge-coupled_device#/media/File:CCD_charge_transfer_animation.gif

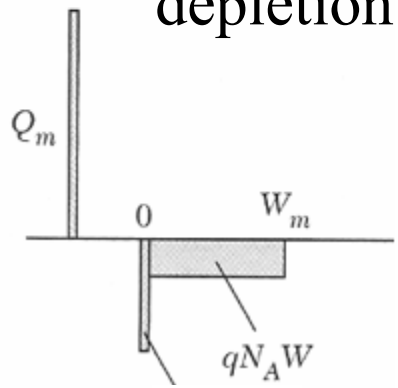
Gradual channel approximation



accumulation



depletion



inversion

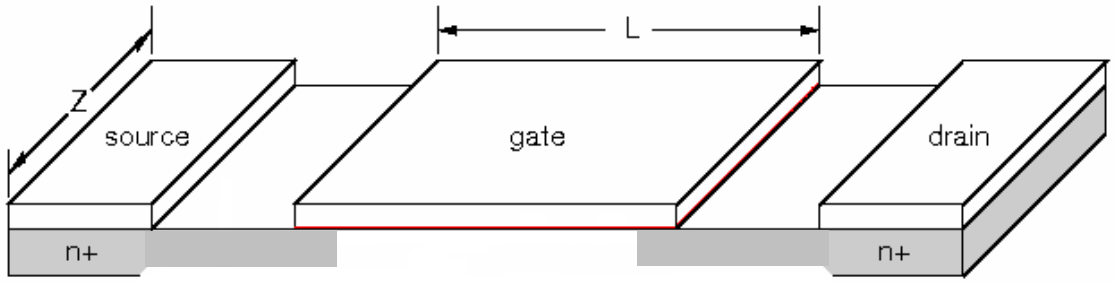
$$Q_{\text{mobile}} = \begin{cases} 0, & \text{for } V_G - V_B < V_T \\ -C_{\text{ox}}(V_G - V_B - V_T) & \text{for } V_G - V_B > V_T \end{cases}$$

http://lampx.tugraz.at/~hadley/psd/L10/gradualchannelapprox.php

Gradual channel approximation

Ohm's law $\longrightarrow$ $j = -nev_d = ne\mu_n E_y$

$$I = Ztj = Ztne\mu_n E_y = Ze\mu_n n_s E_y$$



$n_s = nt$ is the sheet charge at the interface.

$$n_s(y) = \frac{Q}{e} = \frac{-C_{ox}\left(V_G - V_{ch}(y) - V_T\right)}{e}$$

Gradual channel approximation

$$n_s(y) = -\frac{Q(y)}{e} = \frac{C_{ox}(V_G - V_{ch}(y) - V_T)}{e}$$

$$I = Ztj = Ze\mu_n n_s E_y$$

$$I_D = -Z\mu_n C_{ox}(V_G - V_{ch}(y) - V_T)\frac{dV_{ch}}{dy}$$

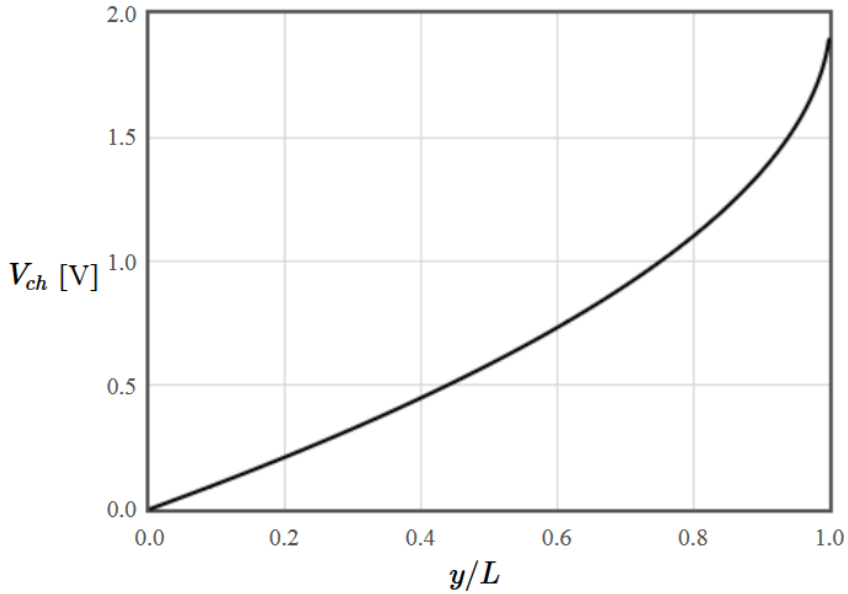
differential equation for V_{ch}

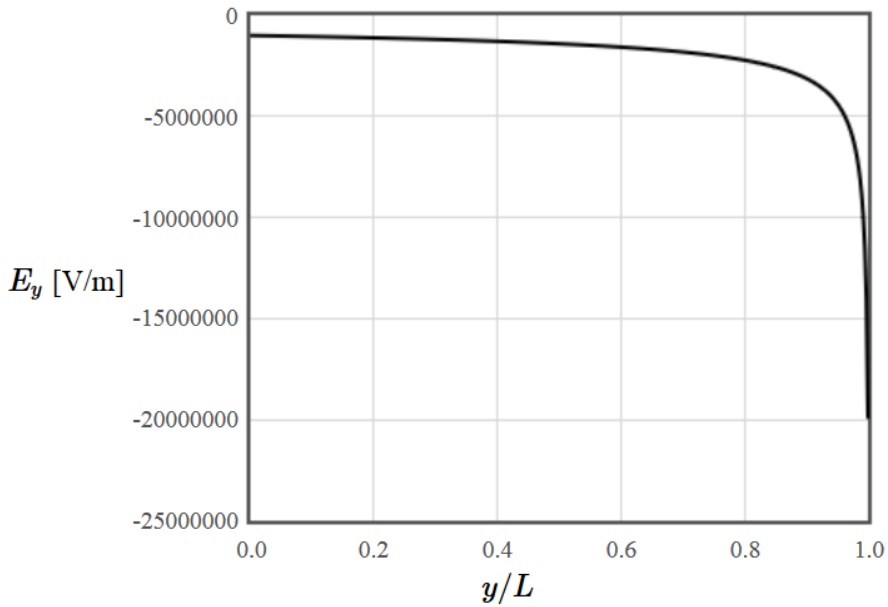
http://lampx.tugraz.at/~hadley/psd/L10/gradualchannelapprox.php

Gradual channel approximation

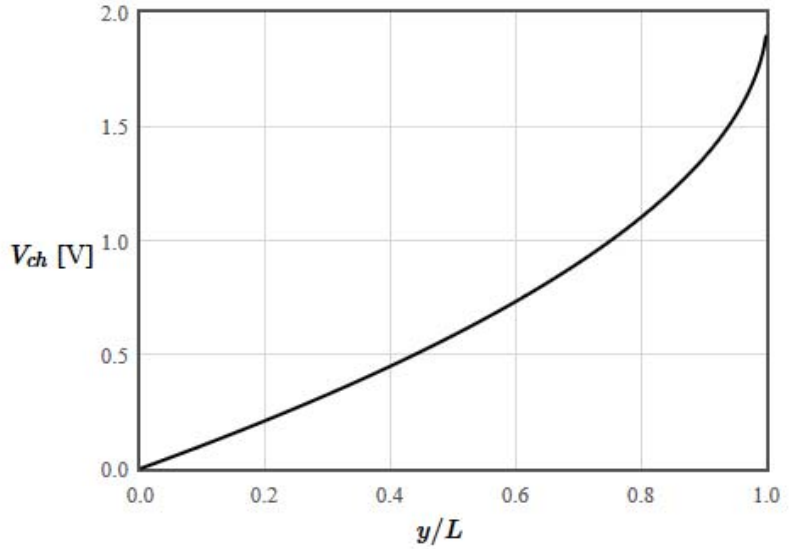
$$V_{ch}(y) = V_G - V_T - \sqrt{(V_G - V_T)^2 - \frac{2I_D y}{Z\mu_n C_{ox}}}$$

$$E_y = -\frac{dV_{ch}}{dy} = -\frac{I_D}{Z\mu_n C_{ox}\sqrt{(V_G - V_T)^2 - \frac{2I_D y}{Z\mu_n C_{ox}}}}$$



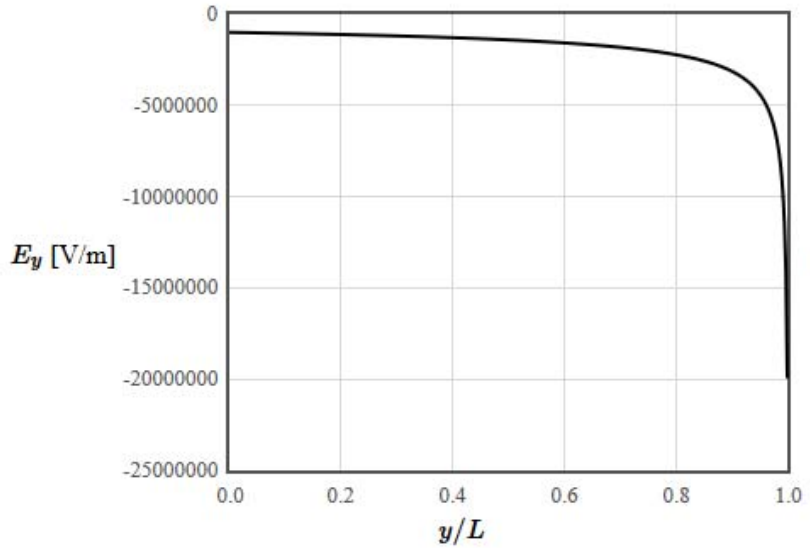


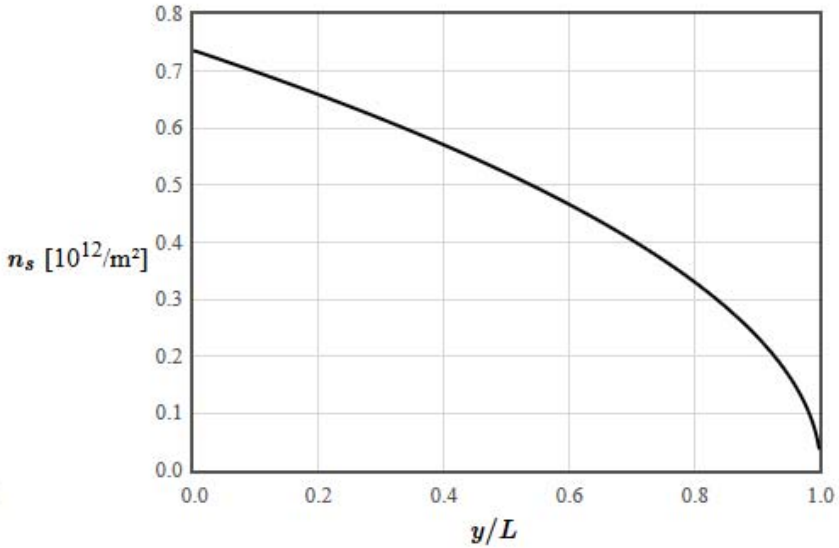
MOSFET Gradual Channel Approximation



$Z =$	1E-5	m
$L =$	1E-6	m
$\mu_n =$	1500	cm²/Vs
$\epsilon_r =$	4	
$t_{ox} =$	3E-9	m
$V_D =$	1.9	V
$V_G =$	3	V
$V_T =$	1	V

Replot





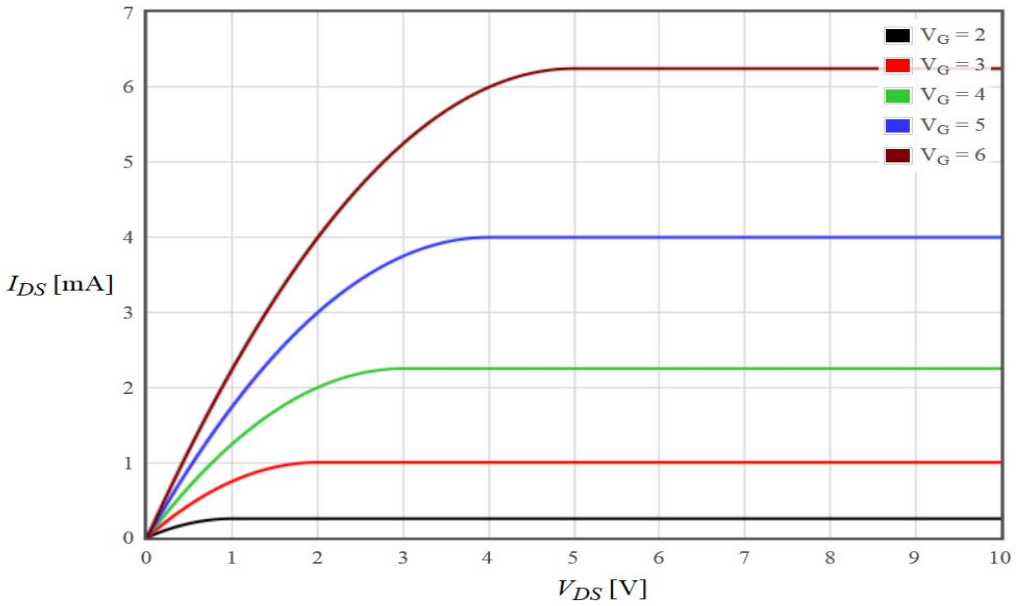
http://lampx.tugraz.at/~hadley/psd/L10/gradualchannelapprox.php

Gradual channel approximation

$$\int_0^L I_D \, \mathrm{d}y = \int_0^{V_D} Z \mu_n C_{ox} (V_G - V_B(y) - V_T) \, \mathrm{d}V$$

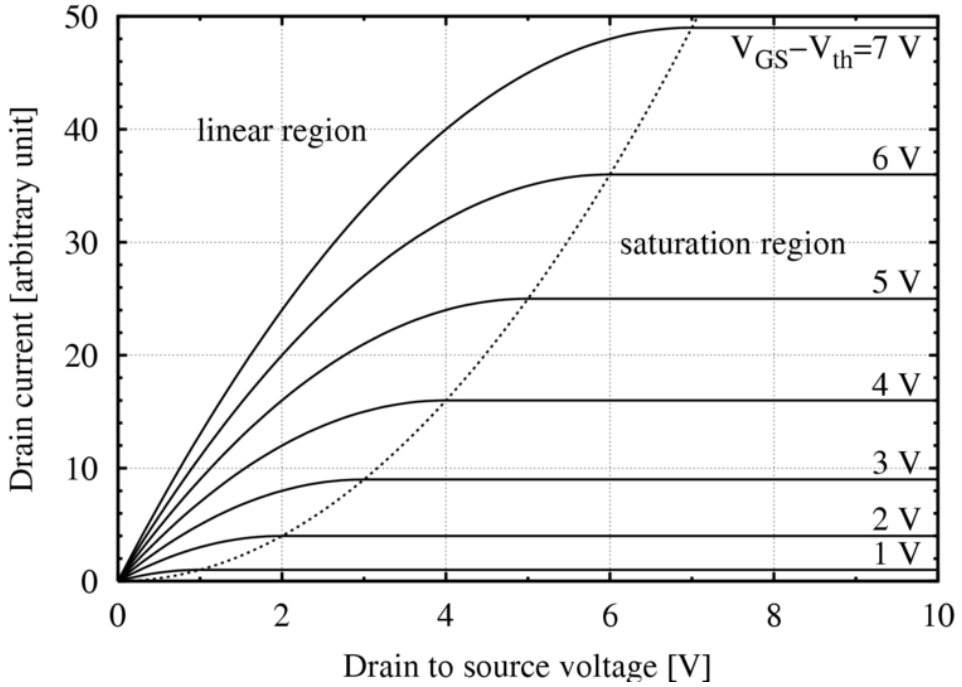
$$\boxed{I_D = \frac{Z}{L} \mu_n C_{ox} \left[(V_G - V_T) V_D - \frac{V_D^2}{2} \right]}$$

Valid in the linear regime (until pinch-off occurs at the drain).



MOSFET-saturation voltage

$$I = \frac{Z}{L}\mu_n C_{ox}\left[\left(V_G - V_T\right)V_D - \frac{V_D^2}{2}\right]$$



At pinch-off, $dI_{ds}/dV_{ds} = 0$

$$\frac{dI}{dV_D} = \frac{Z}{L}\mu_n C_{ox}\left[\left(V_G - V_T\right) - V_D\right] = 0 \qquad V_{sat} = \left(V_G - V_T\right)$$

A MOSFET in saturation is a voltage controlled current source.

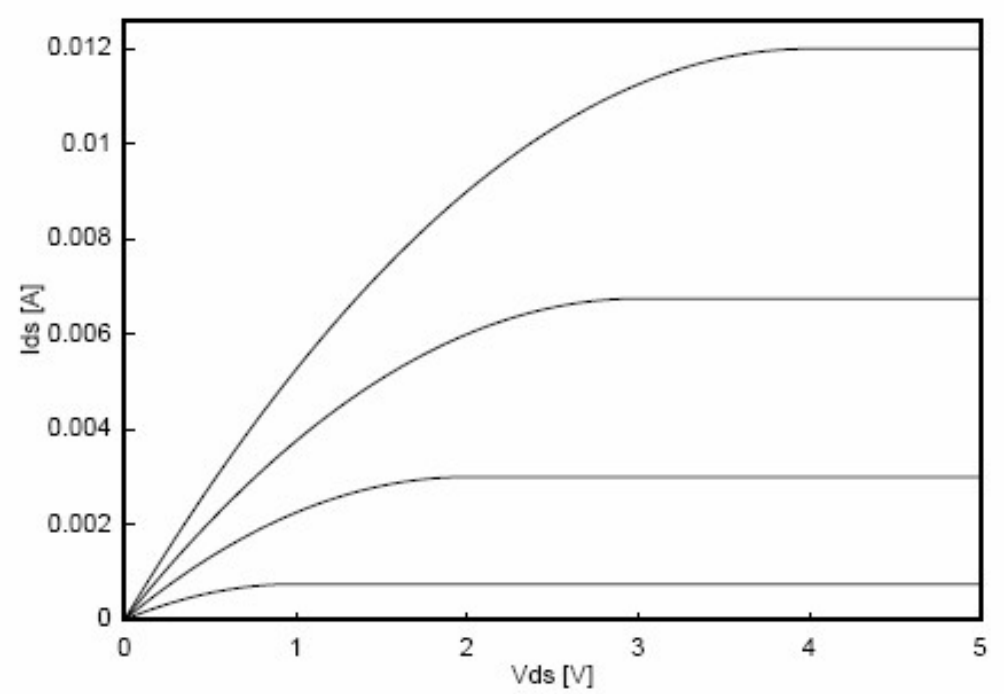
MOSFET - saturation current

Use the saturation voltage at pinch-off to determine the saturation current

$$V_{sat} = \left(V_G - V_T\right)$$

$$I = \frac{Z}{L}\mu_n C_{ox}\left[\left(V_G - V_T\right)V_D - \frac{V_D^2}{2}\right]$$

$$I_{sat} = \frac{Z}{2L}\mu_n C_{ox}\left(V_G - V_T\right)^2$$

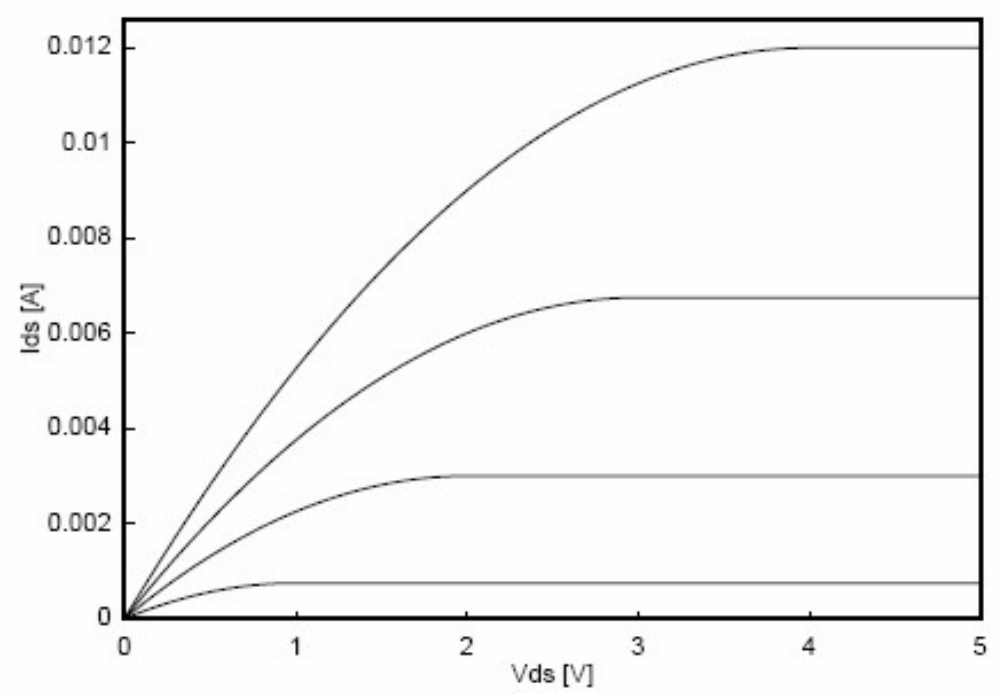


MOSFET (linear regime)

Channel conductance in the linear regime. For small V_D

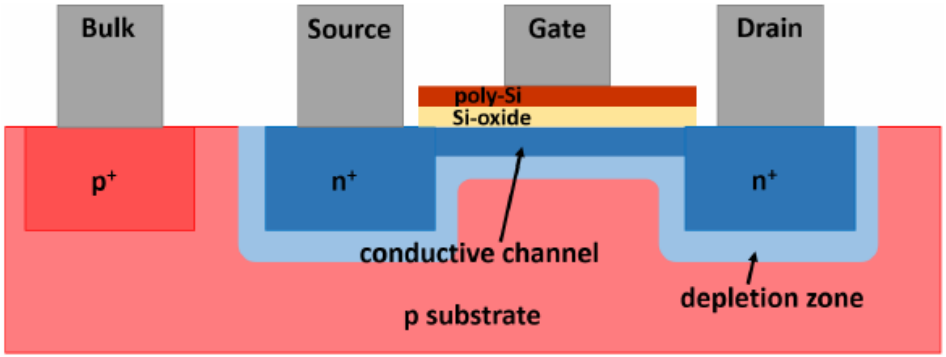
$$I \approx \frac{Z}{L}\mu_n C_{ox}\left[\left(V_G - V_T\right)V_D\right]$$

$$g_D = \frac{dI_D}{dV_D} = \frac{Z}{L}\mu_n C_{ox}\left(V_G - V_T\right)$$

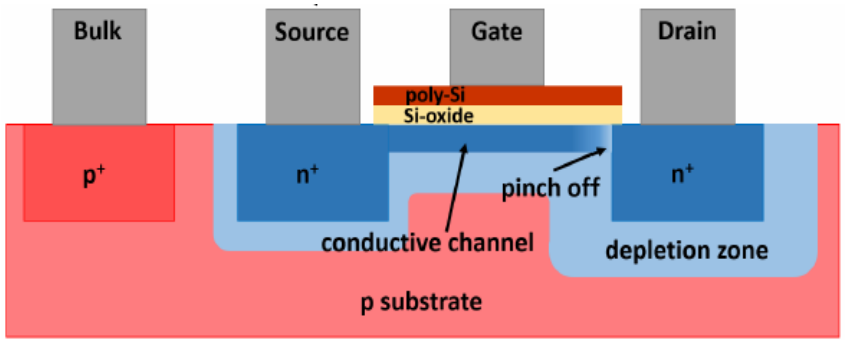


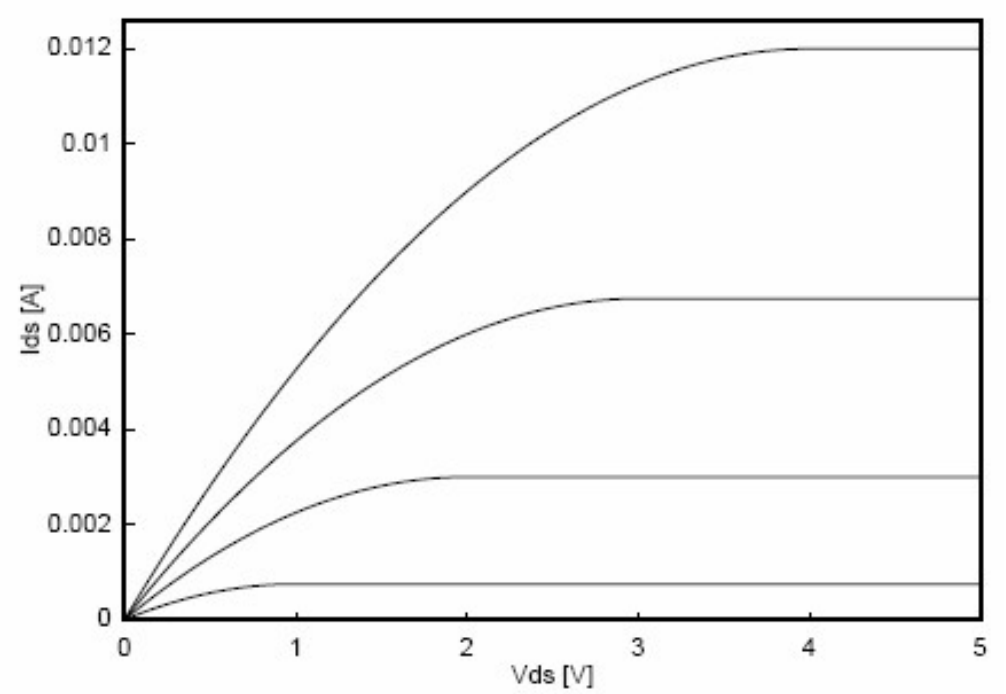
Transconductance

$$g_m = \frac{dI_D}{dV_G} = \frac{Z}{L}\mu_n C_{ox} V_D$$



MOSFET (saturation regime)





$$I_{sat} = \frac{Z}{2L}\mu_n C_{ox}\left(V_G - V_T\right)^2$$

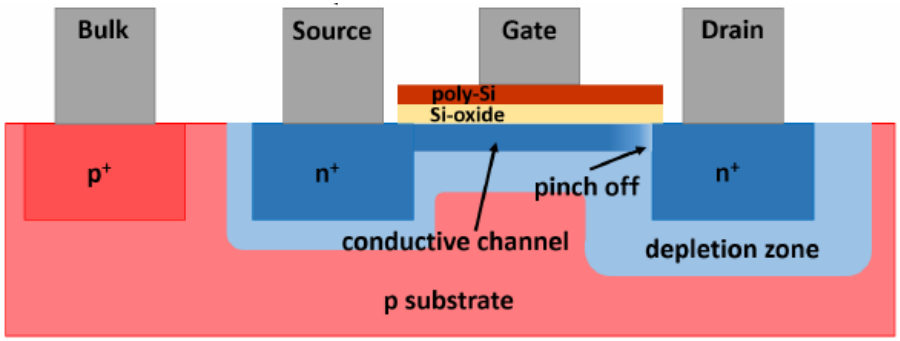
Transconductance

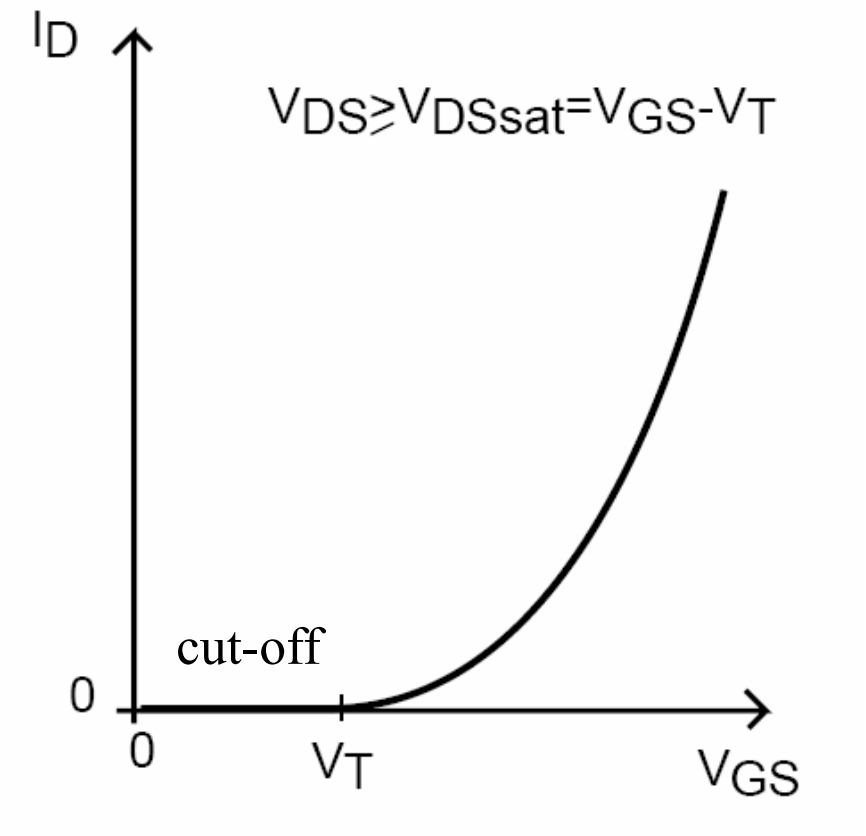
$$g_m = \frac{dI_D}{dV_G} = \frac{Z}{L}\mu_n C_{ox}\left(V_G - V_T\right)$$

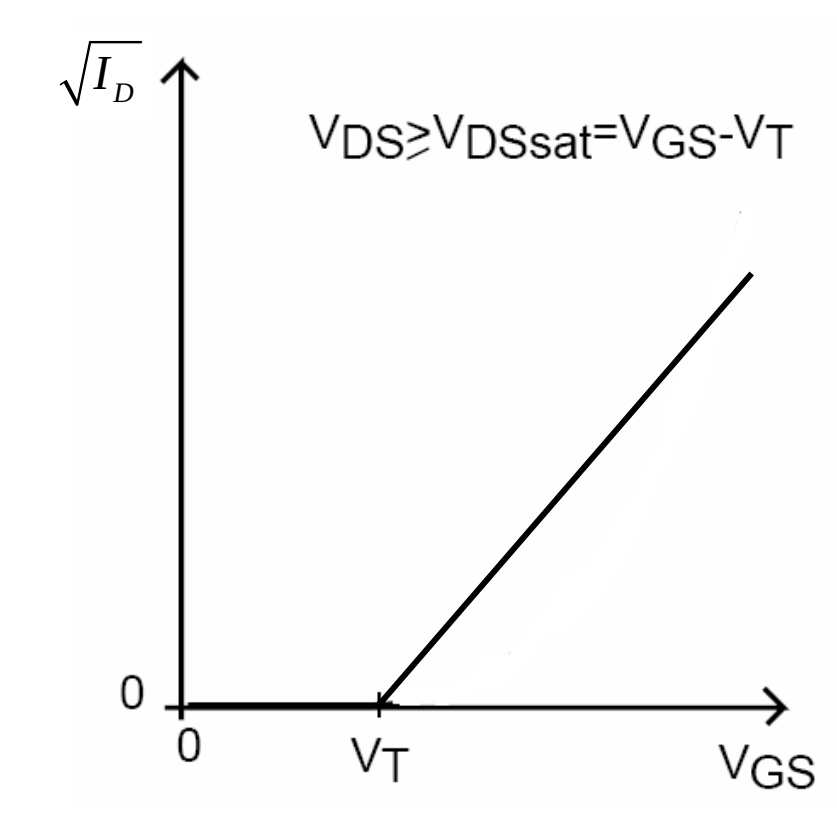
A MOSFET in the saturation regime acts like a voltage controlled current source.

MOSFET (saturation regime)

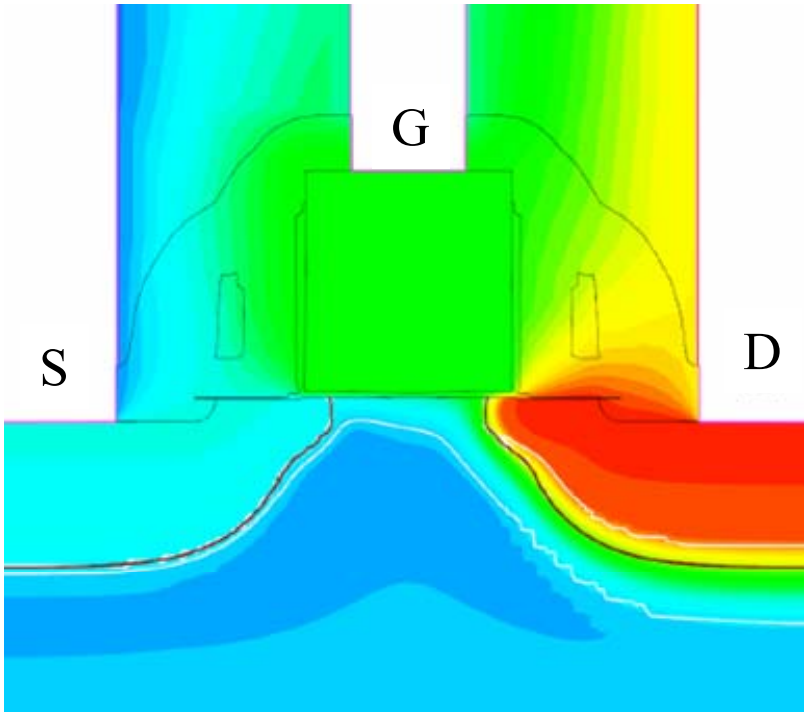
$$I_{sat} = \frac{Z}{2L}\mu_n C_{ox}\left(V_{GS} - V_T\right)^2$$



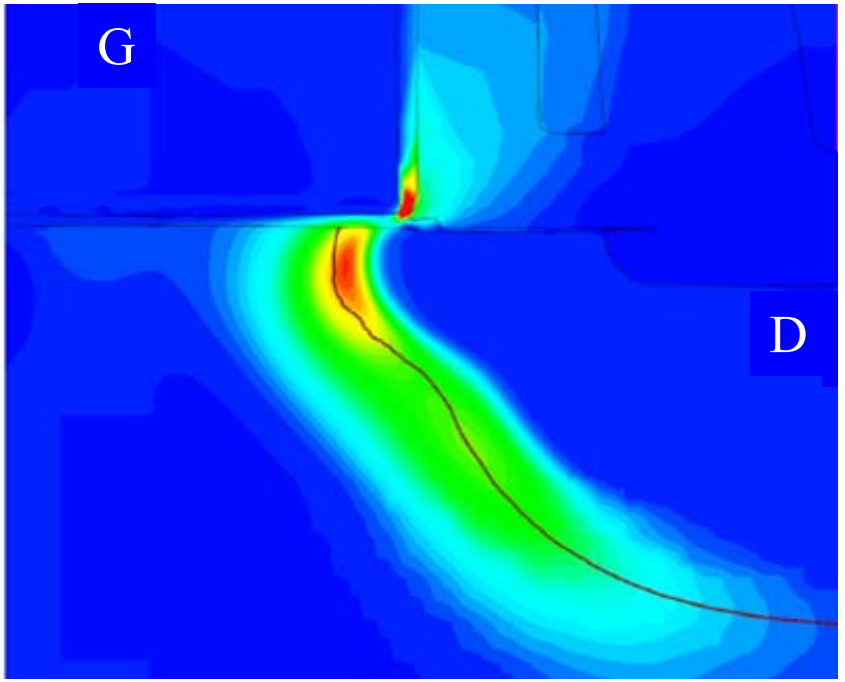




Saturation



Potential

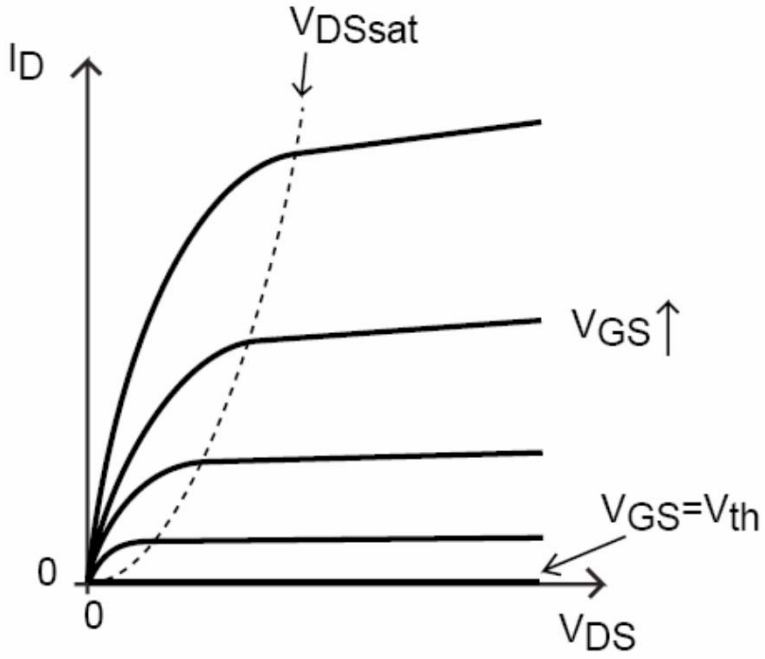


Electric field strength

Alexander Schiffmann, Master Thesis (2016)

MOSFET (saturation regime)

$$I_{sat} = \frac{Z}{2L}\mu_n C_{ox}\left(V_G - V_T\right)^2\left(1-\lambda\left(V_D - V_{sat}\right)\right)$$



Experimentally: channel length modulation $\lambda \propto \frac{1}{L}$

High frequencies

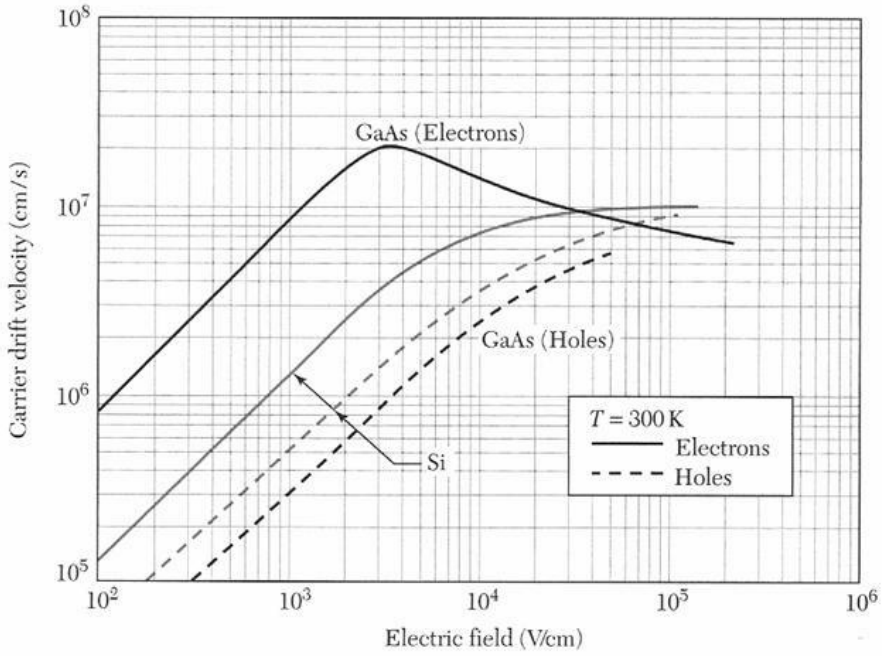
$$\tilde{i}_{in} = 2\pi f C_G \tilde{v}_G \qquad \tilde{i}_{out} = g_m \tilde{v}_G$$

$$\tilde{i}_{in} < \tilde{i}_{out}$$

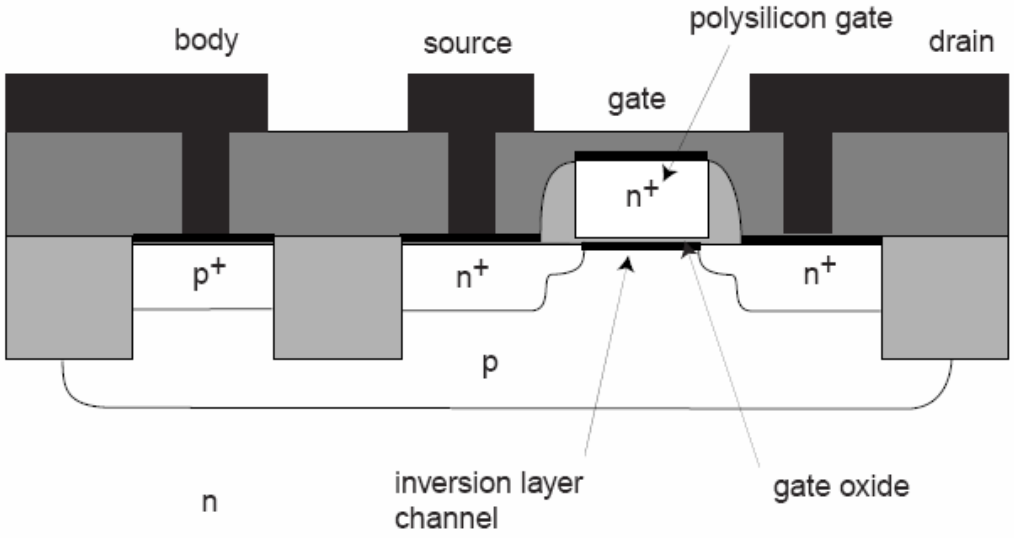
$$f < \frac{g_m}{2\pi C_G} \propto \frac{1}{s^2} = f_T$$

For large E, Ohm's law ($j = ne\mu E$) is not valid. The electron velocity saturates. For velocity saturation:

$$f_T \approx \frac{v_s}{L}$$



Constant E-field Scaling



Gate length L, transistor width Z, oxide thickness t_{ox} are scaled down.

V_{ds}, V_{gs}, and V_T are reduced to keep the electric field constant.

Power density remains constant.

$$L \sim 45\ t_{ox}$$

1975 - 1990: "Days of happy scaling"

Constant E-field scaling

$$I_{sat} = \frac{Z}{2L}\mu_n \frac{\varepsilon_{ox}}{t_{ox}}\left(V_G - V_T\right)^2$$

$$L \Rightarrow sL, \qquad Z \Rightarrow sZ, \qquad t_{ox} \Rightarrow st_{ox}, \qquad V_{th} \Rightarrow sV_{th}$$

$$I_{sat} \Rightarrow sI_{sat} \quad \longleftarrow \quad I_{sat} \text{ gets smaller}$$

$$g_m = \frac{dI_D}{dV_G} = \frac{Z}{L}\mu_n \frac{\varepsilon_{ox}}{t_{ox}}\left(V_G - V_T\right) \quad \longleftarrow \quad \text{Transconductance stays the same.}$$

Power per transistor decreases like L^2. Power per unit area remains constant.

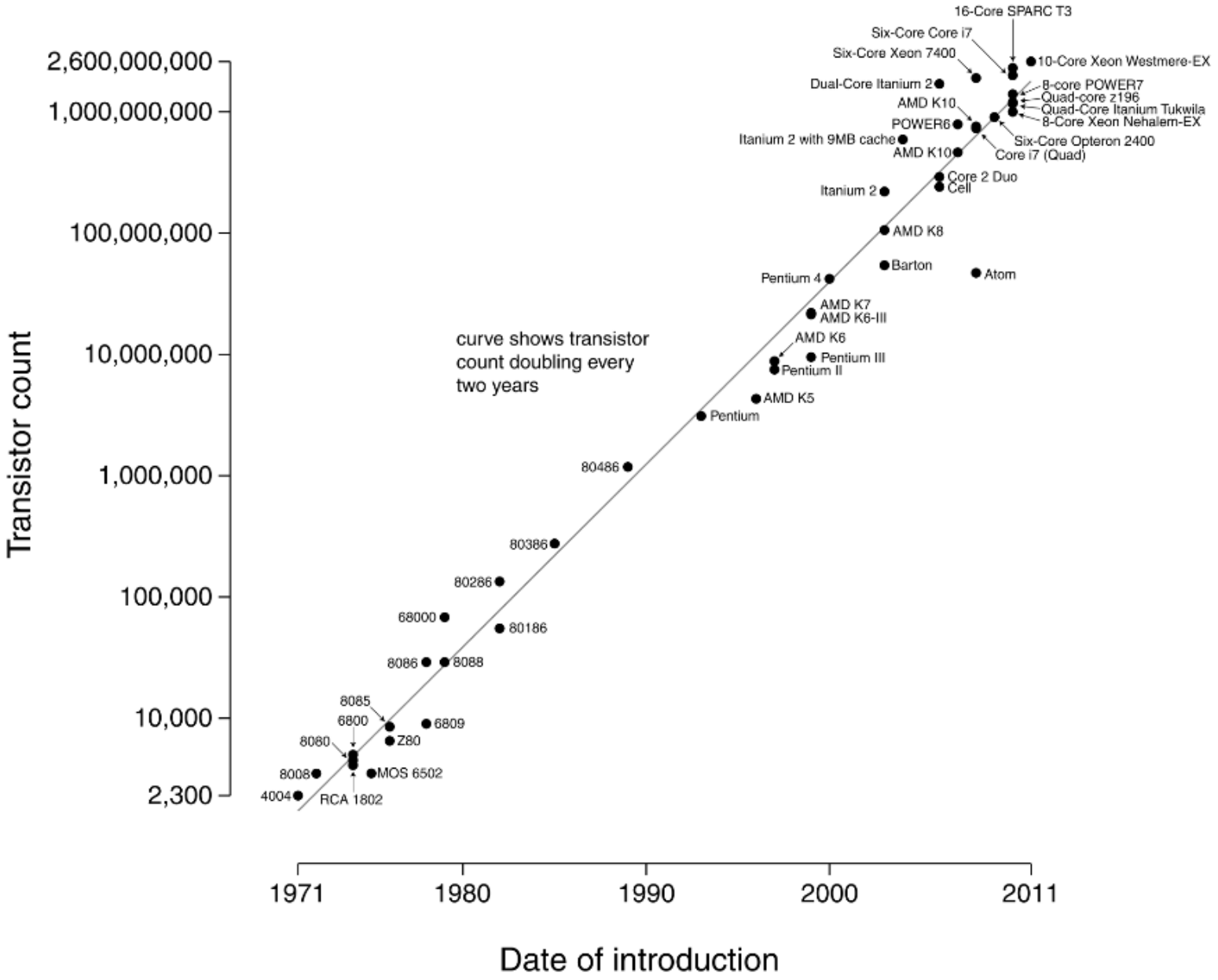
The heat dissipation problem

Microprocessors are hot ~ 100 C
Hotter operation will cause dopants to diffuse

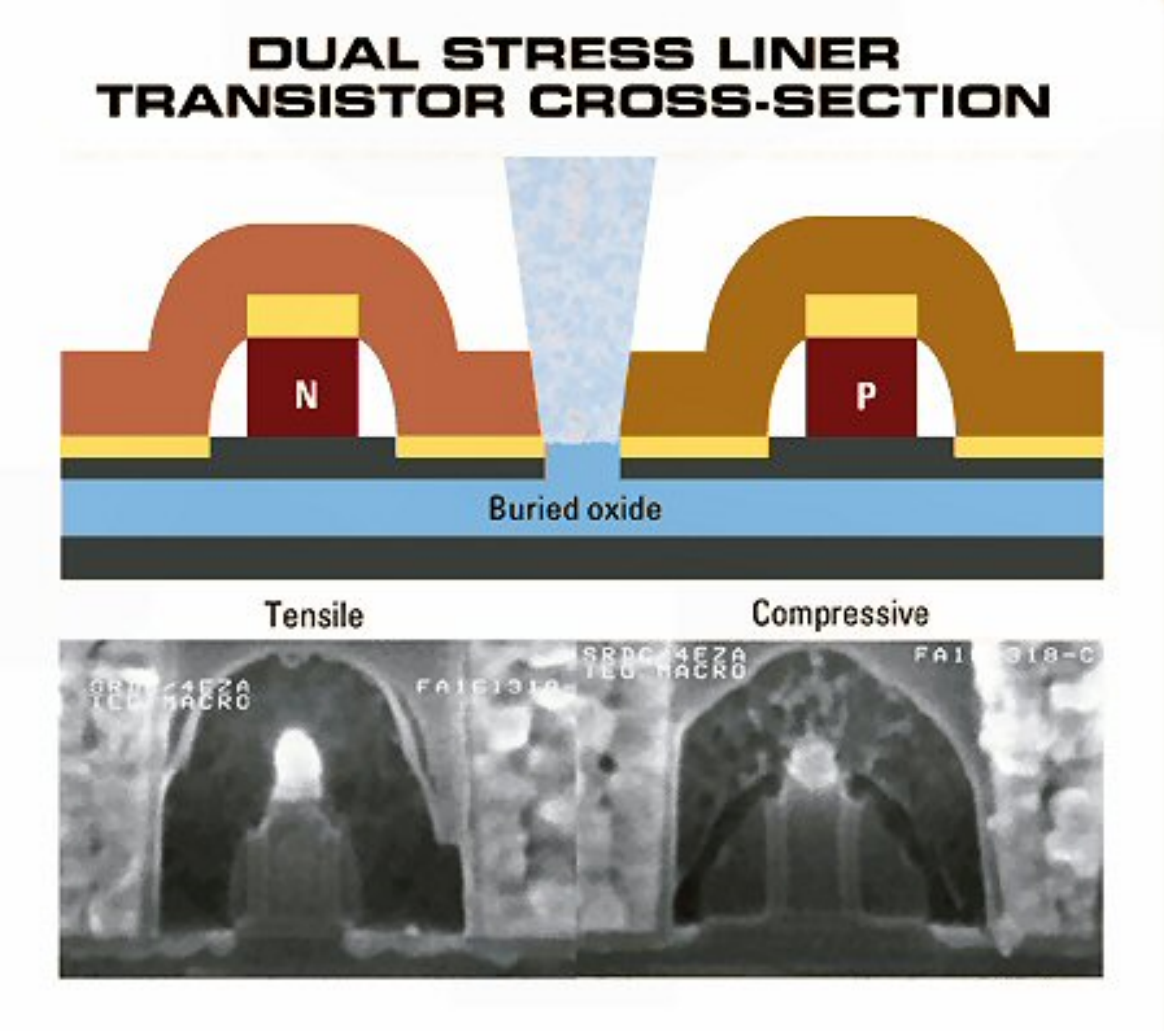
When more transistors are put on a chip they must dissipate less power.

Power per transistor decreases like L^2.

Microprocessor Transistor Counts 1971-2011 & Moore's Law



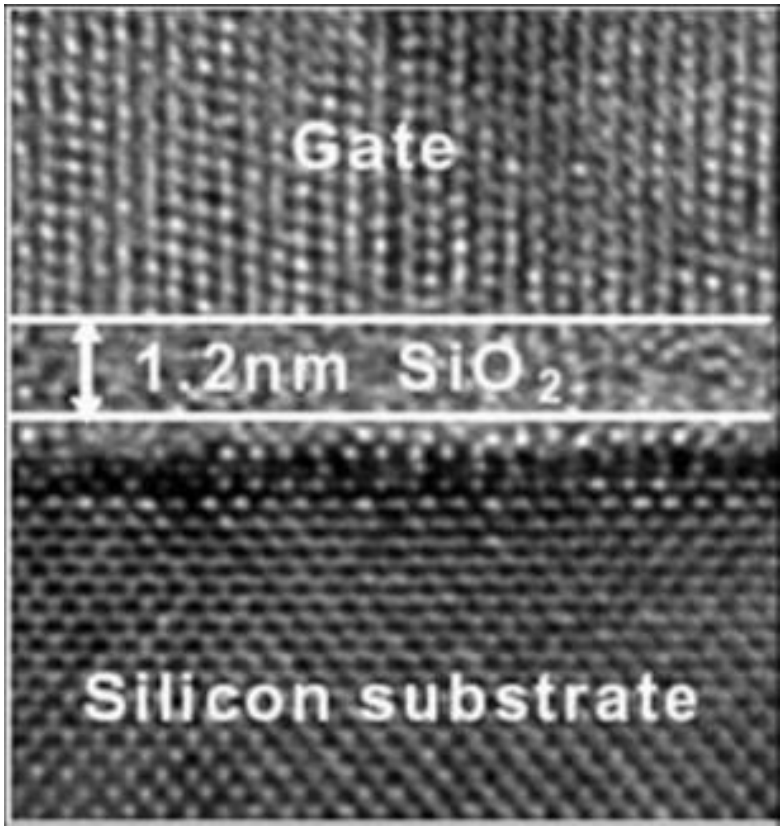
Dual stress liners



Tensile silicon nitride film over the NMOS and a compressive silicon nitride film over the PMOS improves the mobility.

http://www.xbitlabs.com/articles/cpu/display/athlon64-venice_2.html

Gate dielectric



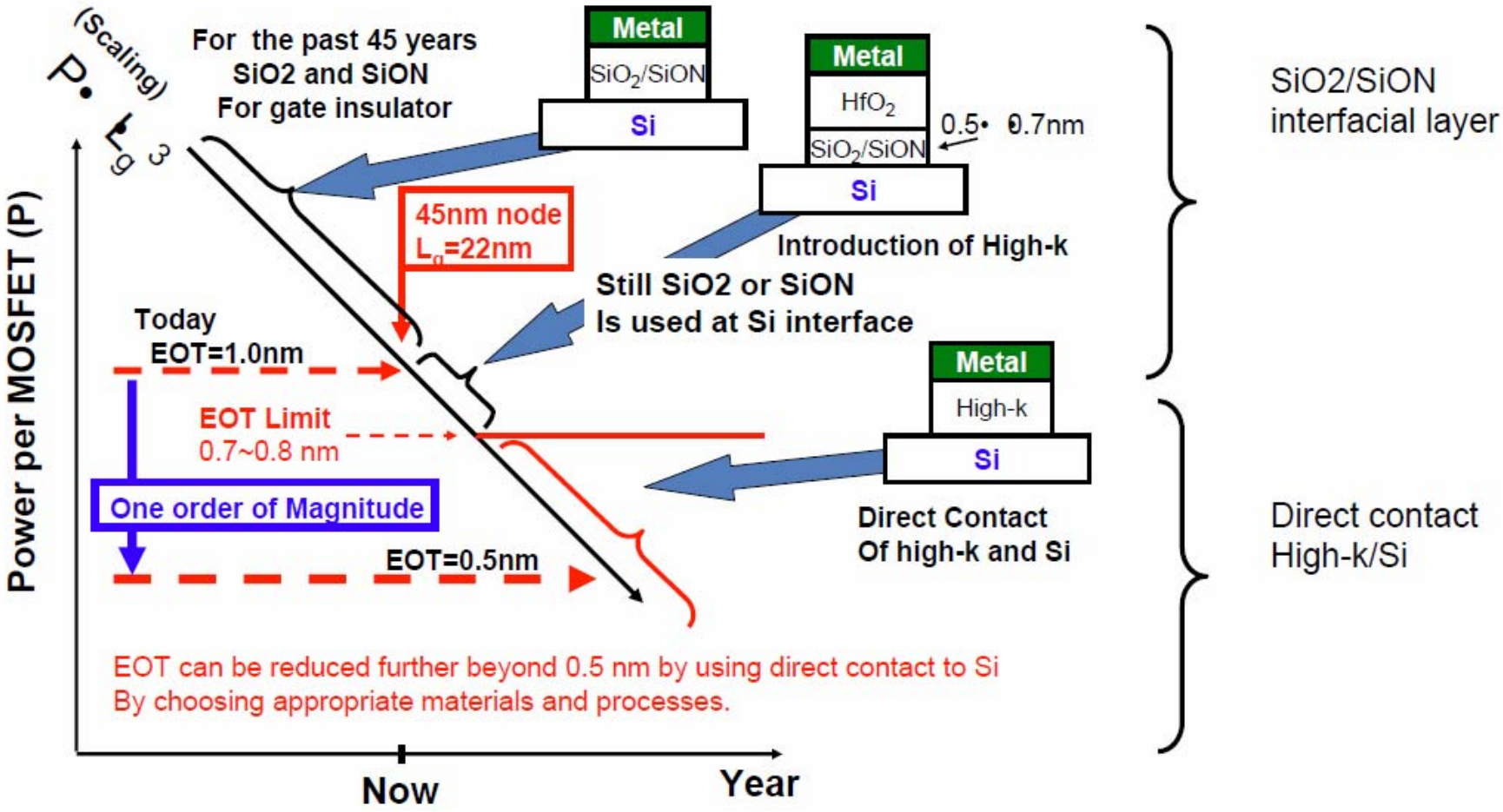
Thinner than 1 nm: electrons tunnel

Large dielectric constant desirable

$\varepsilon_r(SiO_2) \sim 4$

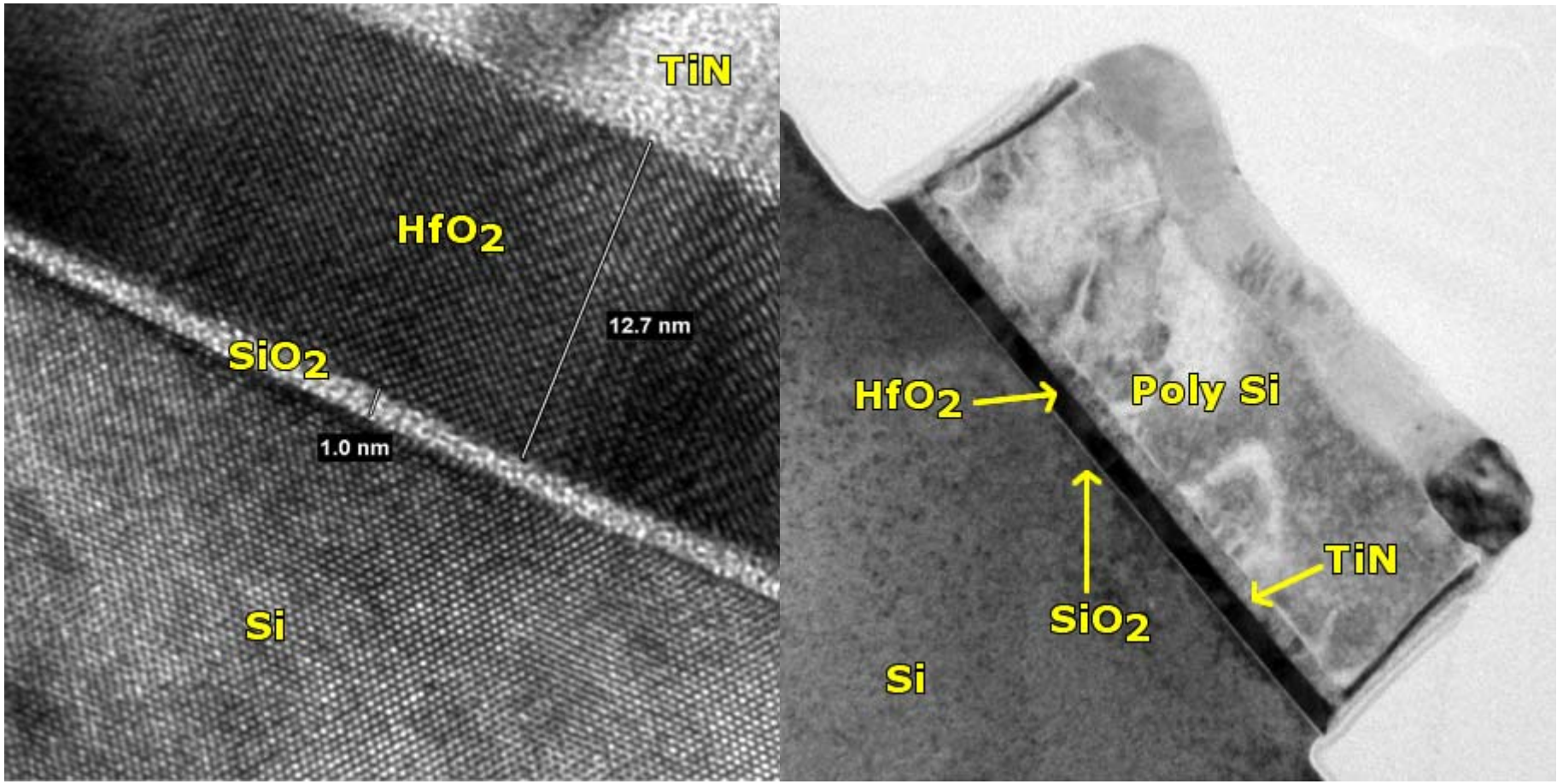
$\varepsilon_r(Si_3N_4) \sim 7$

Direct contact technology of high-k to Si



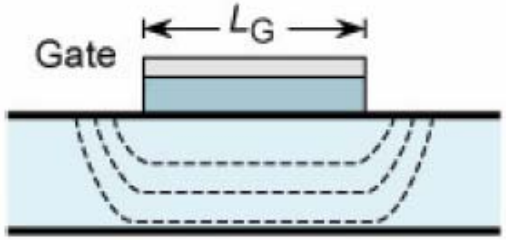
www.iwailab.ep.titech.ac.jp

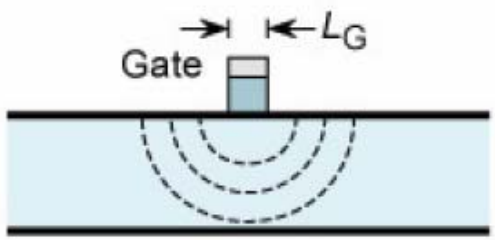
High-k dielectrics

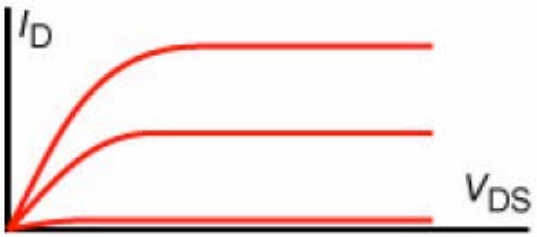


http://nano.boisestate.edu/research-areas/gate-oxide-studies/

Short channel effects







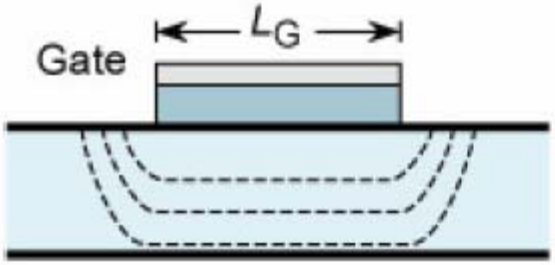
Short-channel effects:

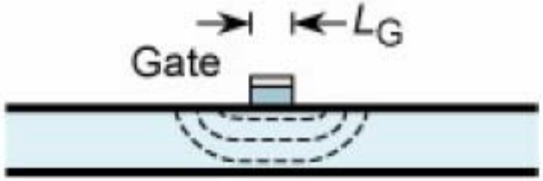
Threshold-voltage shift

Lack of pinch-off

Increased leakage current

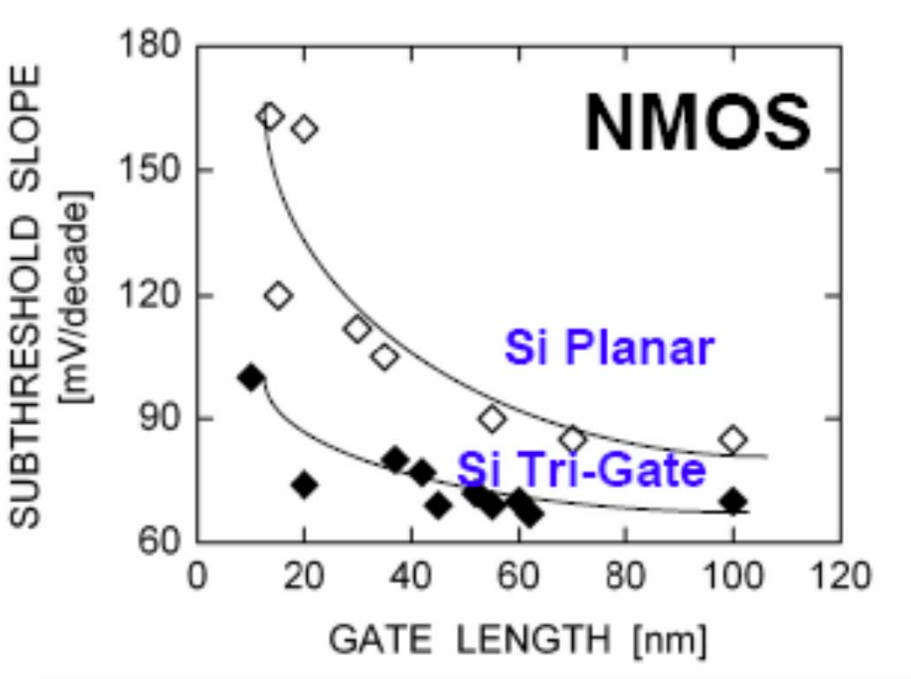
Increase of output conductance



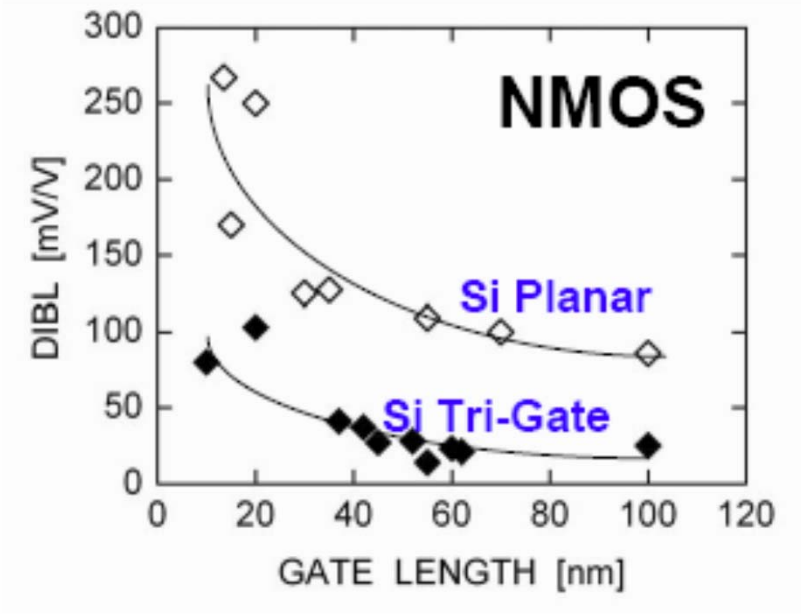


SOI: silicon on insulator

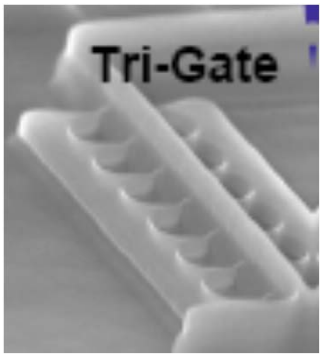
FinFET, Tri-gate



Drain induced barrier lowering

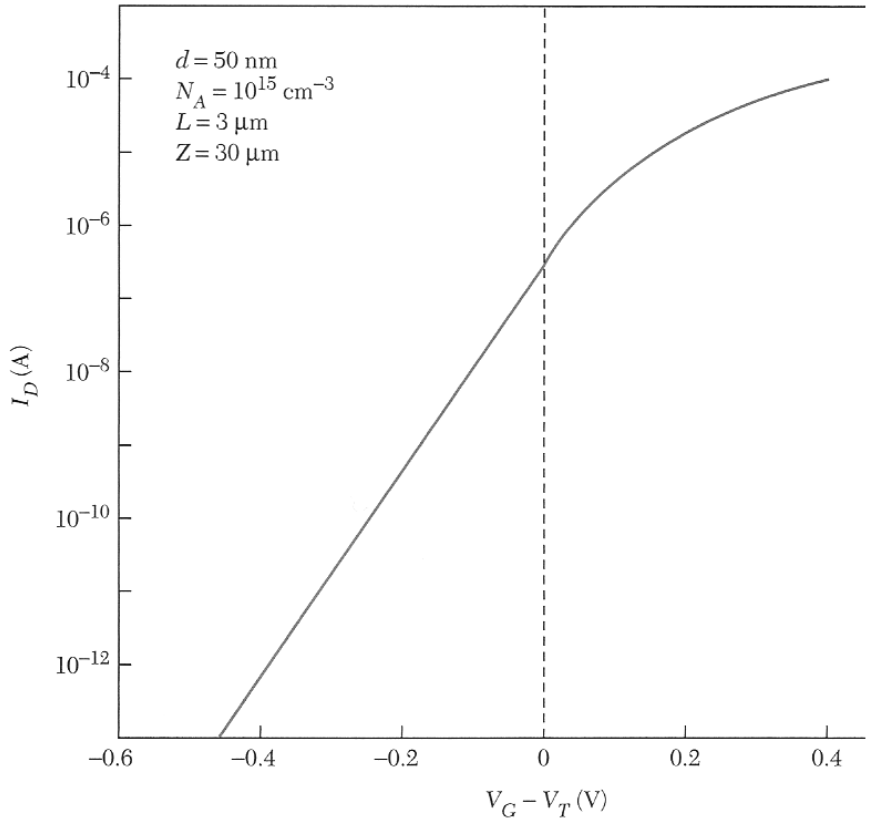


Robert Chau, Intel



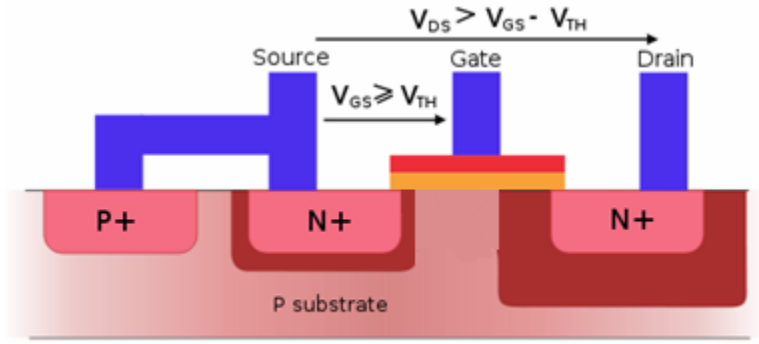
Subthreshold current

For $V_G < V_T$ the transistor should switch off but there is a diffusion current. The current is not really off until ~ 0.5 V below the threshold voltage.



Weak inversion

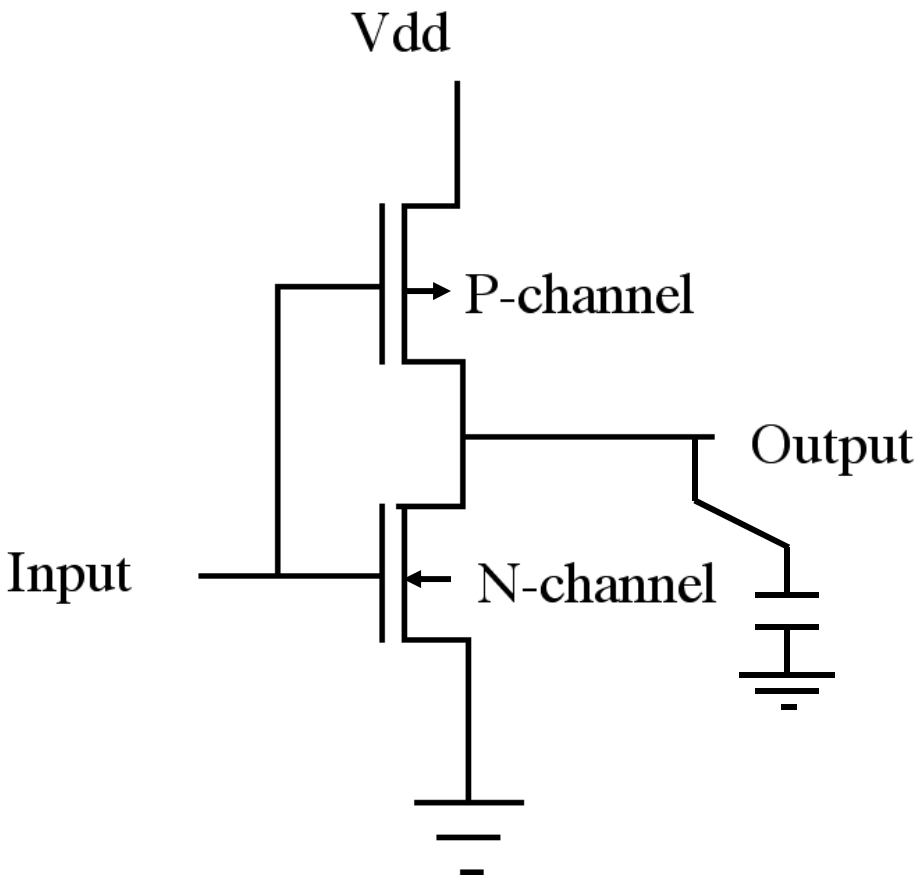
$$I_D \propto \exp\left(\frac{e(V_G - V_T)}{k_B T}\right)$$

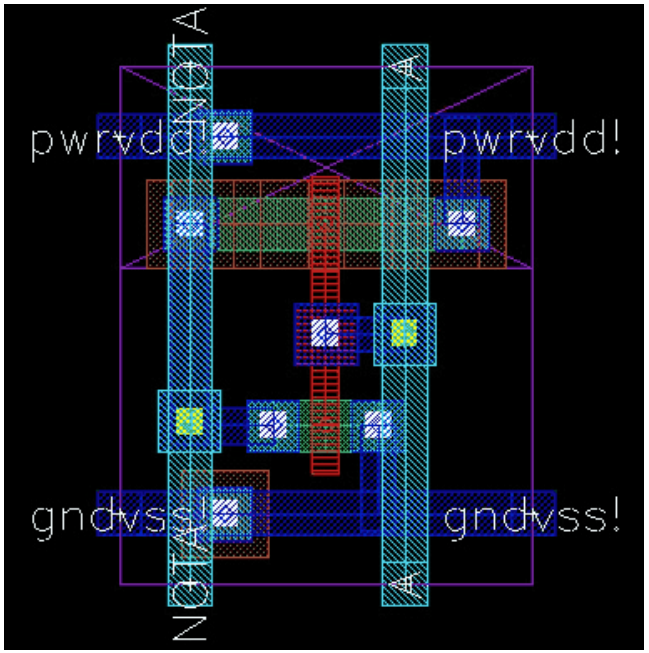


Subthreshold swing: 70-100 mV/decade

CMOS inverter

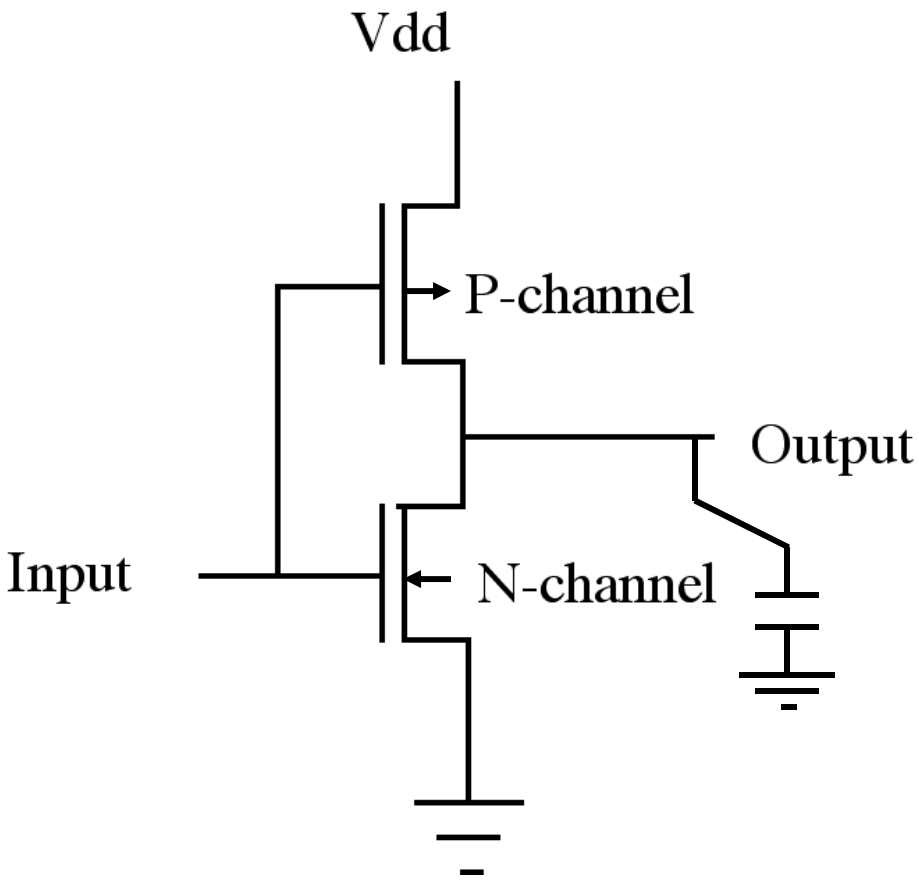
Complementary Metal Oxide Semiconductor



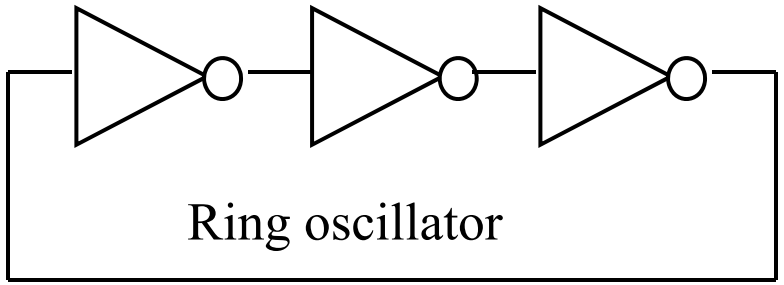


$$E = QV_{dd} = CV_{dd}^2$$

Gate delay

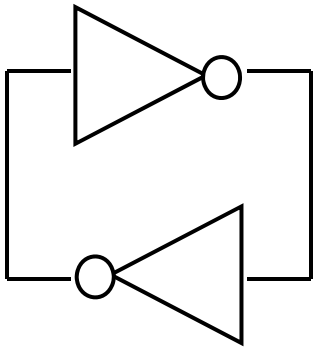


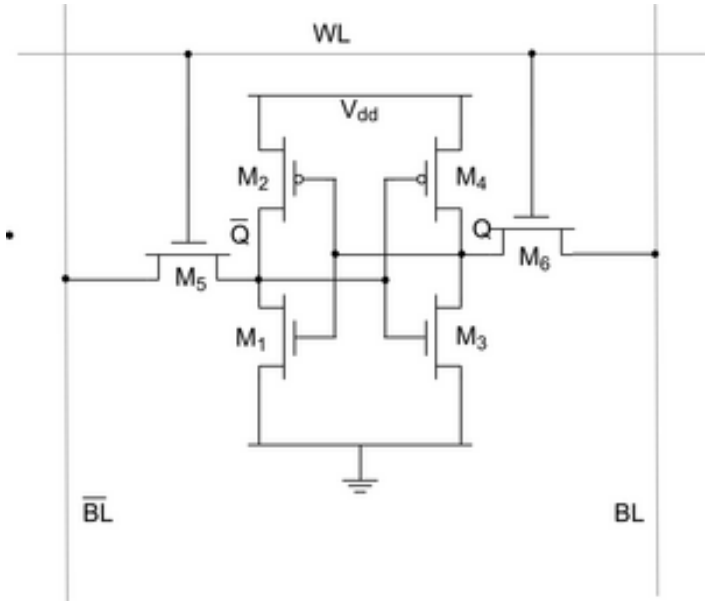
Gate delay is limited by $C_{gate}V_{dd}/I$.



SRAM

Static random access memory

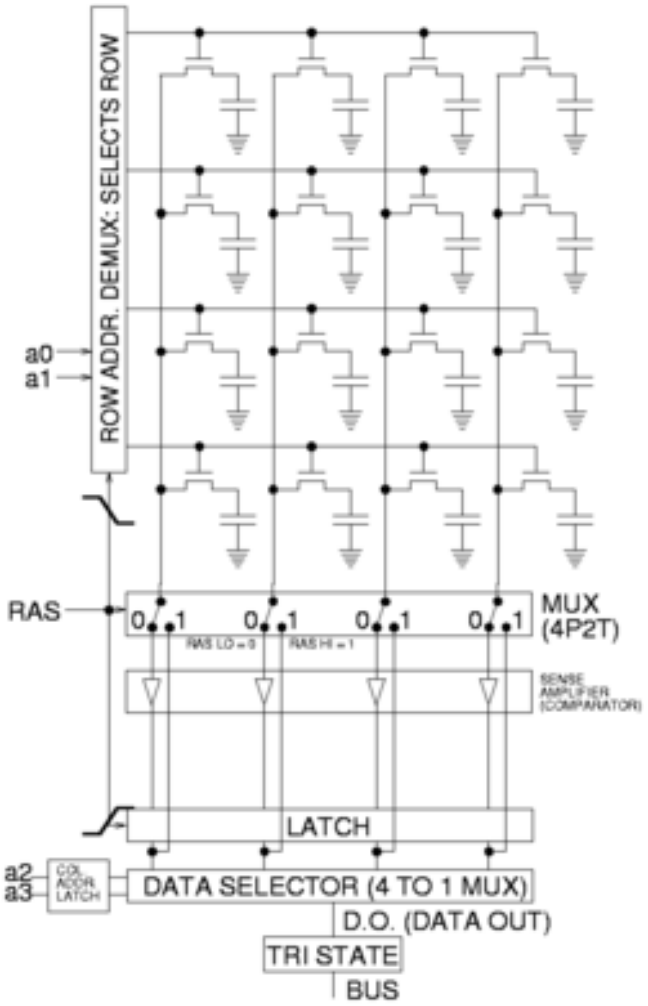




No refresh circuitry needed.

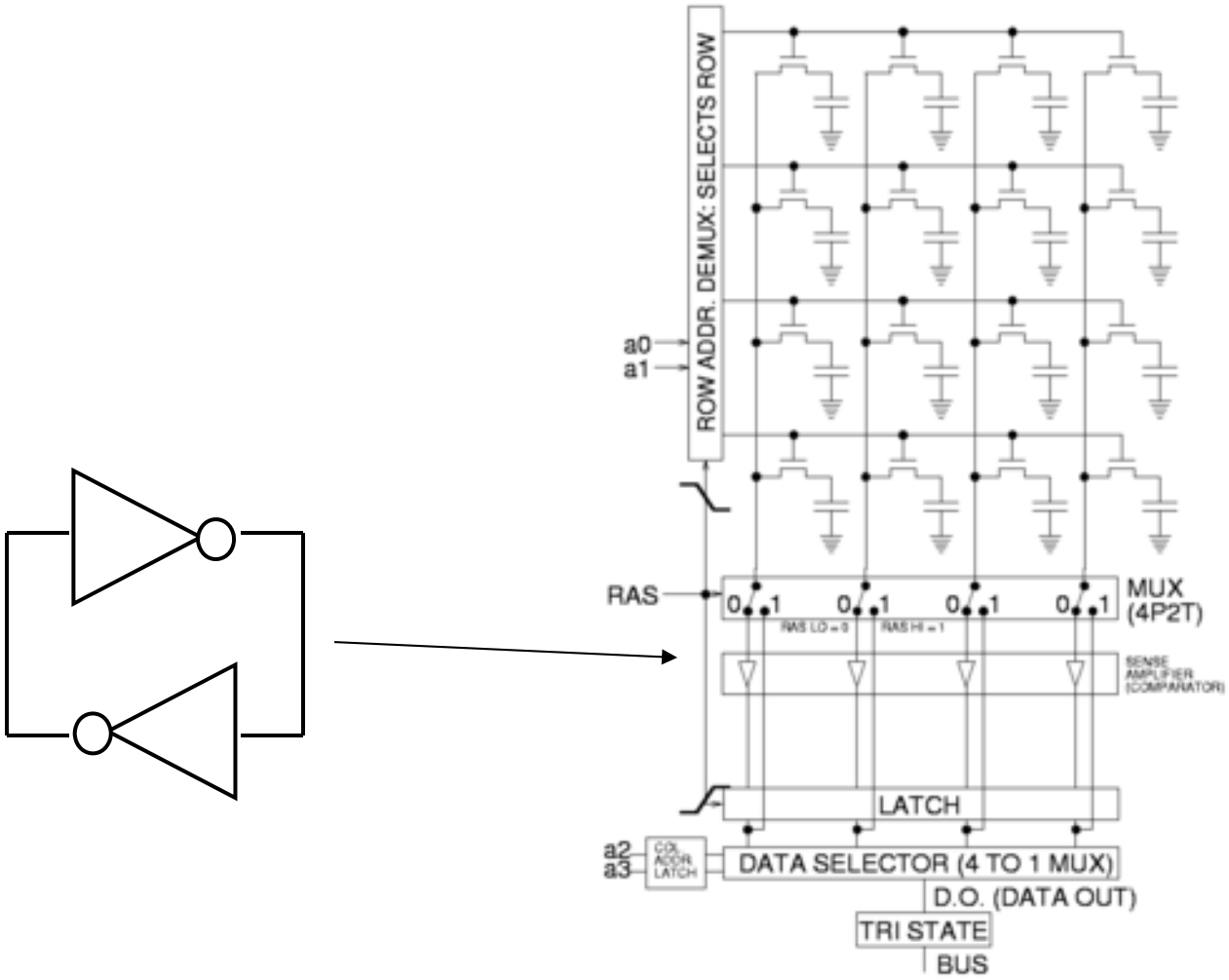
DRAM

Dynamic random access memory

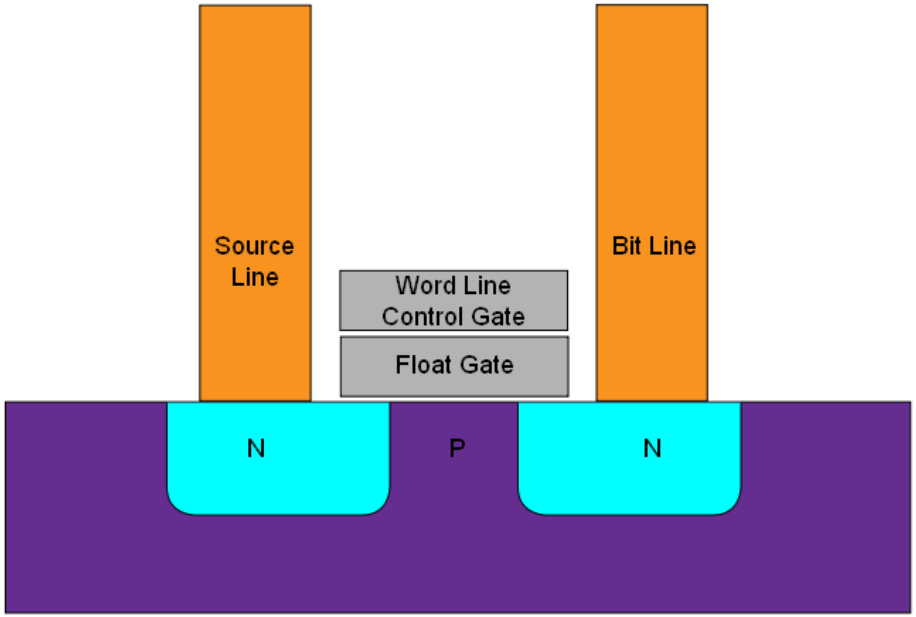


DRAM

Read and refresh DRAM with a SRAM cell



Flash memory



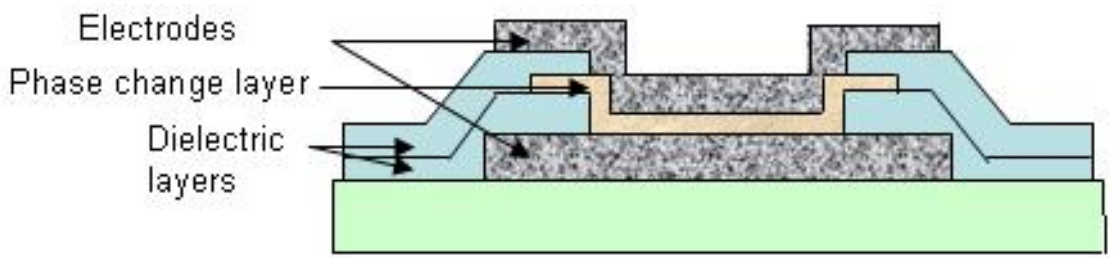
Charge is stored on a floating gate

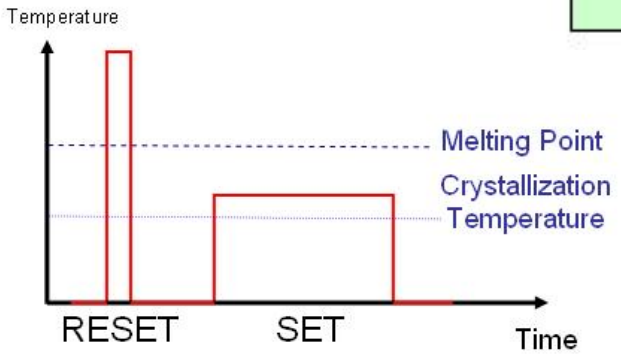
nonvolatile

Phase change memory

Phase-change memory (PRAM) uses chalcogenide materials. These can be switched between a low resistance crystalline state and a high resistance amorphous state.

GeSbTe is melted by a laser in rewritable DVDs and by a current in PRAM.





nonvolatile

High Bandwidth Memory

AMD to launch its HBM graphics cards on 16 June 2015.