

12. MOSFETs

Jan. 8, 2020

Exams

January 31

March 4

April 24

June 24

October ...

Exam

Calculator is ok. One A4 of handwritten notes.

Explain some concept:

(tunnel contact, indirect band gap, thermionic emission, inversion, threshold voltage, ...)

Perform a calculation:

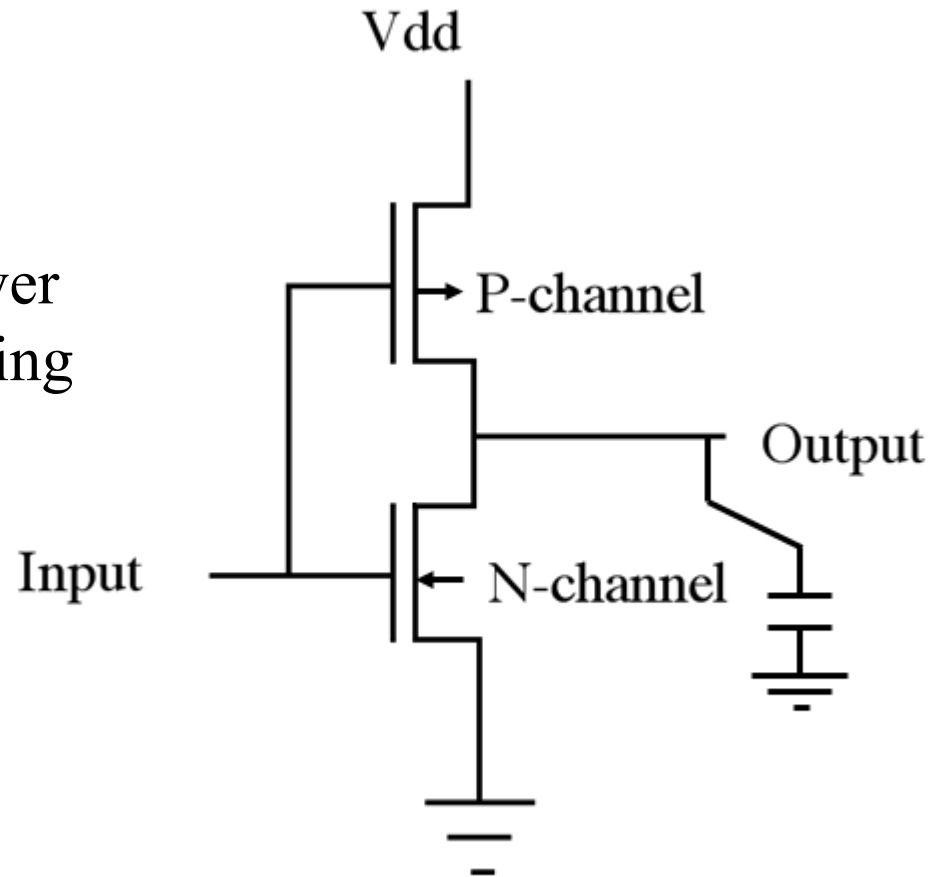
(concentration of minority carriers, integrate charge density to find electric field, ...)

Explain how a device works:

(JFET, MESFET, MOSFET, laser diode, bipolar transistor, LED, Schottky diode, Heterojunction bipolar transistor, ...)

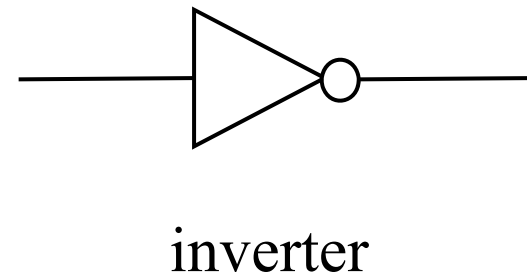
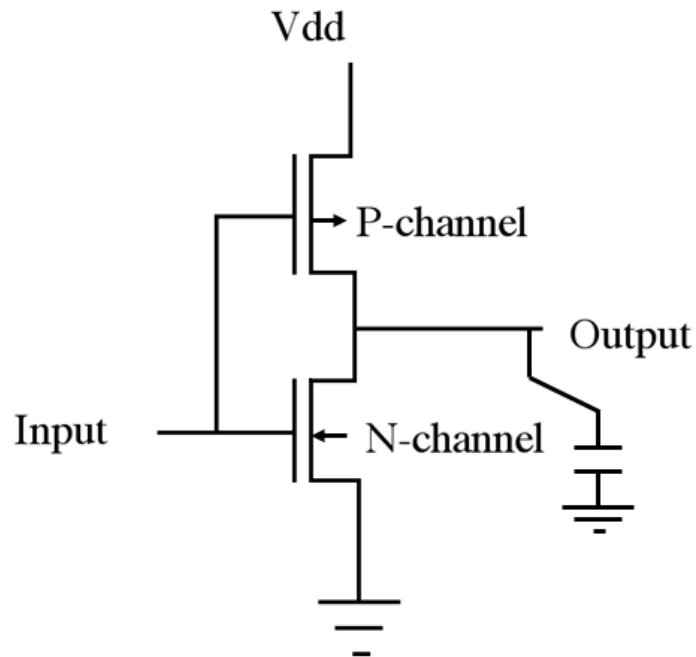
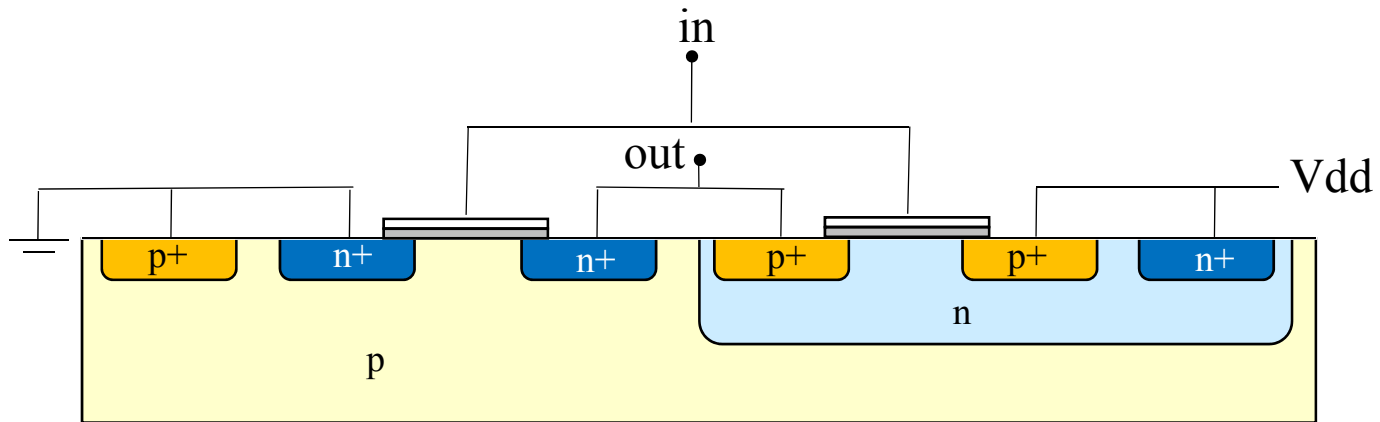
CMOS inverter

Dissipates little power
except when switching

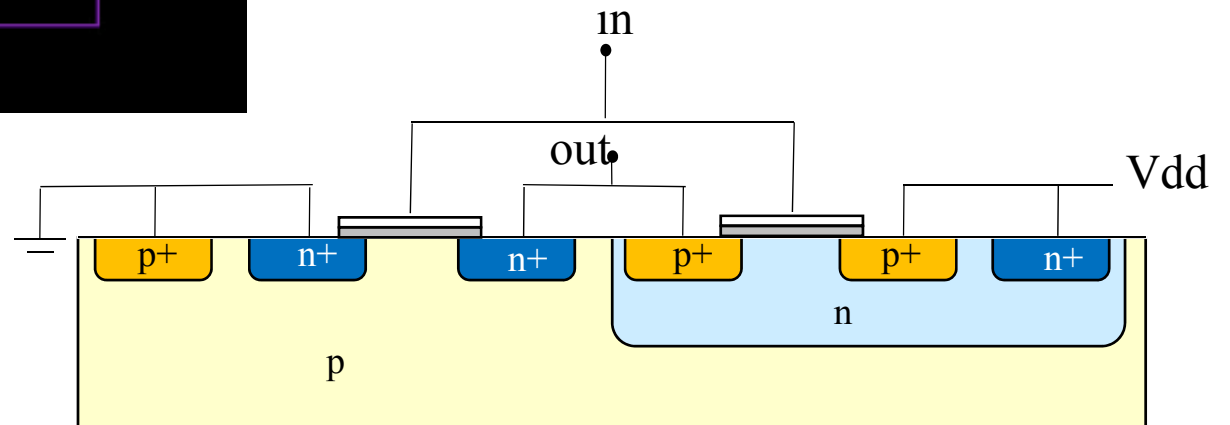
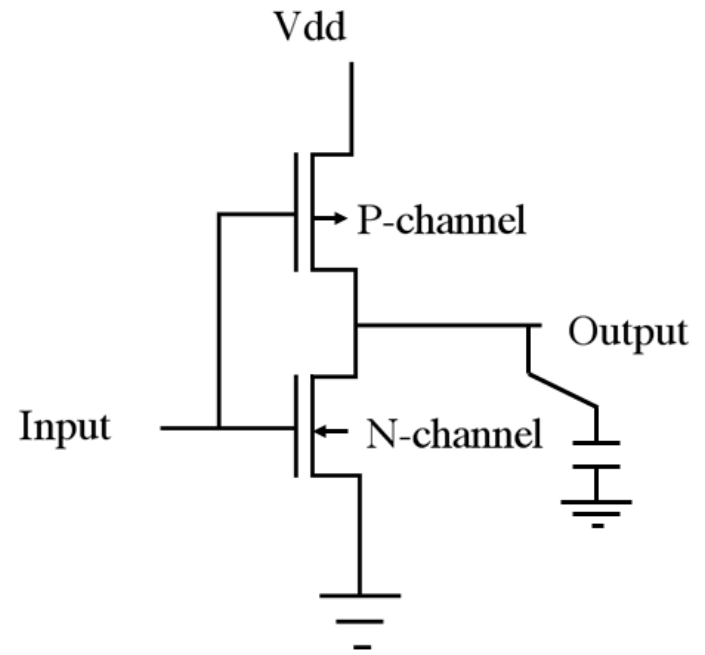
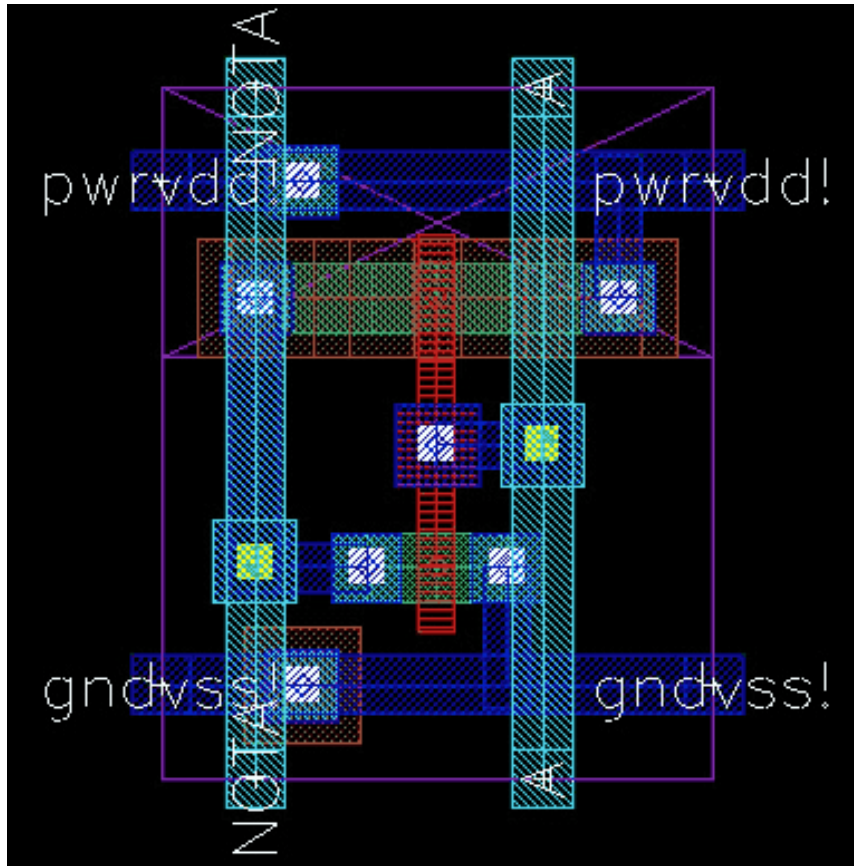


$$E = QV_{dd} = CV_{dd}^2$$

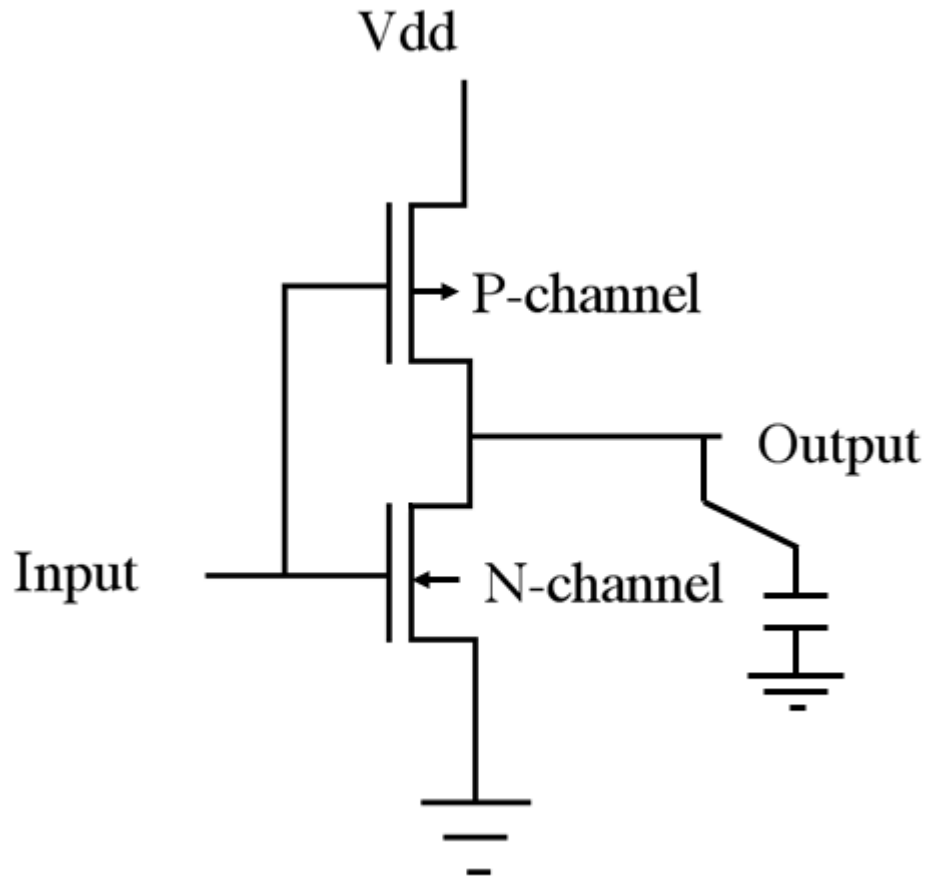
CMOS inverter



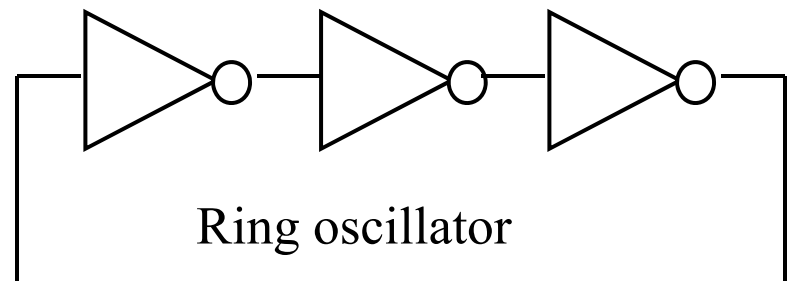
CMOS inverter



Gate delay

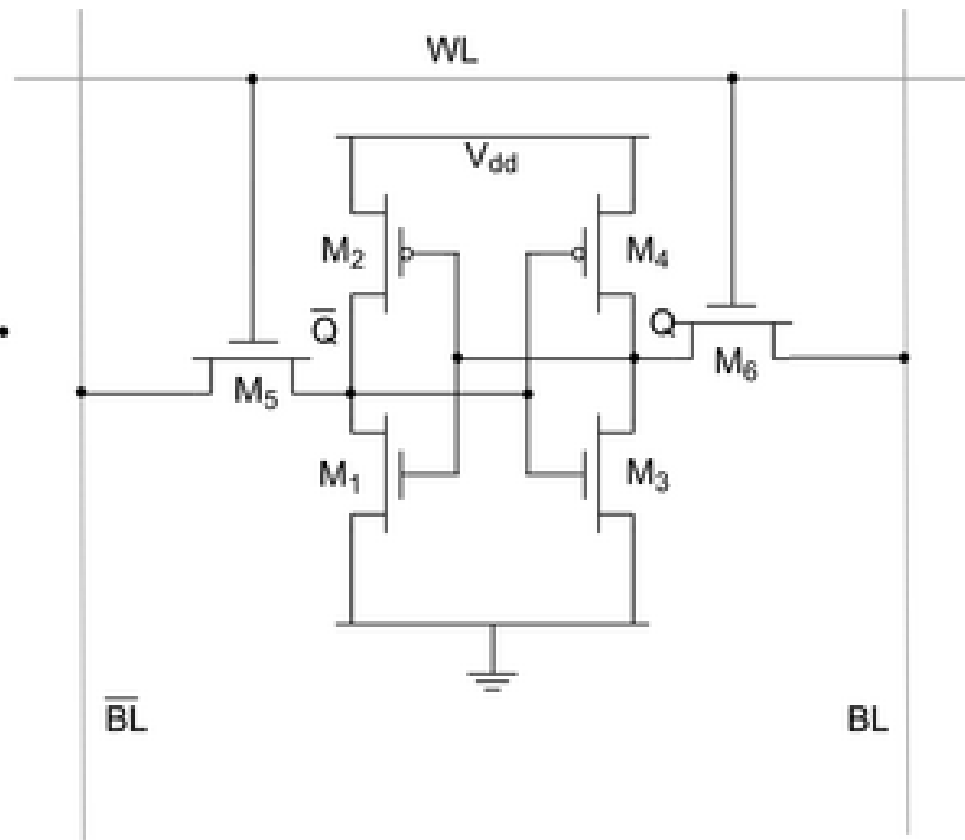
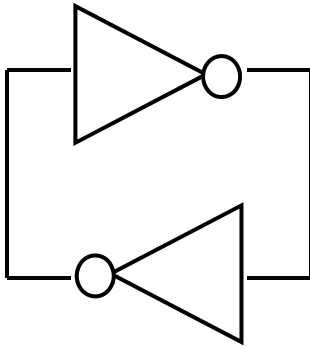


Gate delay is limited by $C_{gate}V_{dd}/I$.



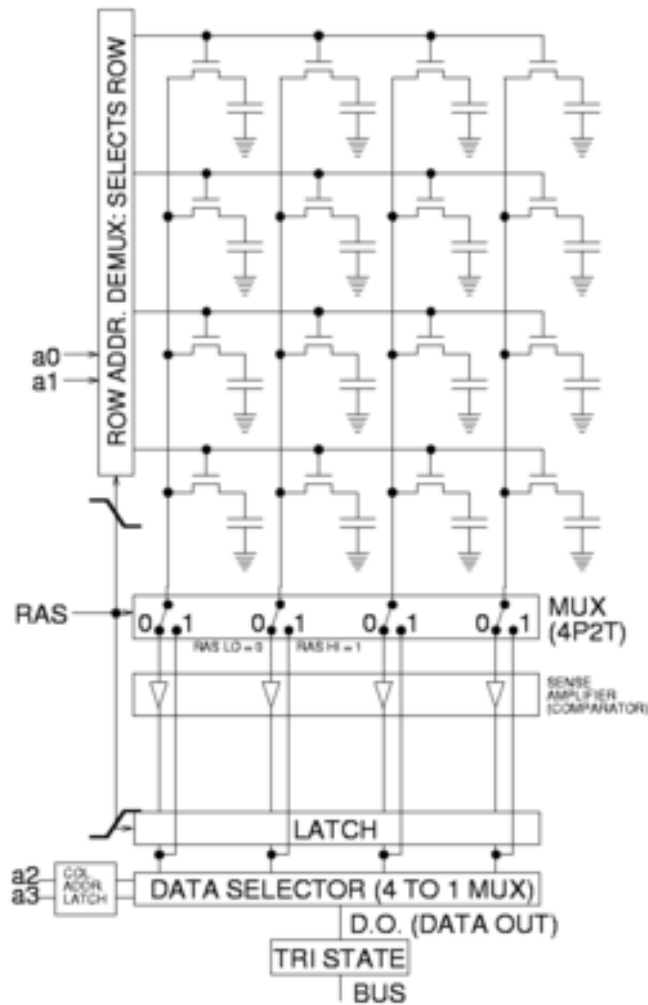
SRAM

Static random access memory



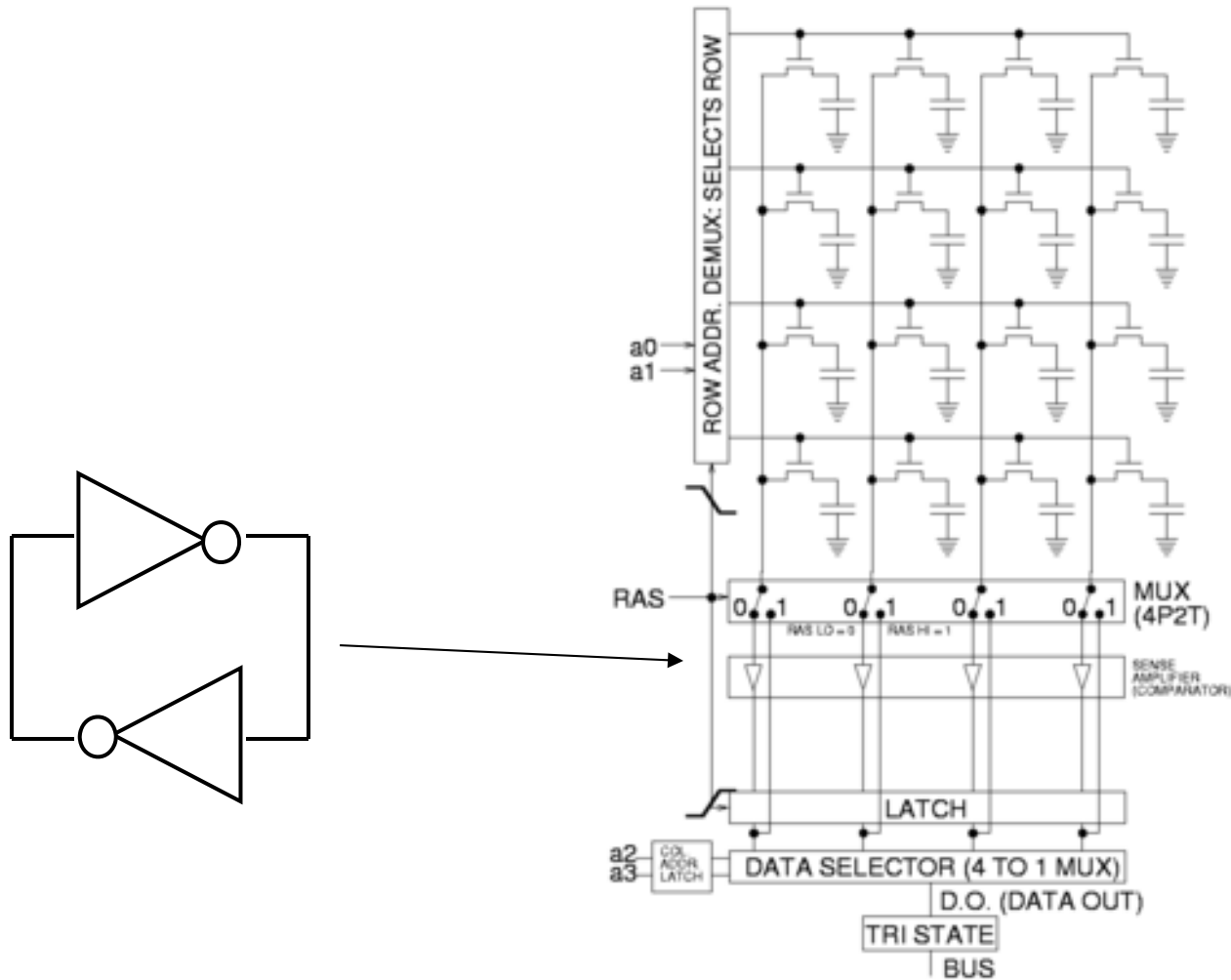
DRAM

Dynamic random access memory

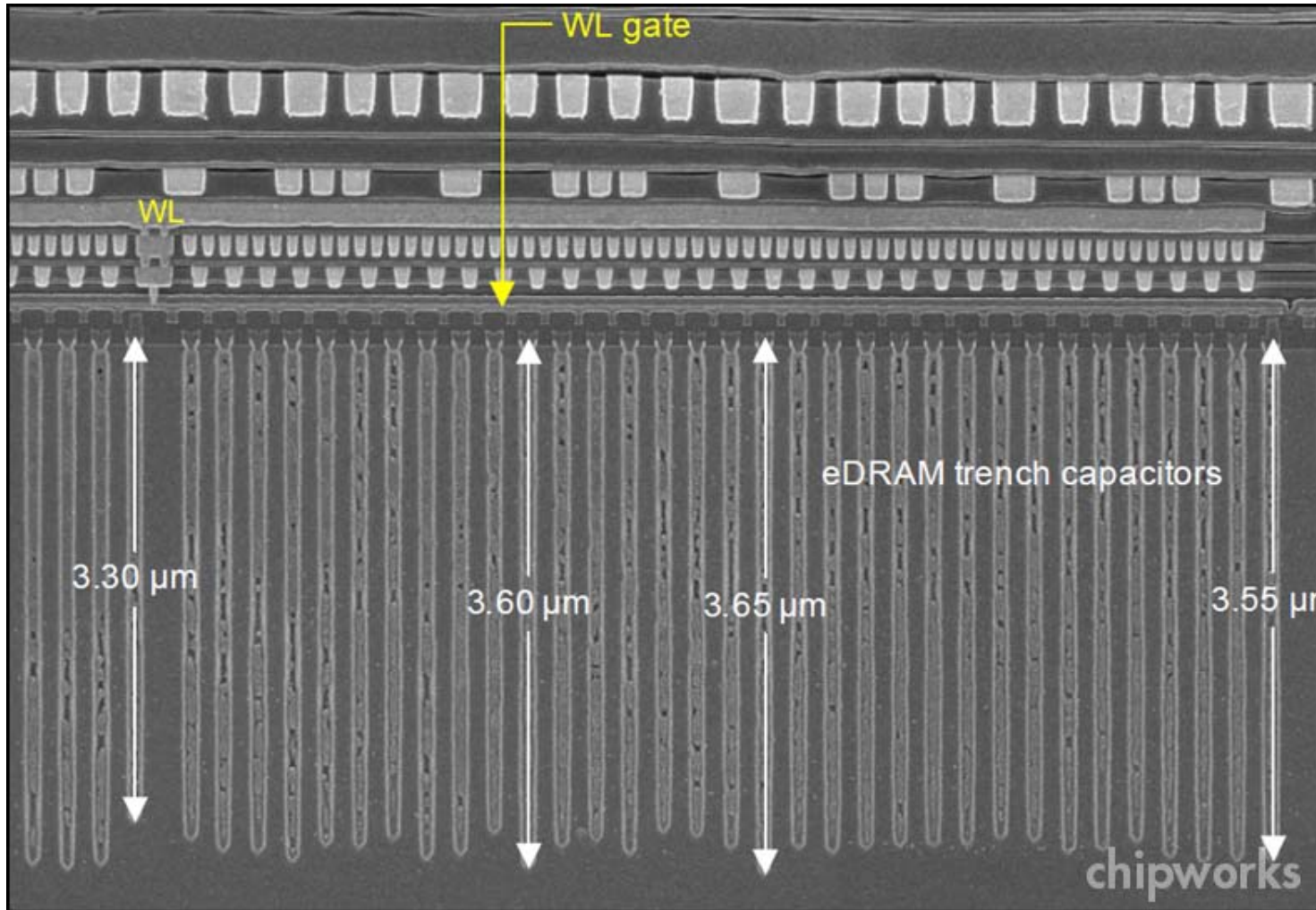


DRAM

Read and refresh DRAM with a SRAM cell



DRAM

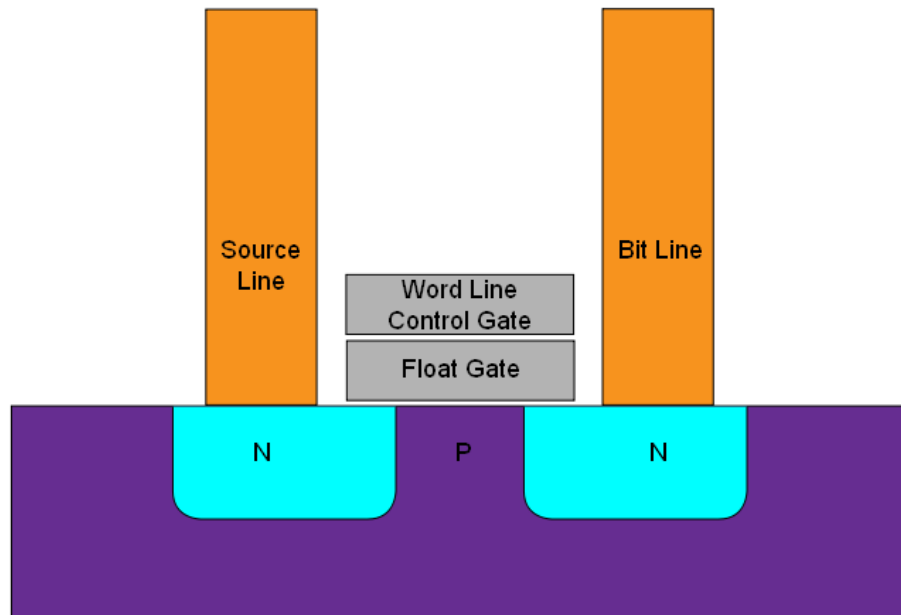


75:1

Silicon oxynitride SiO_xN_y dielectric

http://electroi.com/chipworks_real_chips_blog/

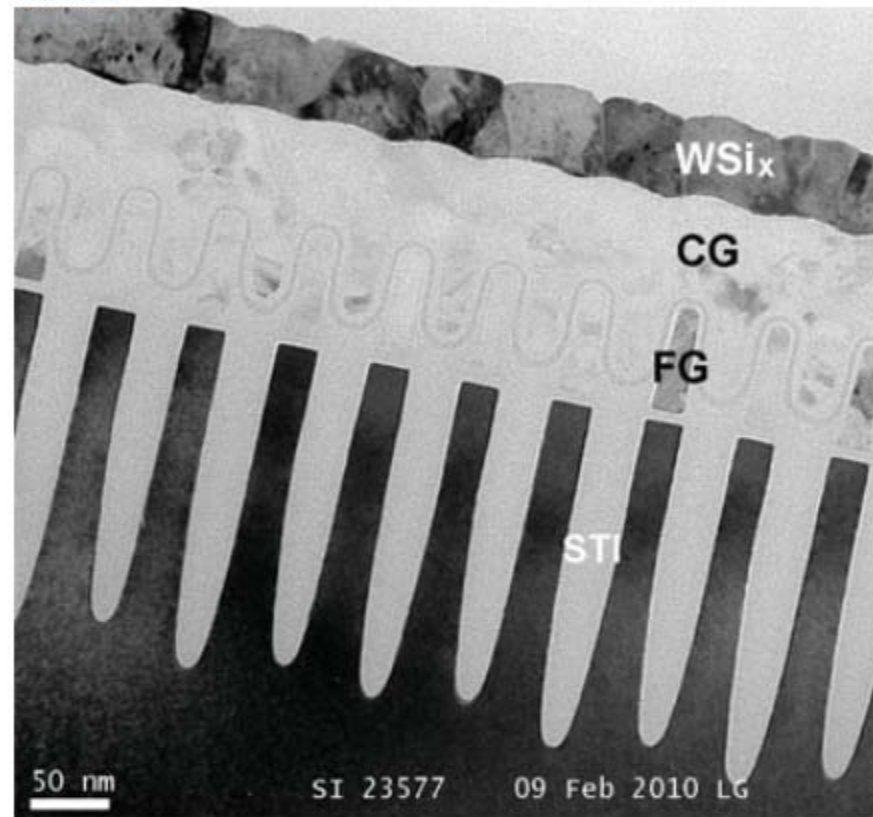
Flash memory



Charge is stored on a floating gate

nonvolatile

Intel Micron Flash Technologies (IMFT)
Shallow Trench Isolation (STI)
Control Gate (CG)
Floating Gate (FG)
Self-Aligned Doubled Patterning (SADP)

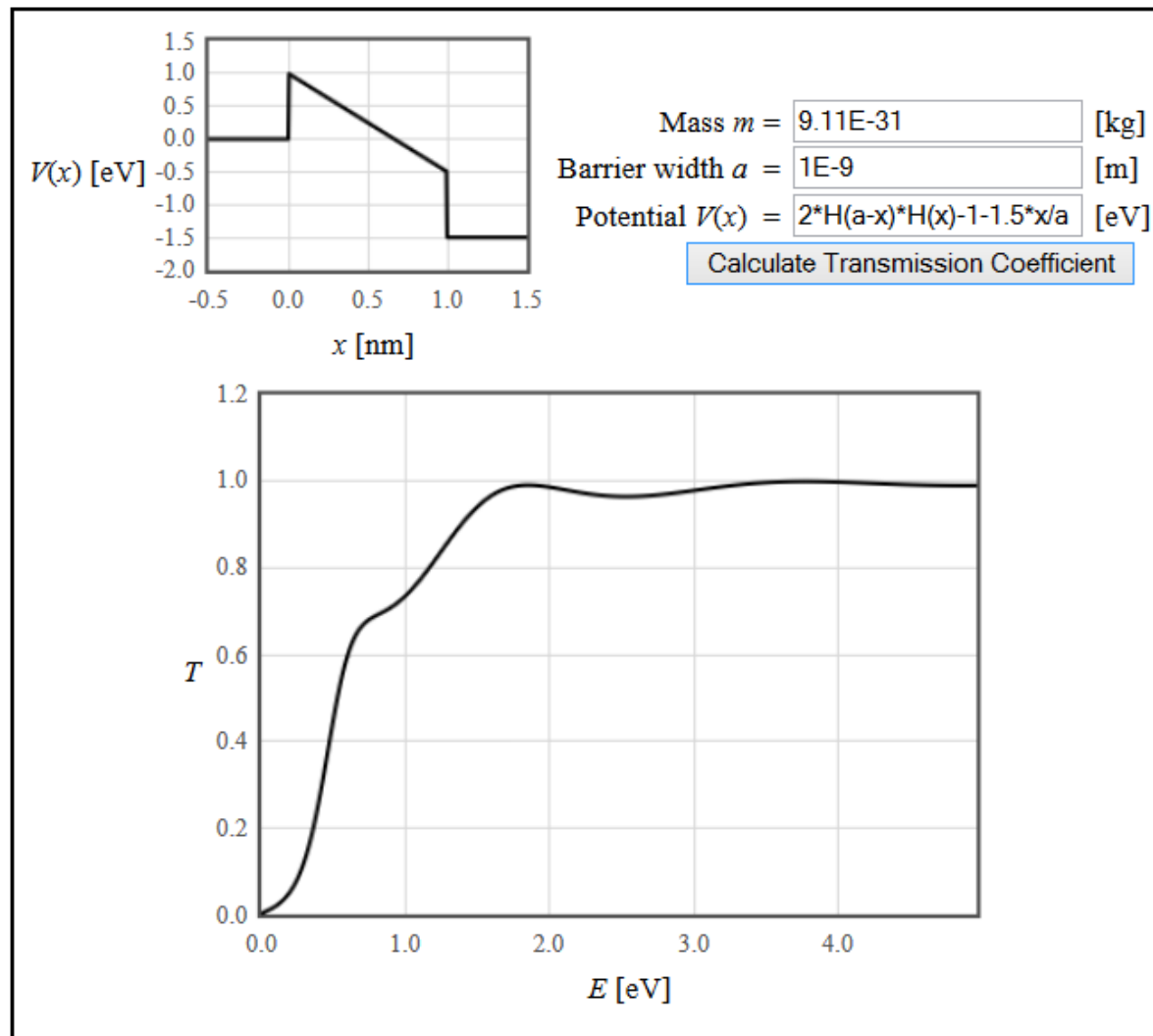


Topographical SEM image of the IMFT 25-nm flash memory array at gate level: array trench depth is shallower to allow a denser flash array

The extent of immersion-lithography tool usage cannot be known, but our end-of-the-wordline analysis and STI pattern analysis of the IMFT device has shown some interesting spacing patterns that could give useful insight into the lithography and SADP processes. Technically, immersion lithography is the mainstream technology for NAND flash integration for sub-50 nm and is used along with SADP to shrink line widths and avoid overlay issues. Strongly enhanced DP (two exposures + spacer approach) could extend immersion to 21 nm and beyond. Since the extreme ultraviolet lithography (EUVL) tool is not going to be ready till 2012, immersion would continue to fill the gap up to 2x-nm node and beyond.

Tunneling through an arbitrarily shaped potential barrier

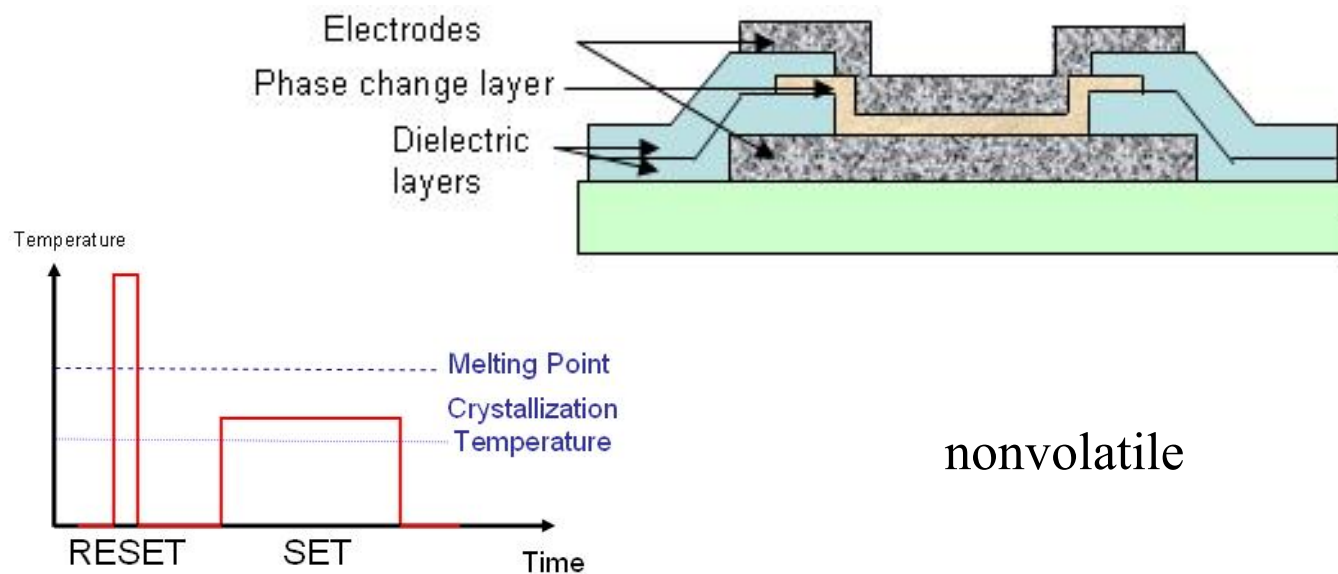
In quantum mechanics, there is some probability that a particle of mass m will tunnel through a potential barrier even if the energy of the particle is less than the energy of the barrier. During a direct tunneling process, the energy of the electron remains constant. The form below calculates the transmission coefficient for tunneling. The shape of the tunnel barrier can be arbitrarily defined in the interval between $x = 0$ and $x = a$. The potential is assumed to be constant to the left of the tunnel barrier at the value $V(x=0)$ and constant to the right of the barrier at the value $V(x=a)$.



Phase change memory

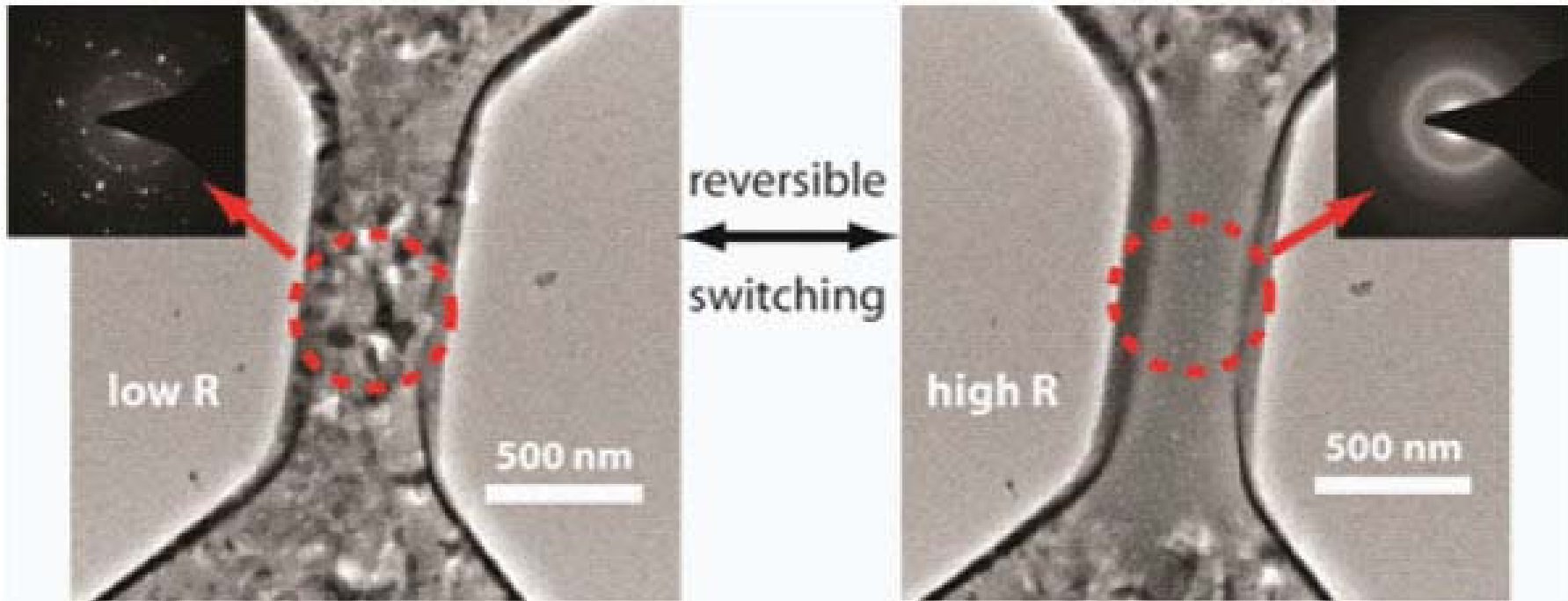
Phase-change memory (PCM) uses chalcogenide materials. These can be switched between a low resistance crystalline state and a high resistance amorphous state.

GeSbTe is melted by a laser in rewritable DVDs and by a current in PCM.



Phase change material

Electron diffraction in a TEM of a GeSbTe alloy.

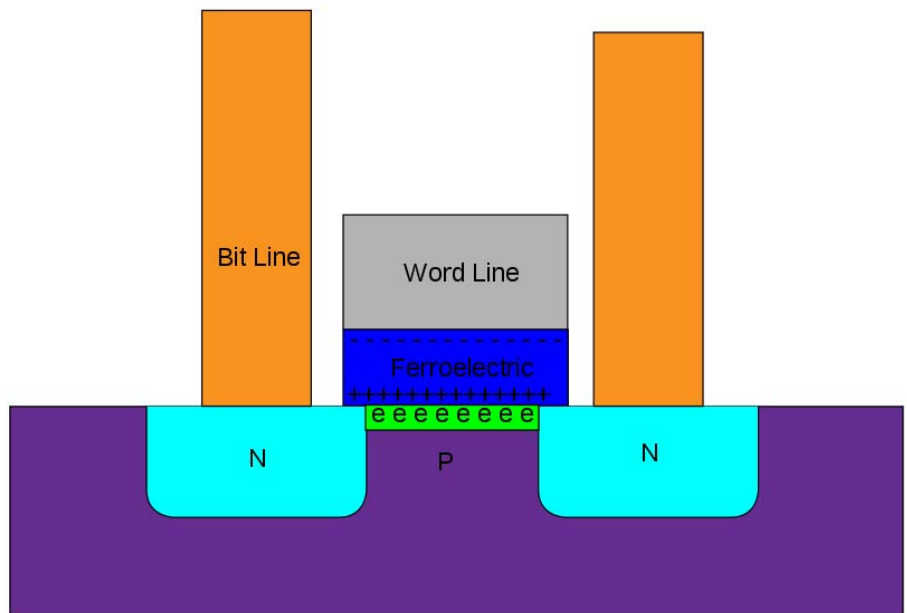


http://web.stanford.edu/group/cui_group/research.htm

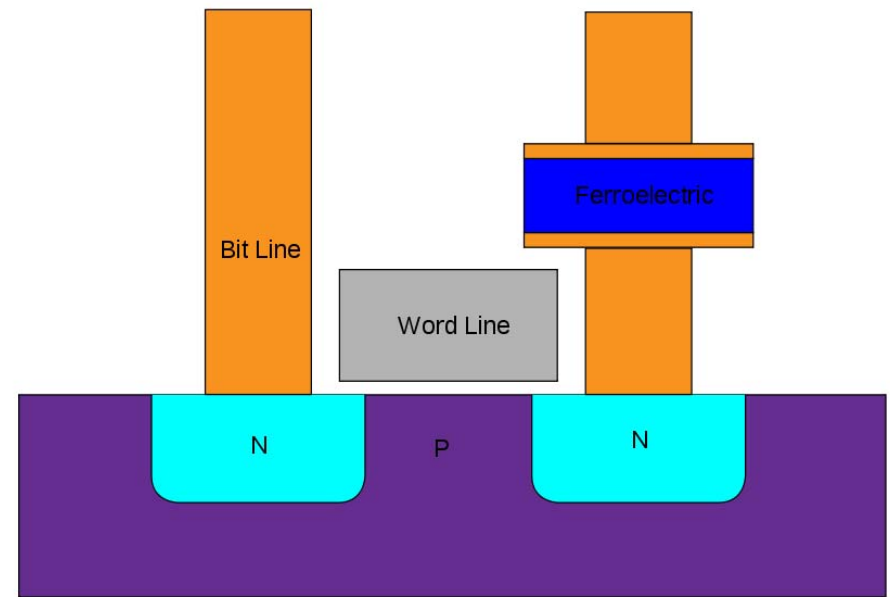
Ferroelectric RAM

FeRAM uses a Ferroelectric material like PZT to store information.

Sometimes used in smart cards.

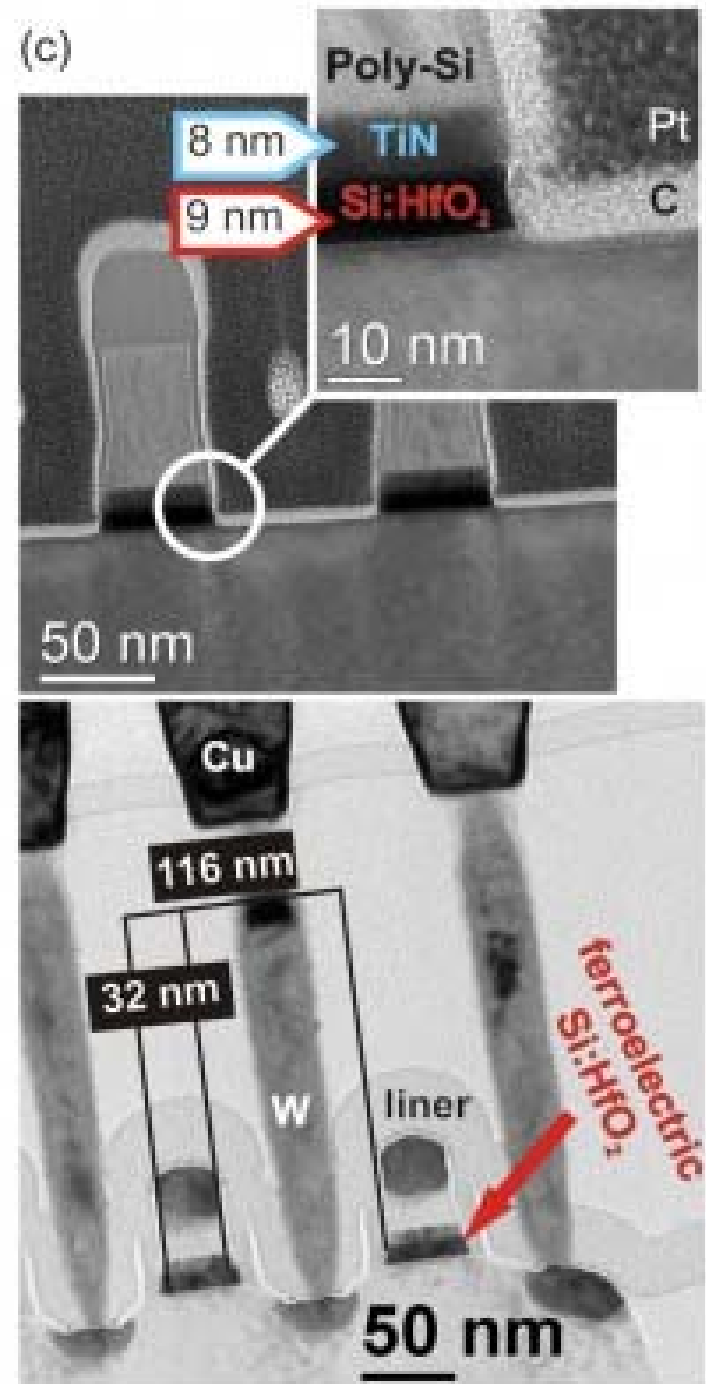
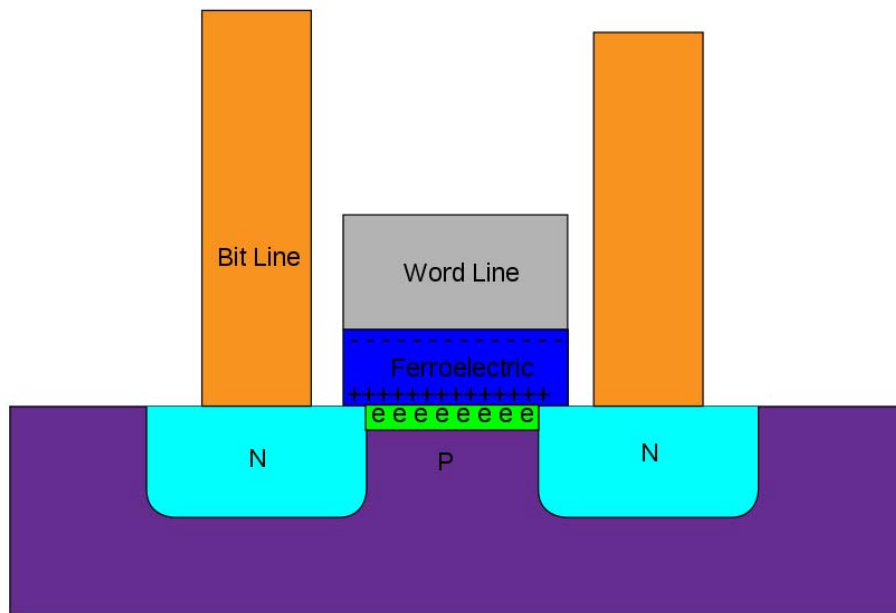


nonvolatile



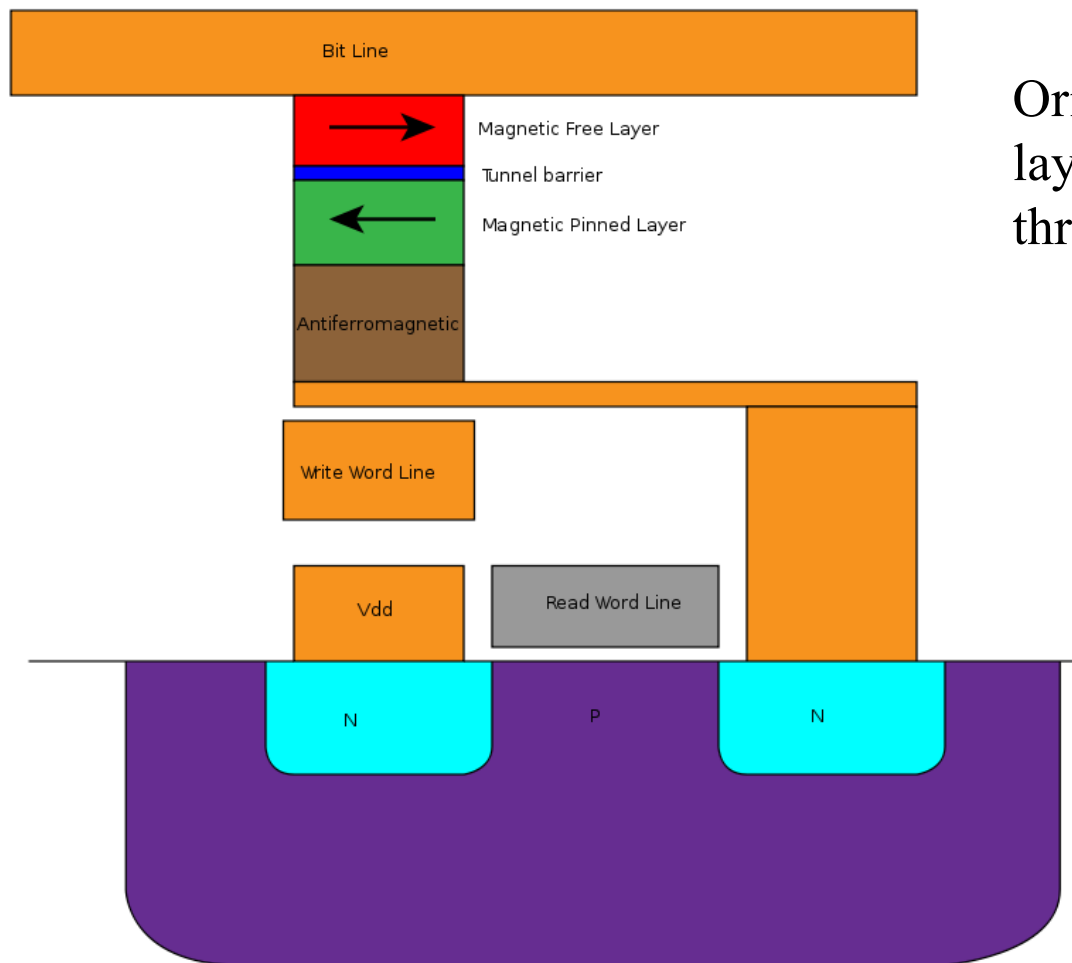
To read, try to write a 0,
if a current flows, it was a 1.

Ferroelectric RAM



Magnetic memory

In MRAM the resistance depends on whether the magnetic layers are parallel or antiparallel.

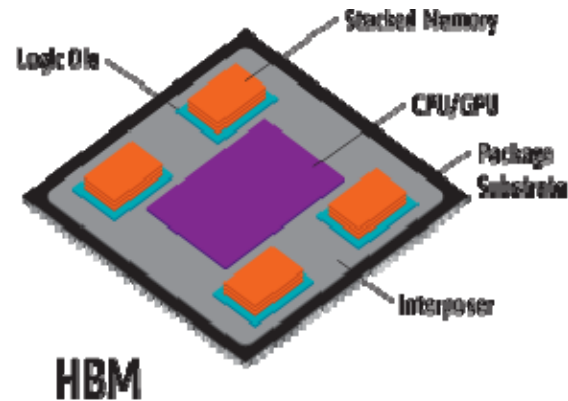
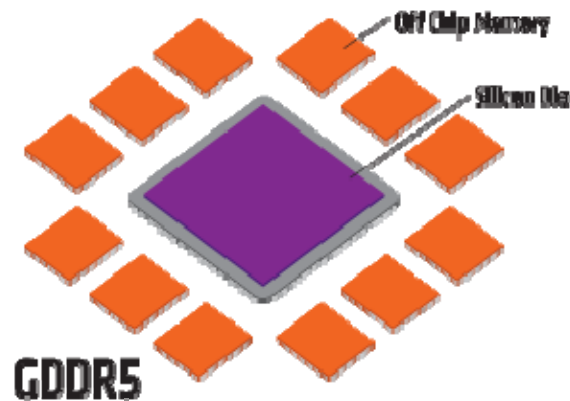
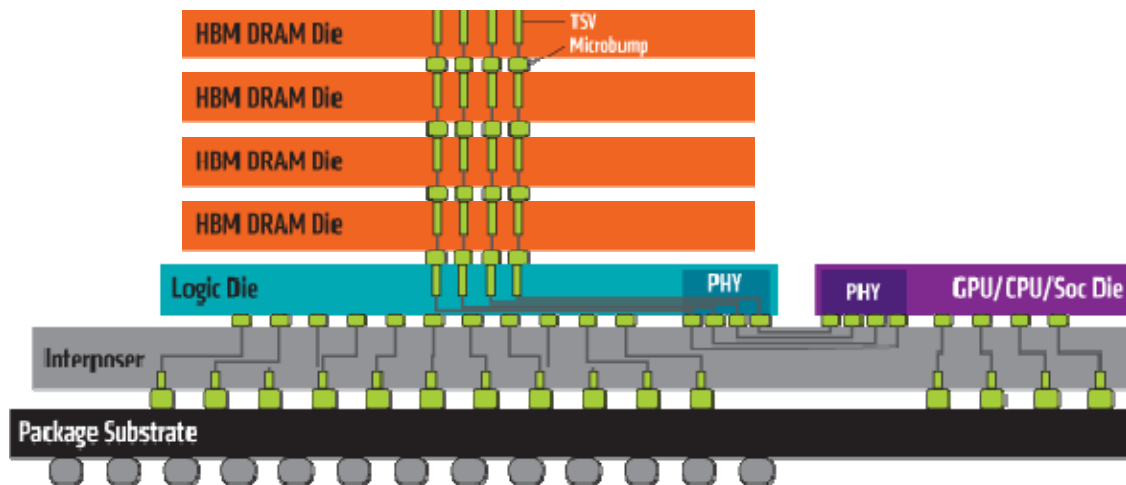


Orientaion of the magnetic free layer is set by sending a current through the bit and word lines.

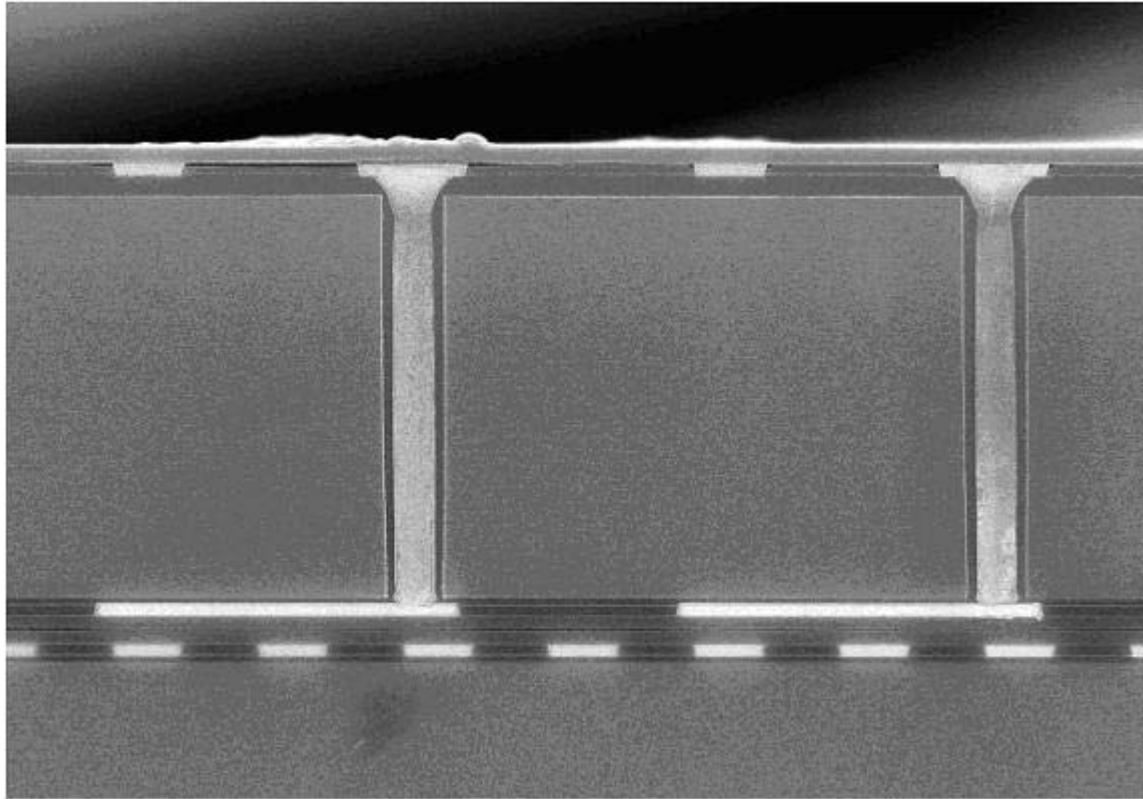
nonvolatile

High Bandwidth Memory

AMD to launch its HBM graphics cards on 16 June 2015.



Through-Silicon Via (TSV)



A vertical electrical connection (via) passing completely through a silicon wafer.

Used in 3D integration.

Bosch process

Repeat 2 processes over and over

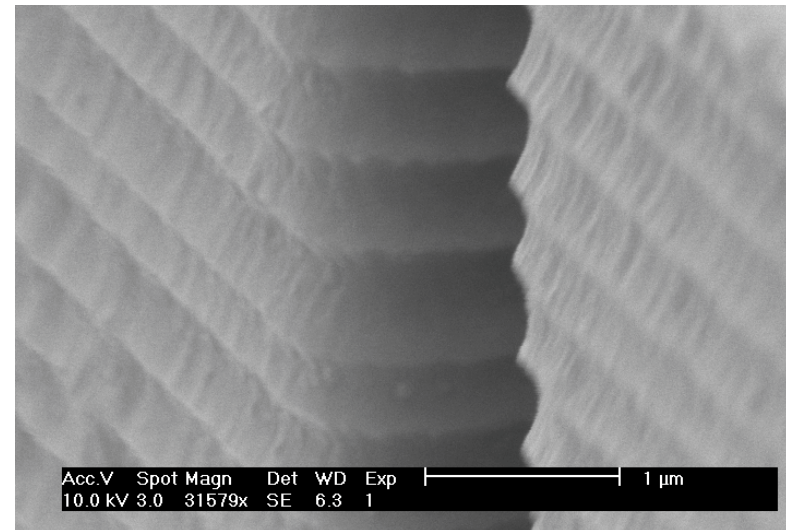
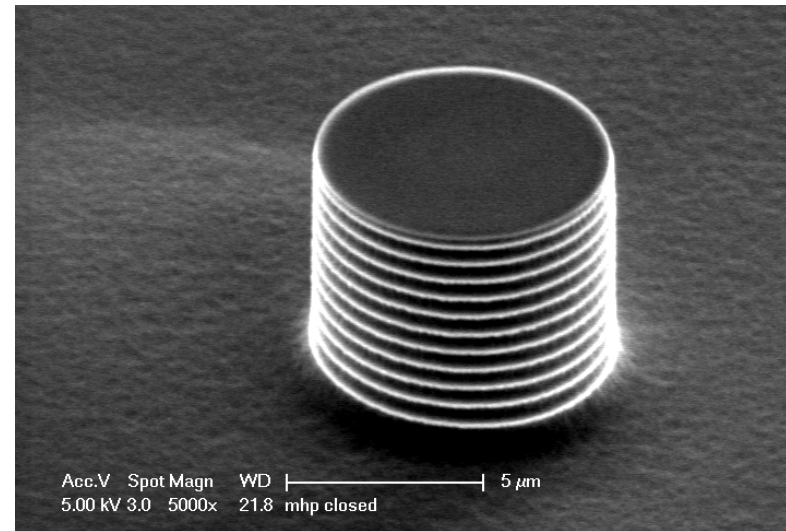
1. Etch Si with SF_6 (nearly isotropic)

2. Deposit passivation layer C_4F_8

Directional etching at the bottom breaks through the passivation layer.

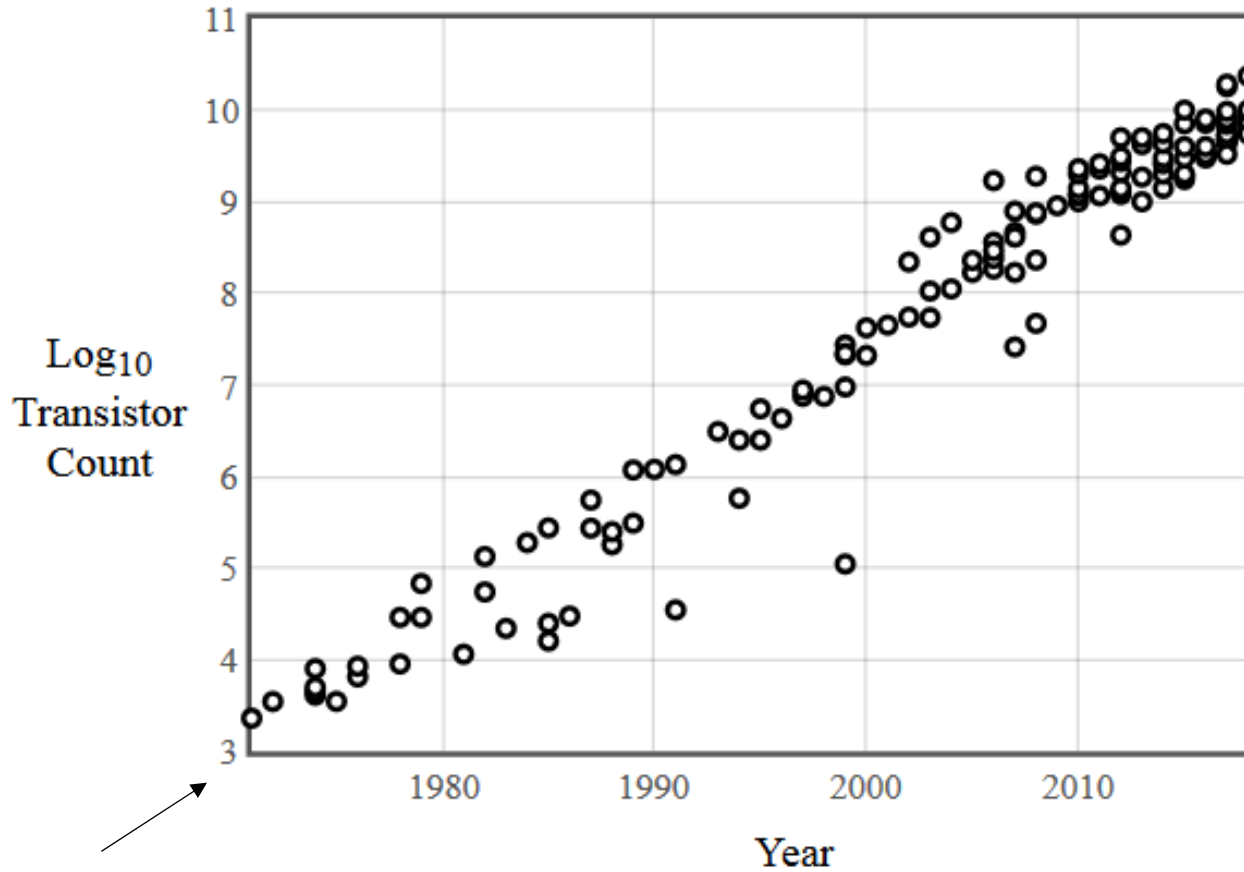
Short cycles: smooth walls

Long cycles: fast etching



http://en.wikipedia.org/wiki/Deep_reactive-ion_etching

Transistor Count 2018



Jan 1 1970

Transistor count doubles about every 2 years

https://en.wikipedia.org/wiki/Transistor_count

Miniaturization ends with CMOS

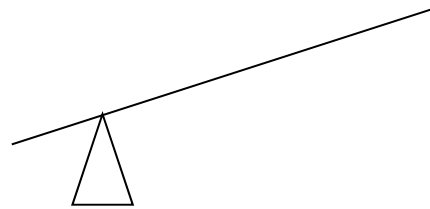
There are no technologies (single electron transistors, molecular electronics, superconducting electronics, spintronics, NEMs...) that can provide performance similar to CMOS at a **much** smaller size scale.

There are presently no transistors cheaper than silicon transistors

Candidates for orders of magnitude improvements of performance are quantum computing and molecular electronics.

Gain requires leverage

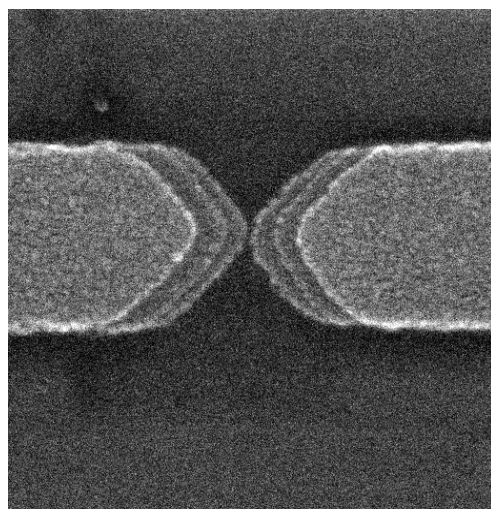
There are two lengths in an amplifier.



In CMOS the gate insulator is much thinner than the gate length.

If the short length is 1 nm, the long length is 10 nm.

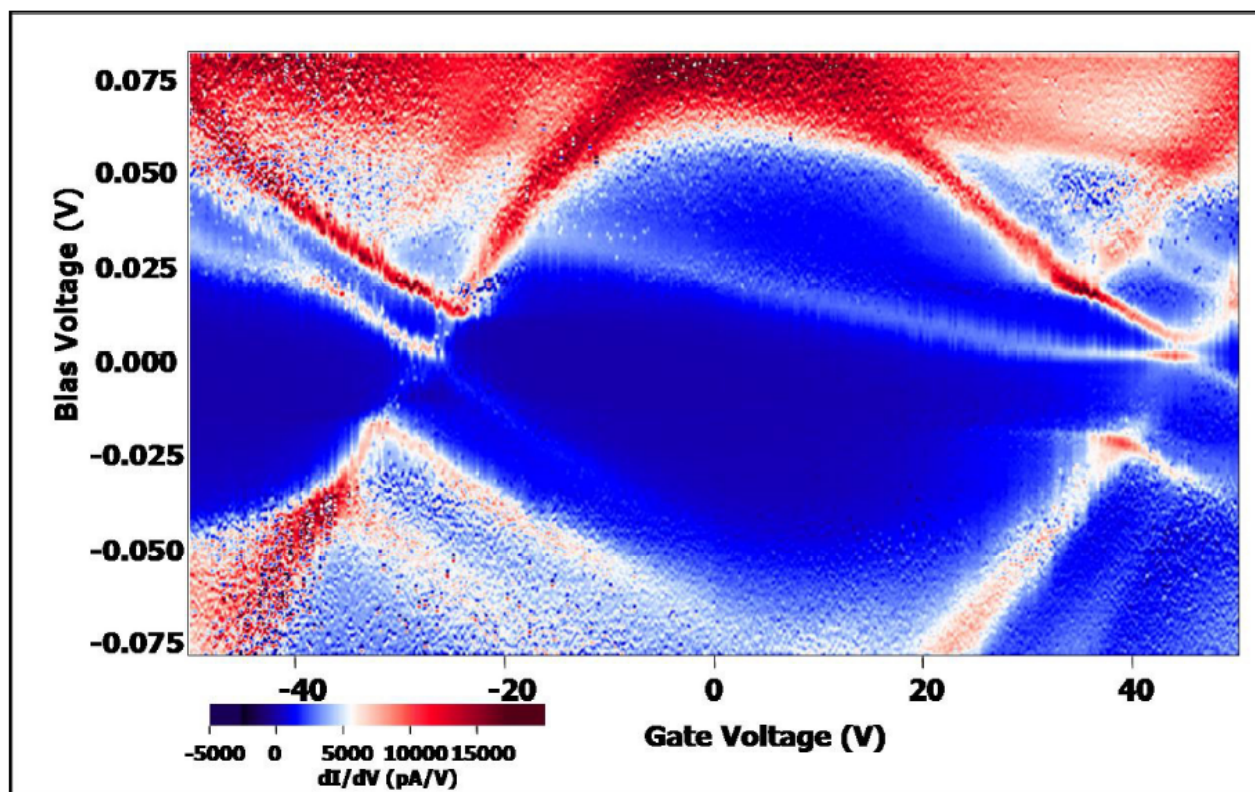
Measuring molecules



electrode 25-6

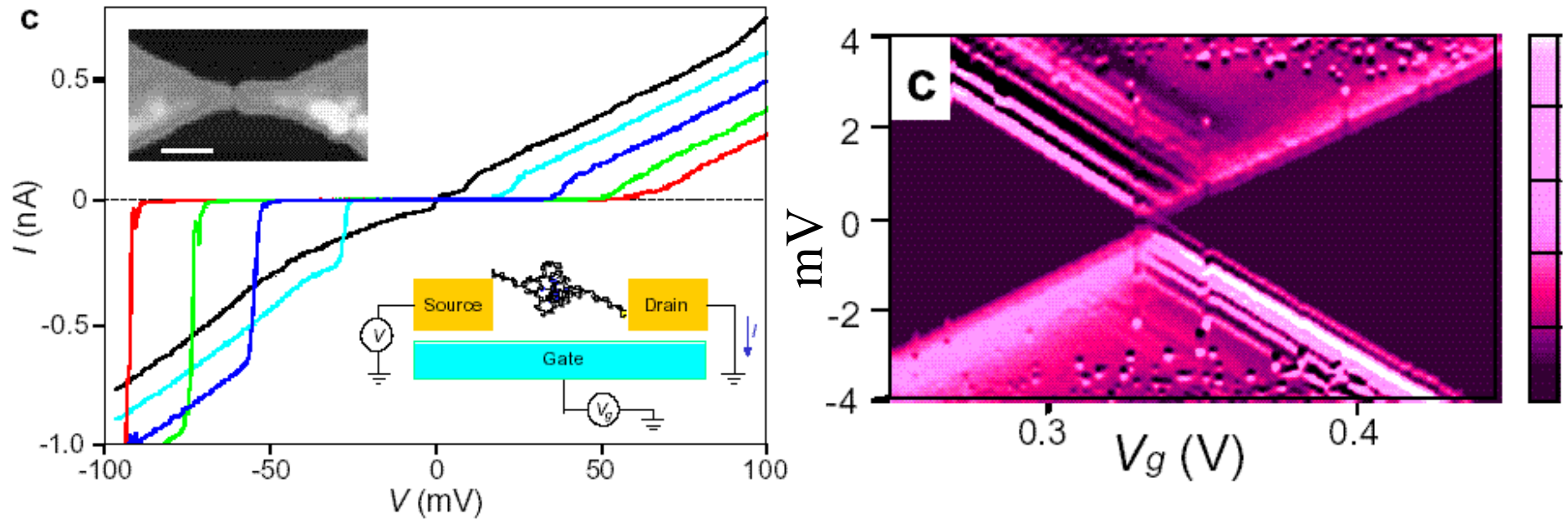
8.3μm

1,4-benzenedithiol

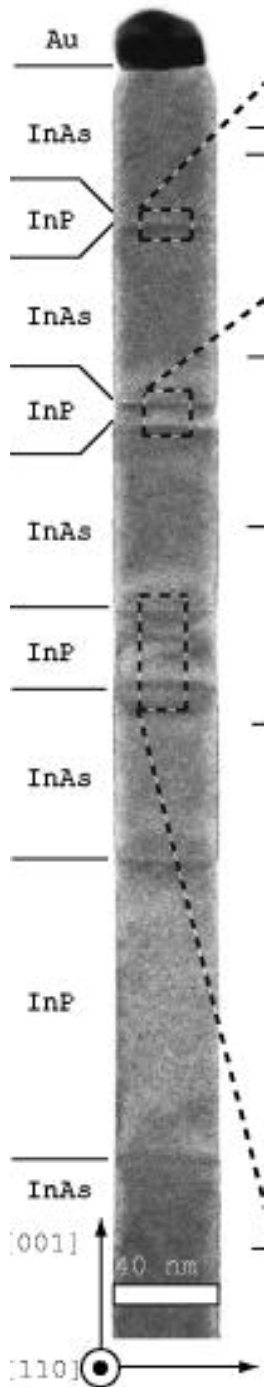


Results are unreproducible

Molecular electronics



Jiwoong Park, Abhay N. Pasupathy, Jonas I. Goldsmith, Connie Chang, Yuval Yaish, Jason R. Petta, Marie Rinkoski, James P. Sethna, Héctor D. Abruña, Paul L. McEuen, and Daniel C. Ralph, *Nature* 417 p. 722 (2002).

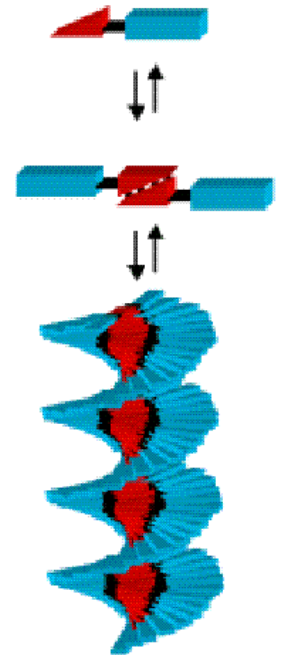
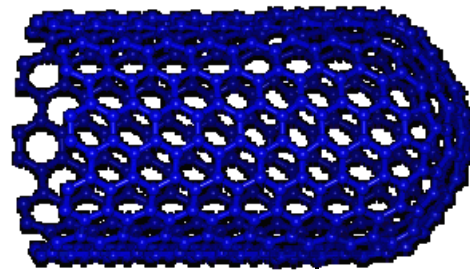


Use big 'molecules' as electronic components

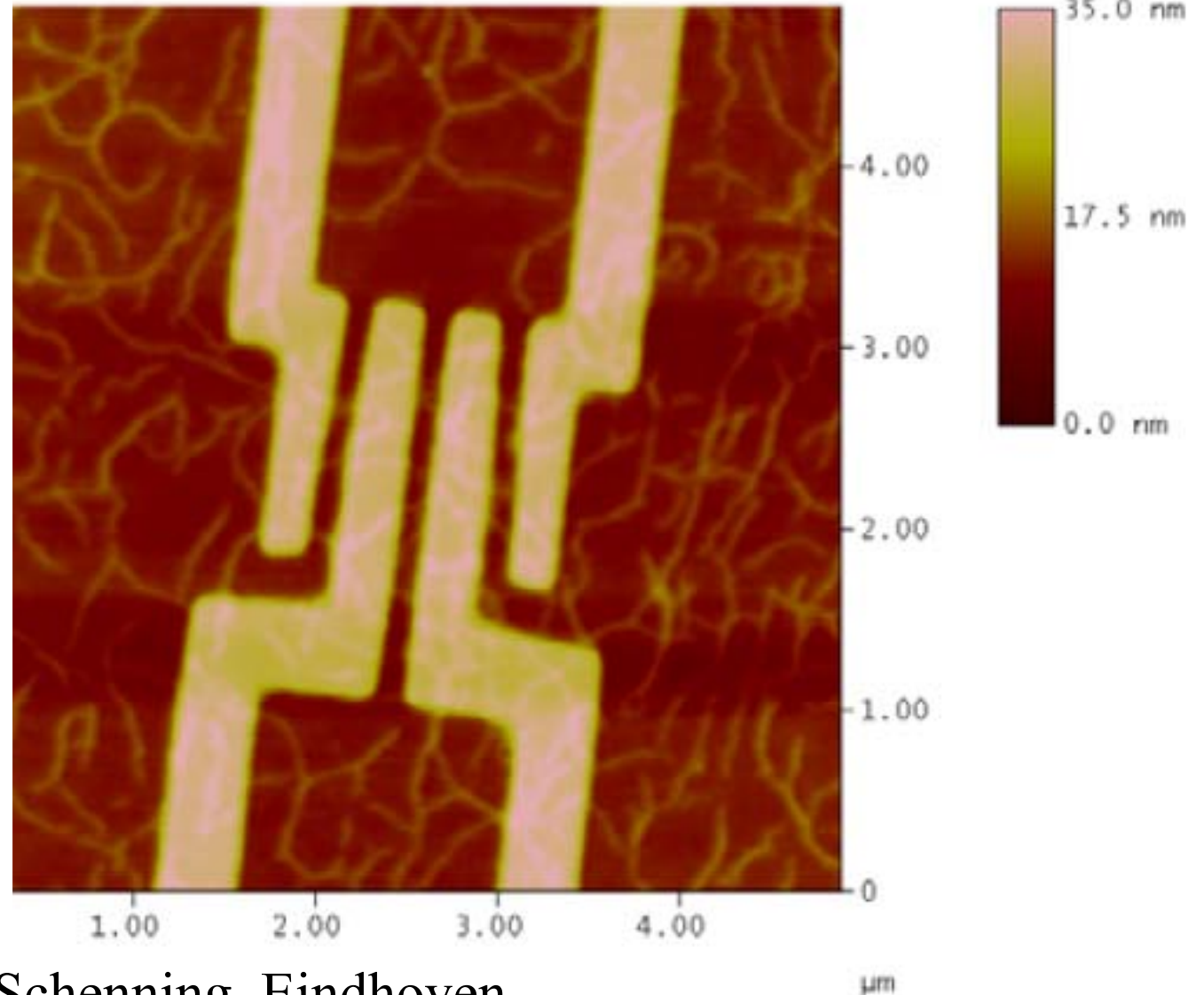
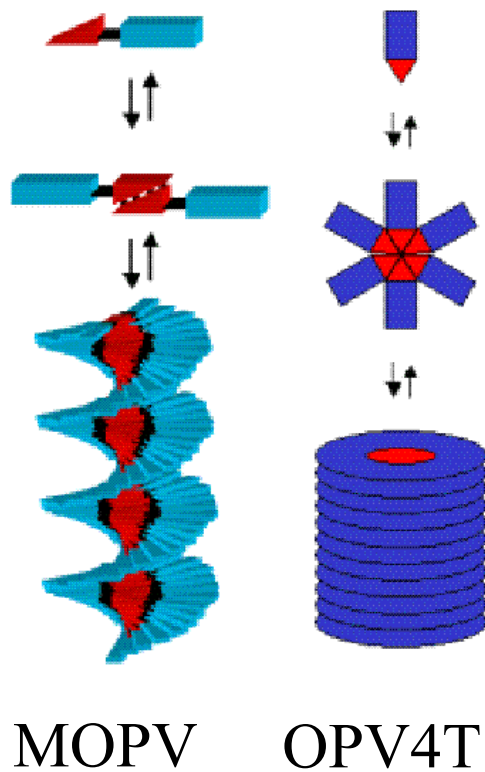
Easier to make reproducible contacts.

Imaging of individual molecular assemblies possible

Nanowires or nanocrystals of conventional semiconductors

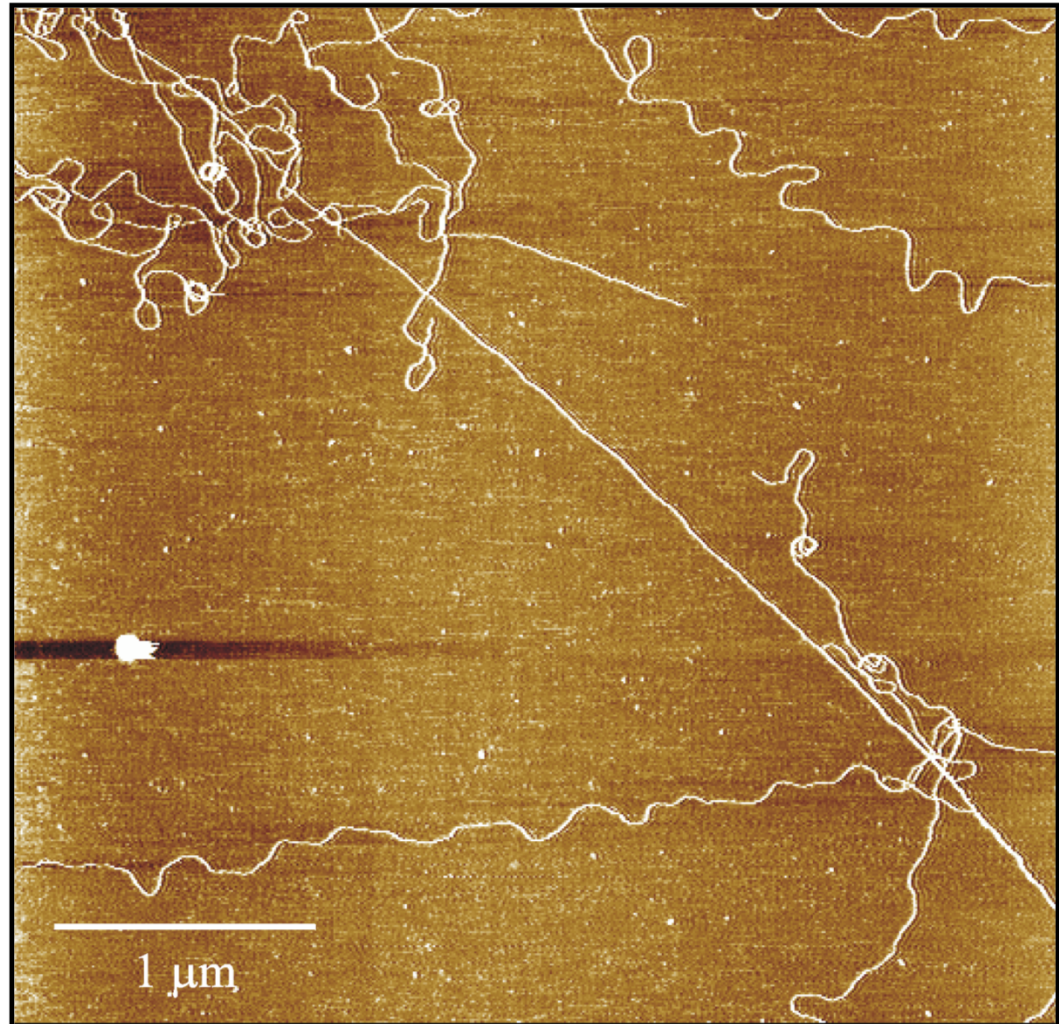
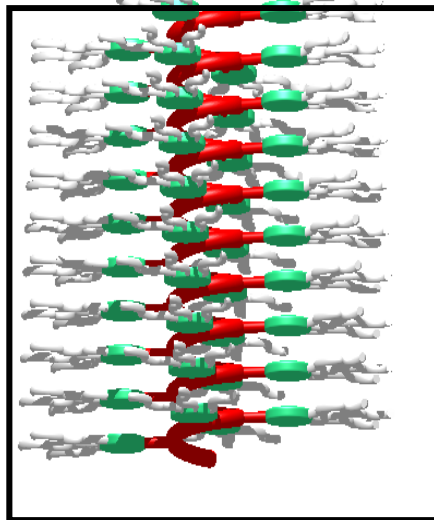
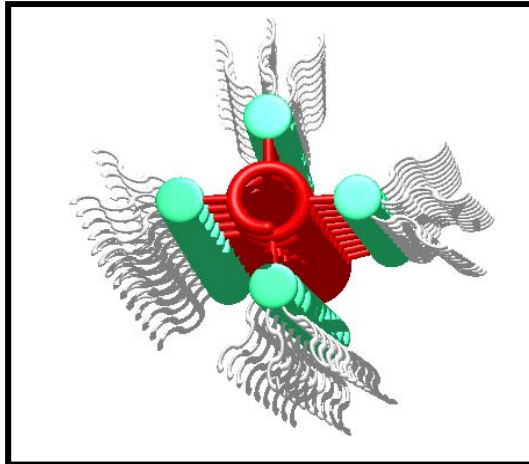


AFM image of MOPV4 fibers



Albert Schenning, Eindhoven

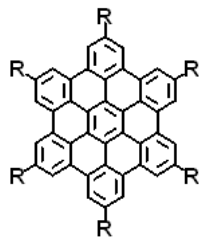
Using templates for self-assembly



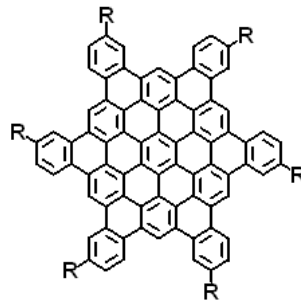
Alan Rowan, Nijmegen

Phthalocyanine Polyisocyanides

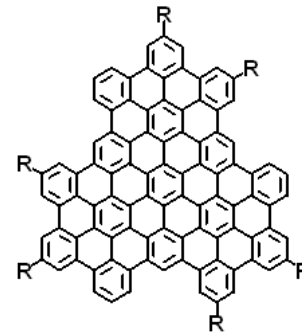
hexabenzocoronenes



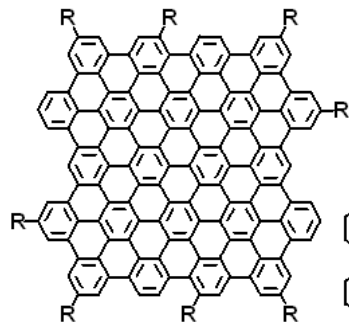
C42 (HBC)



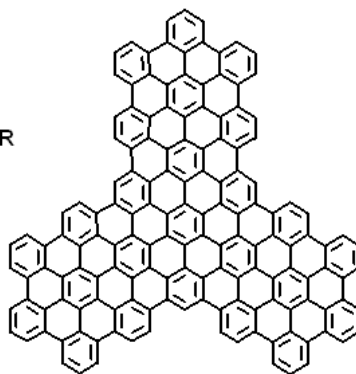
C78



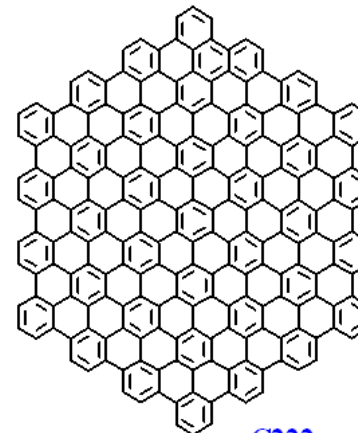
C96



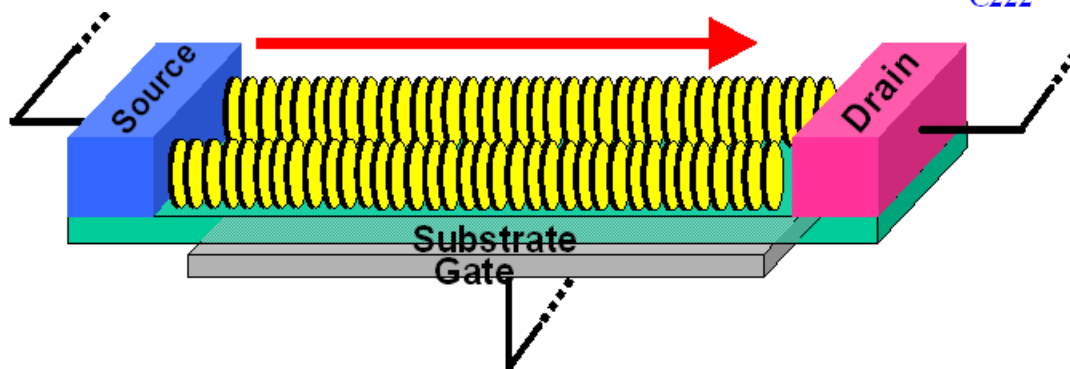
C132



C150

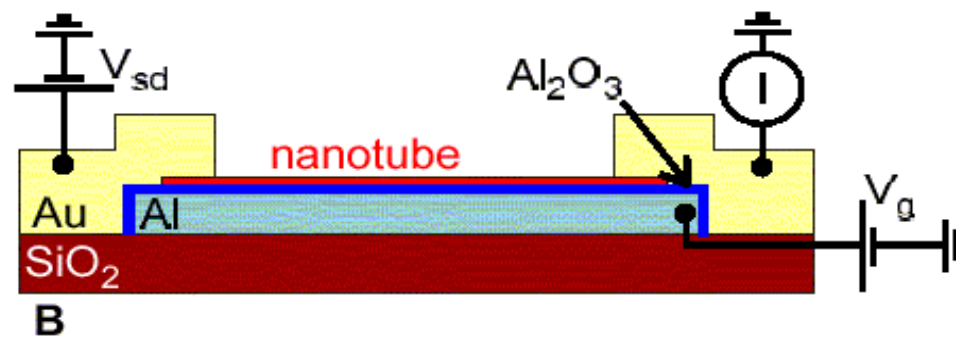
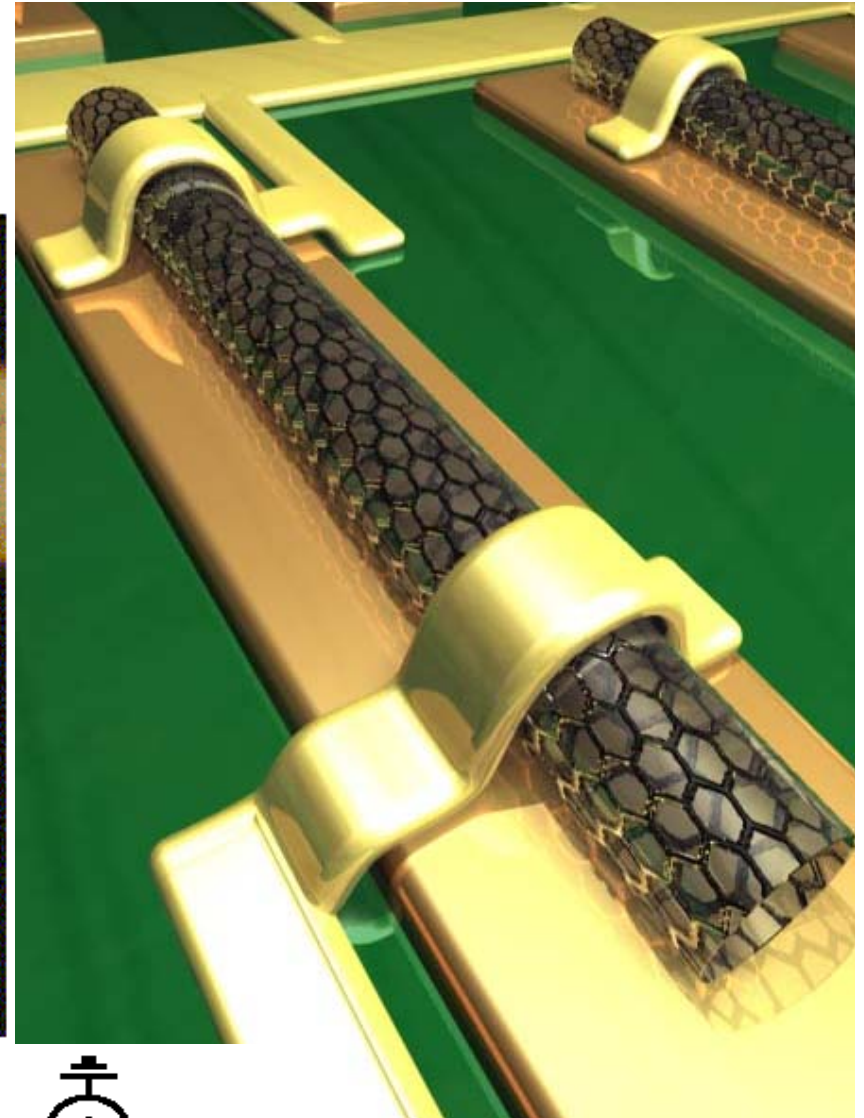
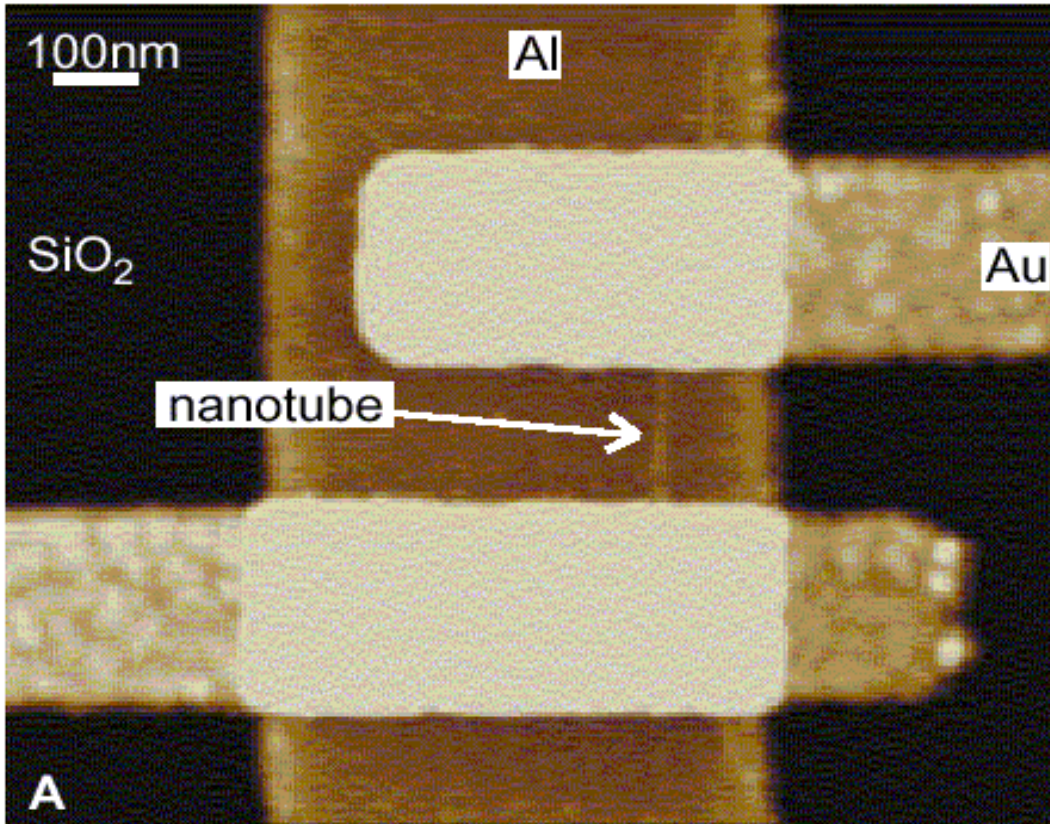


C222



Müllen, Mainz

Carbon nanotube transistors



After Miniaturization

Increasing the level of self-assembly in a fabrication process will replace miniaturization as a guiding principle for making cheaper circuits.

Molecular transistors must be large molecules. Transistors will have dimensions of ~ 10 nm

Low current drive of molecular devices will mean they will have to be put in parallel.

Lighting panels and solar cells will be the first self-assembled devices.

Organic microprocessor



A modern computer has the processing power of a mosquito brain.