1. Physics of Semiconductor Devices

Oct. 2, 2018

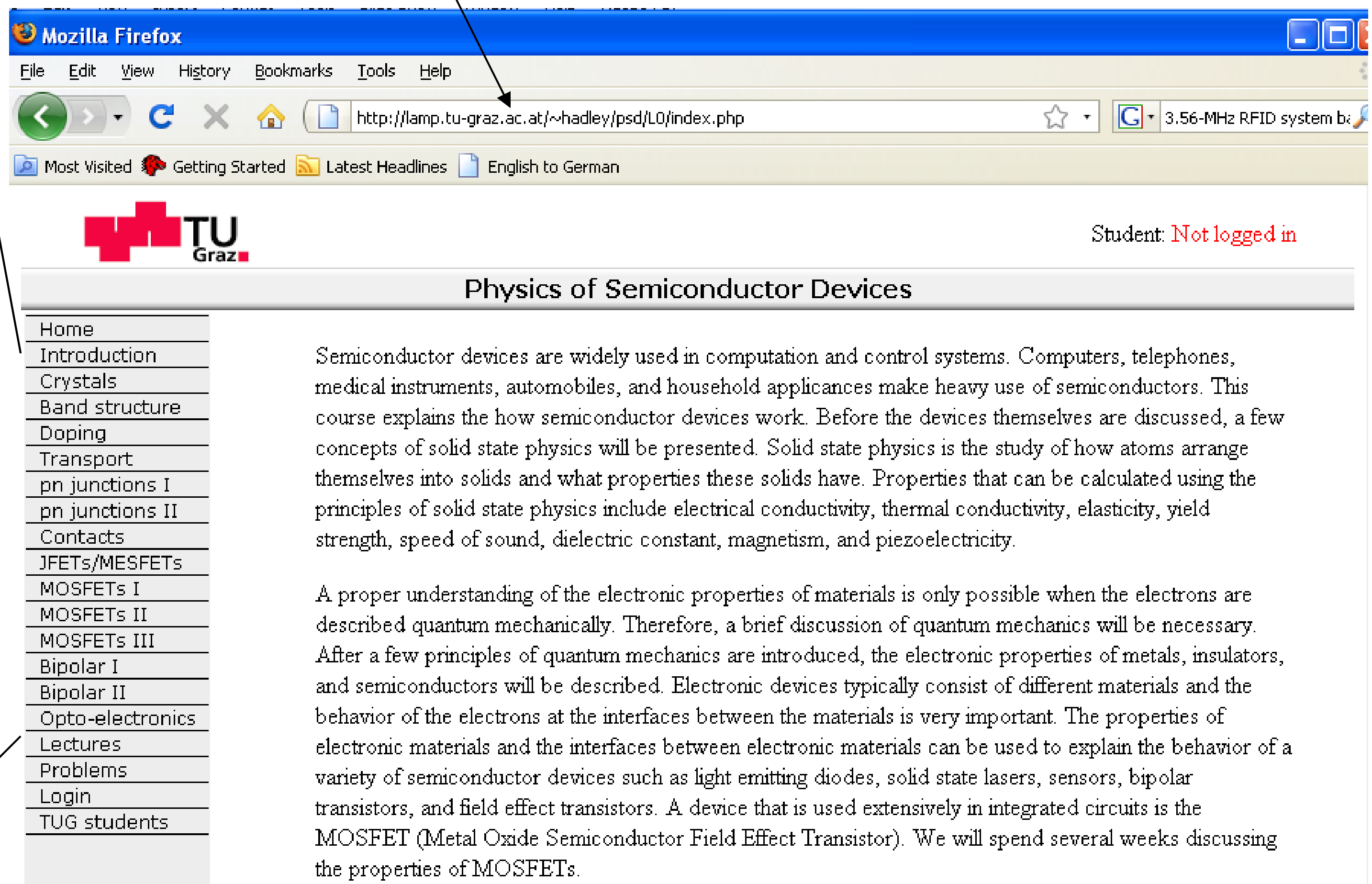
Physics of Semiconductor Devices

- Diodes, solid state lasers, transistors
- Computing, communications
- Controllers: vacuum cleaners, coffee makers, etc.
- Transportation, autonomous driving, electric cars
- Efficient lighting, solar cells, displays
- Lasers

Peter Hadley

- Home
- Outline
- Introduction
- Crystals
- Intrinsic Semiconductors
- Extrinsic Semiconductors
- Transport
- pn junctions
- Contacts
- JFETs/MESFETs
- MOSFETs
- Bipolar transistors
- Opto-electronics
- Lectures
- Exam questions
- Making presentations
- TUG students
- Student projects

http://www.if.tugraz.at/psd.html



Before the lecture, the slides will be uploaded to:
https://cloud.tugraz.at/index.php/s/NjuEDwhj1R5CBGT

Examination

1 hour written exam

One page of handwritten notes

1 Contribution to improve the course

Chapter summaries

Solutions to exam questions

Simulations

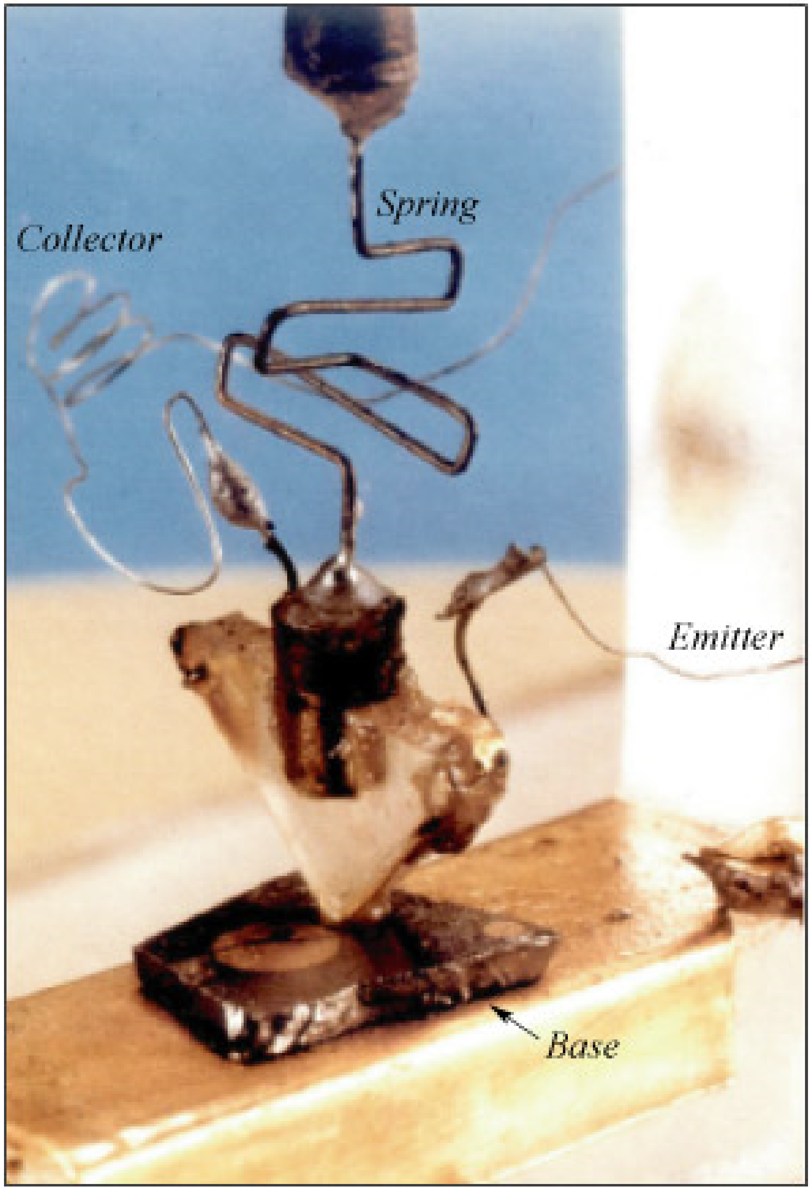
Videos

Oral exam

The first point contact transistor

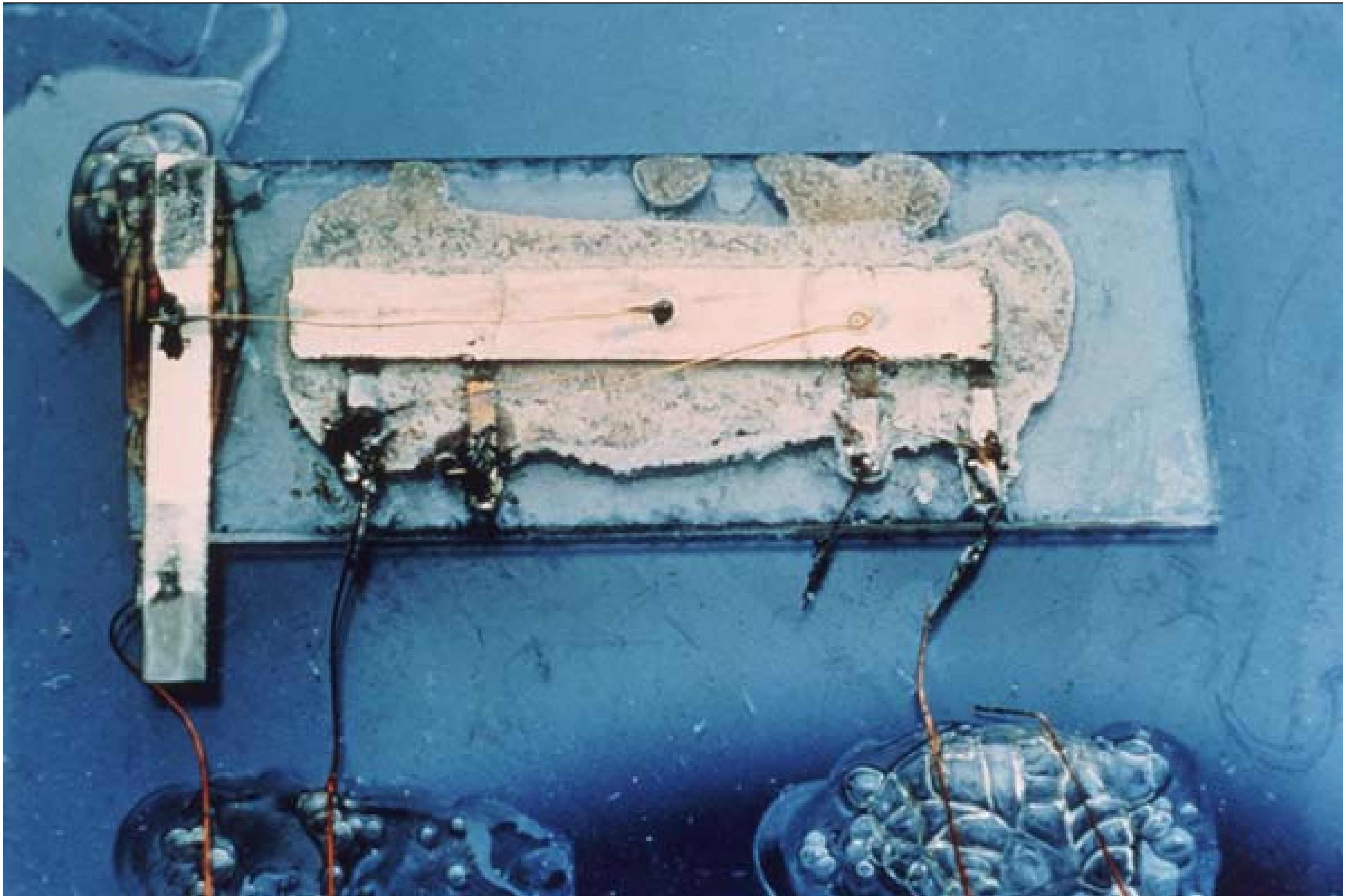
William Shockley, John Bardeen, and Walter Brattain

Bell Laboratories, Murray Hill, New Jersey (1947)

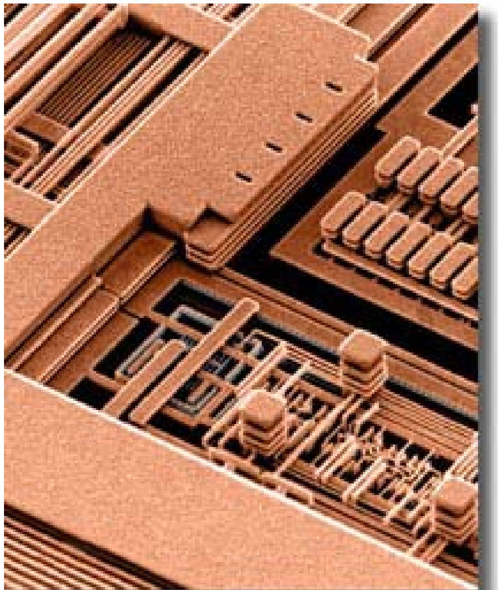


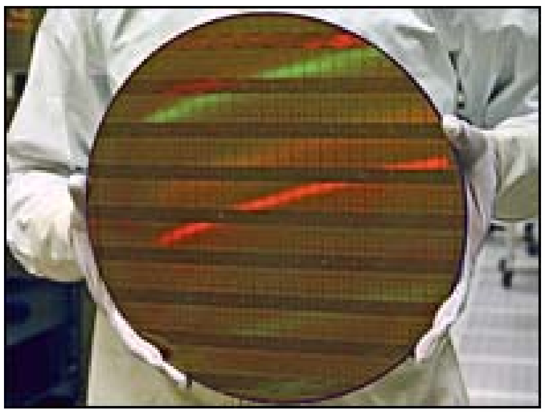
Bardeen Brattain

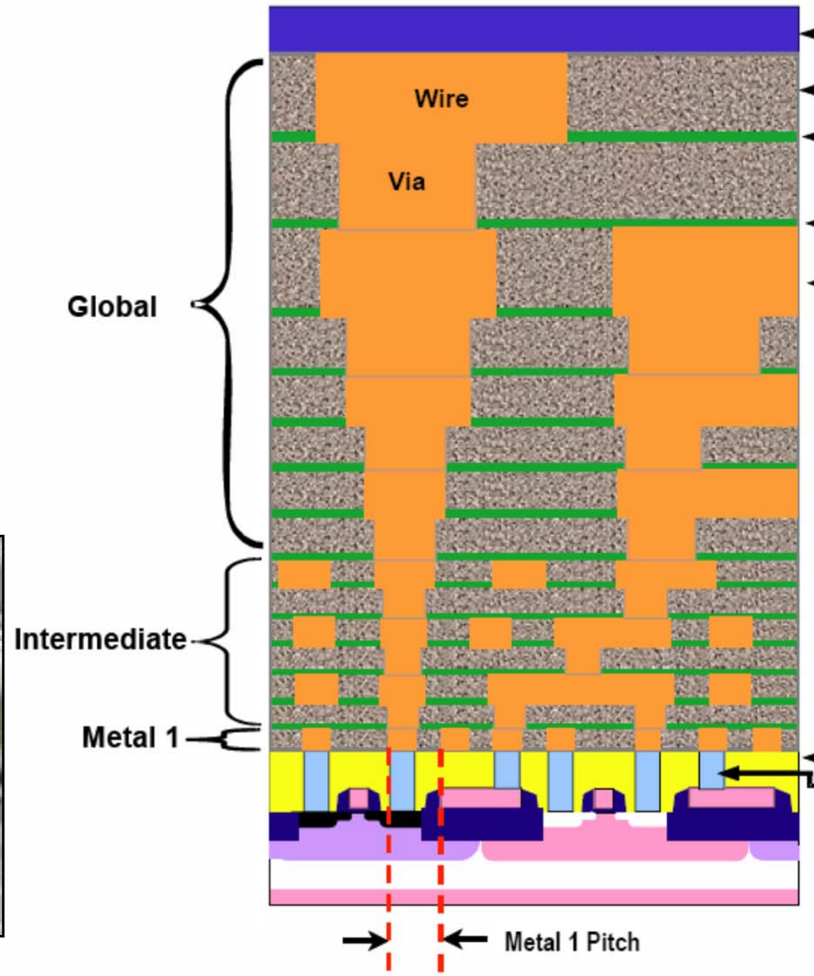
Shockley



Jack Kilby's first integrated circuit 1958







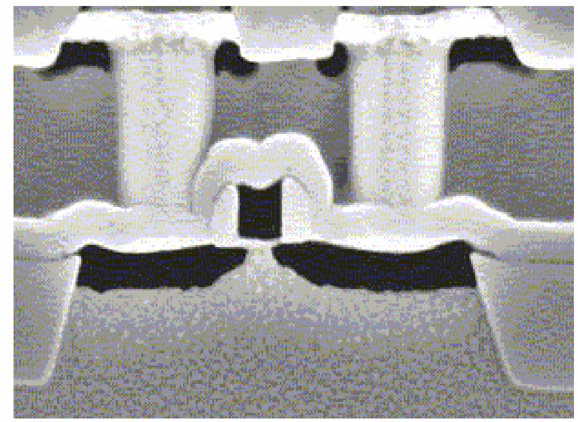
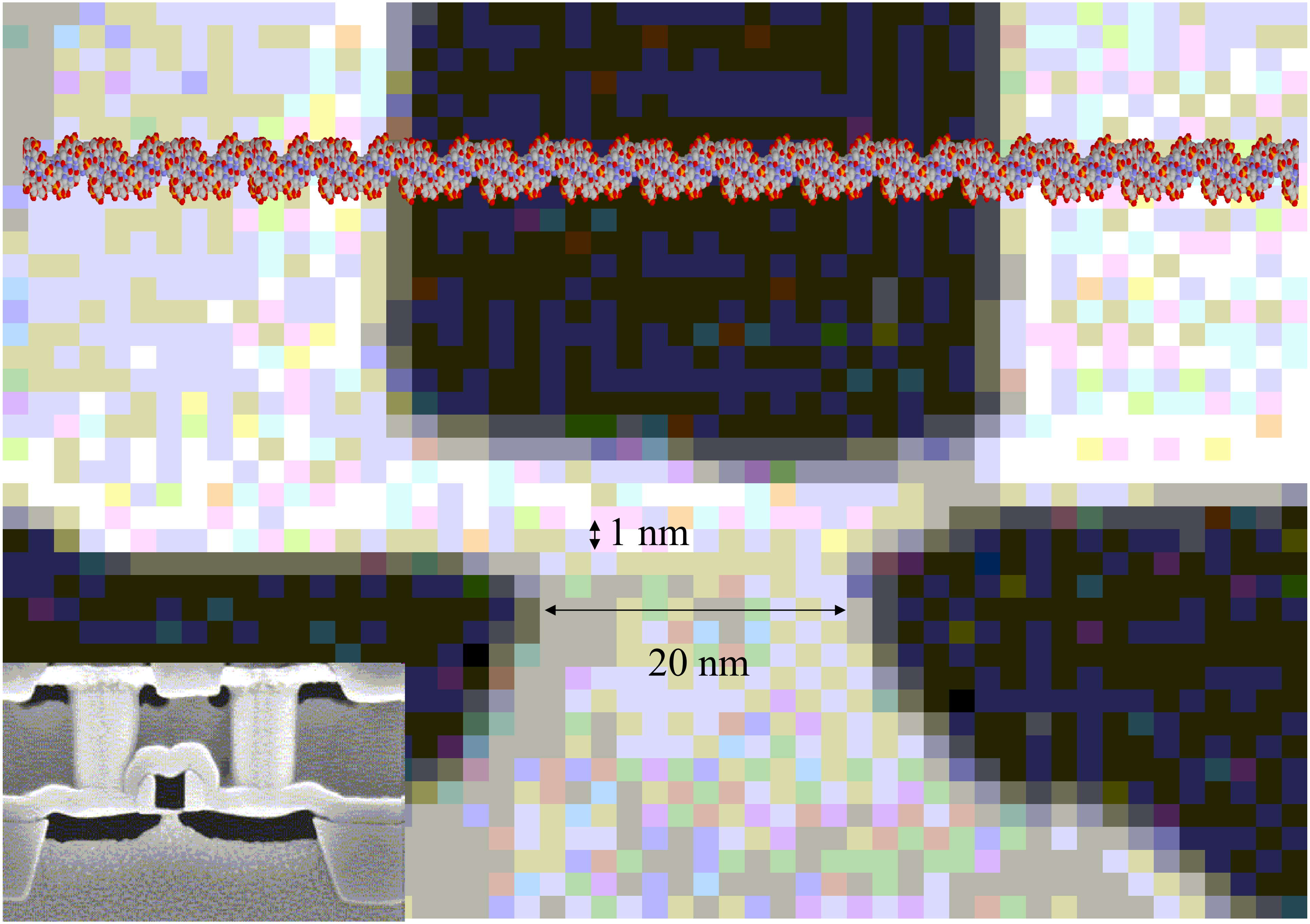


Table PIDS2a High-performance (HP) Logic Technology Requirements

	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028
node	"16/14"		"11/10"		"8/7"		"6/5"		"4/3"		"3/2.5"		"2/1.5"		"1/0.75"	
metal 1/2 pitch	40	32	32	28.3	25.3	22.5	20.0	17.9	15.9	14.2	12.6	11.3	10.0	8.9	8	7.1
gate length	20	18	16.7	15.2	13.9	12.7	11.6	10.6	9.7	8.8	8.0	7.3	6.7	6.1	5.6	5.1



1 nm
20 nm

INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS™

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INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS

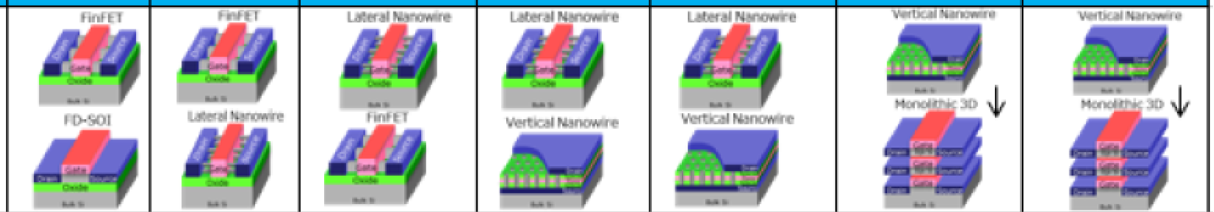
INTERNATIONAL
ROADMAP
FOR
DEVICES AND SYSTEMS

2017 EDITION

EXECUTIVE SUMMARY

1. Application Benchmarking (AB)
2. Systems and Architectures (SA)
3. Outside System Connectivity (OSC)
4. More Moore (MM) ⬅
5. Beyond CMOS (BC) ⬅
6. Packaging Integration (PI)
7. Factory Integration (FI)
8. Lithography (L)
9. Emerging Research Materials (ERM) ⬅
10. Yield Enhancement (YE)
11. Metrology (M)
12. Environment, Safety, Health (ESH/S), and Sustainability

YEAR OF PRODUCTION	2017	2019	2021	2024	2027	2030	2033
	P54M36	P48M28	P42M24	P36M21	P32M14	P32M14T2	P32M14T4
Logic industry "Node Range" Labeling (nm)	"10"	"7"	"5"	"3"	"2.1"	"1.5"	"1.0"
IDM-Foundry node labeling	i10-f7	i7-f5	i5-f3	i3-f2.1	i2.1-f1.5	i1.5-f1.0	i1.0-f0.7
Logic device structure options	finFET FDSOI	finFET LGAA	LGAA finFET	LGAA VGAA	LGAA VGAA	VGAA, LGAA 3DVLSI	VGAA, LGAA 3DVLSI
Logic device mainstream device	finFET	finFET	LGAA	LGAA	LGAA	VGAA	VGAA
DEVICE STRUCTURES							

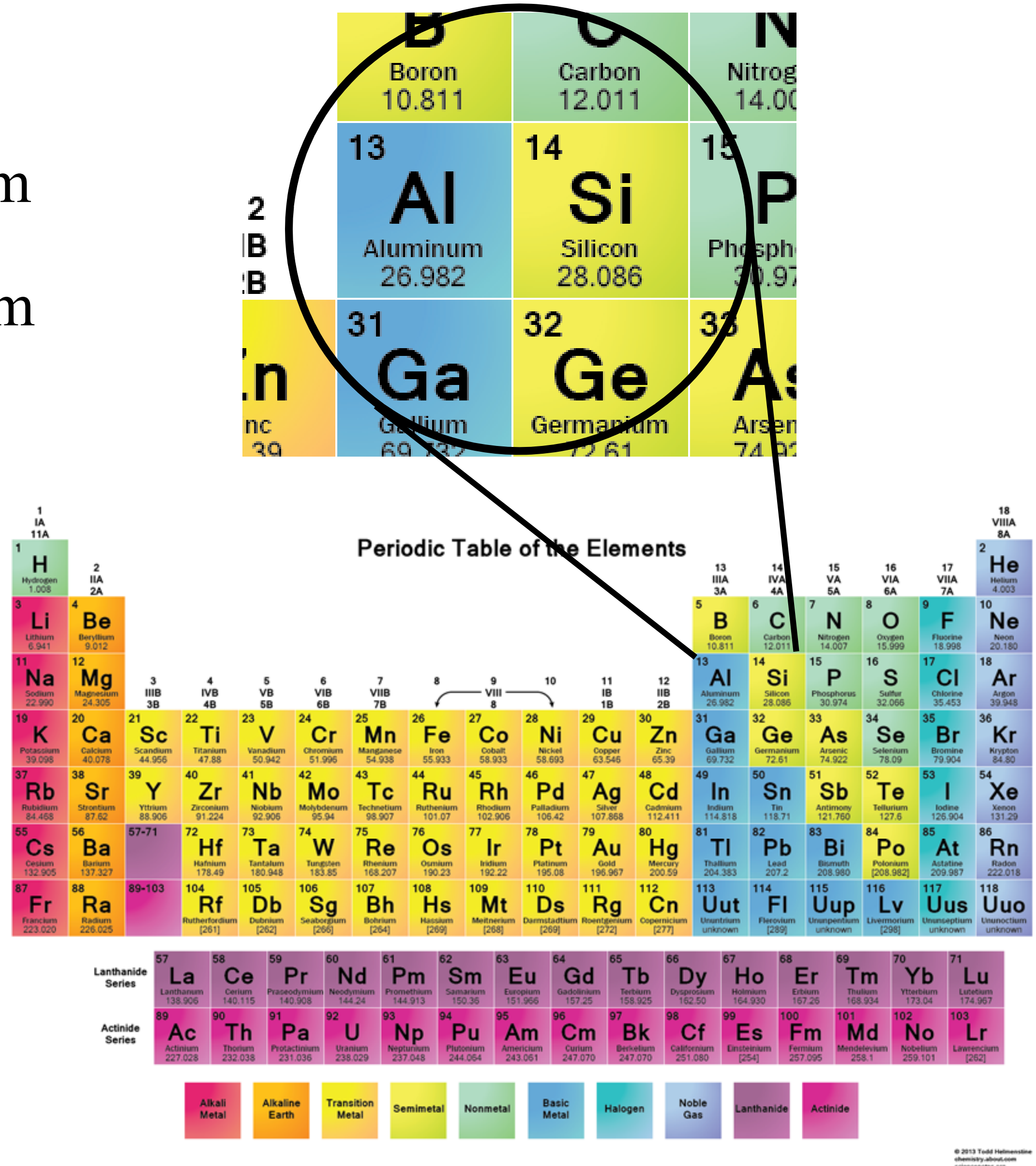


YEAR OF PRODUCTION	2017	2019	2021	2024	2027	2030	2033
LOGIC DEVICE GROUND RULES							
MPU/SoC Metalx ½ Pitch (nm)[1,2]	18.0	14.0	12.0	10.5	7.0	7.0	7.0
MPU/SoC Metal0/1 ½ Pitch (nm)	18.0	14.0	12.0	10.5	7.0	7.0	7.0
Contacted poly half pitch (nm)	27.0	24.0	21.0	18.0	16.0	16.0	16.0
L_g: Physical Gate Length for HP Logic (nm) [3]	20	18	16	14	12	12	12
L_g: Physical Gate Length for LP Logic (nm)	22	20	18	16	14	14	14
Channel overlap ratio - two-sided	0.80	0.80	0.80	0.80	0.80	0.80	0.80
Spacer width (nm)	8	7	6	5	5	5	5
Contact CD (nm) - finFET, LGAA	18	16	14	12	10		
Contact CD (nm) - VGAA						12	12
Device architecture key ground rules							
FinFET Fin Half-pitch (nm)	16.0	14.0					
FinFET Fin Width (nm)	8.0	7.0					
FinFET Fin Height (nm)	45	50					
Footprint drive efficiency - finFET	3.06	3.82					
Lateral GAA lateral half-pitch (nm)			12.0	10.5	9.0		
Lateral GAA vertical half-pitch (nm)			8.0	8.0	8.0		
Lateral GAA (nanosheet) thickness (nm)			5.0	5.0	5.0		
Lateral GAA (nanosheet) minimum width (nm)			7.0	7.0	6.0		
Number of vertically stacked nanosheets			3	4	5		
Device height (nm)			47	63	79		
Footprint drive efficiency - lateral GAA			3.00	4.57	6.11		
Vertical GAA lateral half-pitch (nm)						7.0	7.0
Vertical GAA width (nm)						6.0	6.0
Contact-gate enclosure (nm)						2.0	2.0
Footprint drive efficiency - vertical GAA						1.7	1.7
Defice effective width (nm)	98.0	107.0	72.0	96.0	110.0	24.0	24.0
Device lateral half pitch (nm)	16.0	14.0	12.0	10.5	9.0	7.0	7.0
Device height (nm)	45.0	50.0	47.0	63.0	79.0	24.0	24.0
Minimum device width (fin, nanosheet) or diameter (nm)	8.0	7.0	7.0	7.0	6.0	6.0	6.0

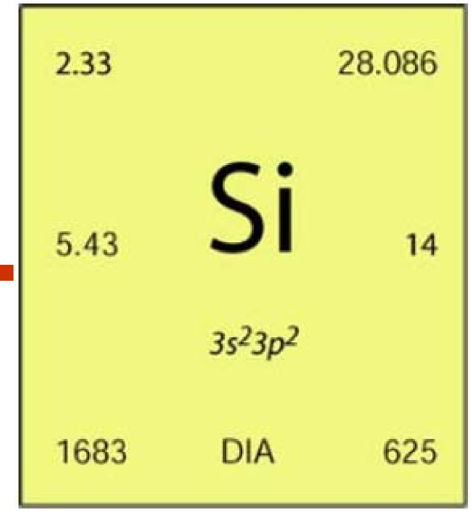
Conductivity

Al: $\sigma = 3.5 \times 10^{7}\ 1/\Omega\cdot m$

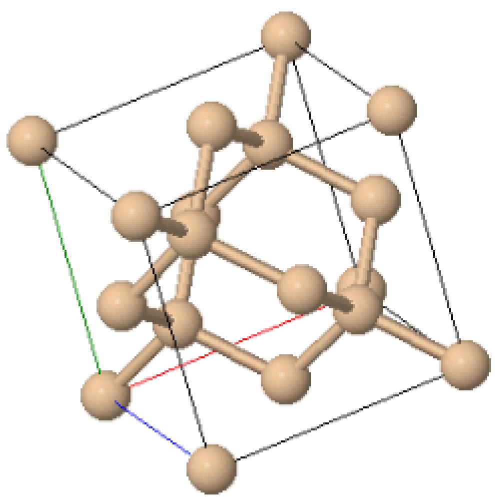
Si: $\sigma = 4.3 \times 10^{-4}\ 1/\Omega\cdot m$



Silicon



• Important semiconducting material
• 2nd most common element on earths crust (rocks, sand, glass, concrete)
• Often doped with other elements
• Oxide SiO_2 is a good insulator

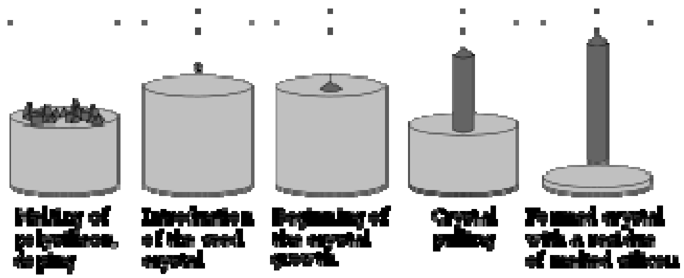


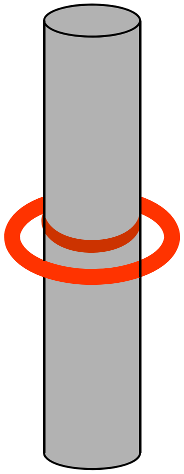
silicon crystal = diamond crystal structure

Silicon

Large (2 m) single crystals are grown

Czochralski process



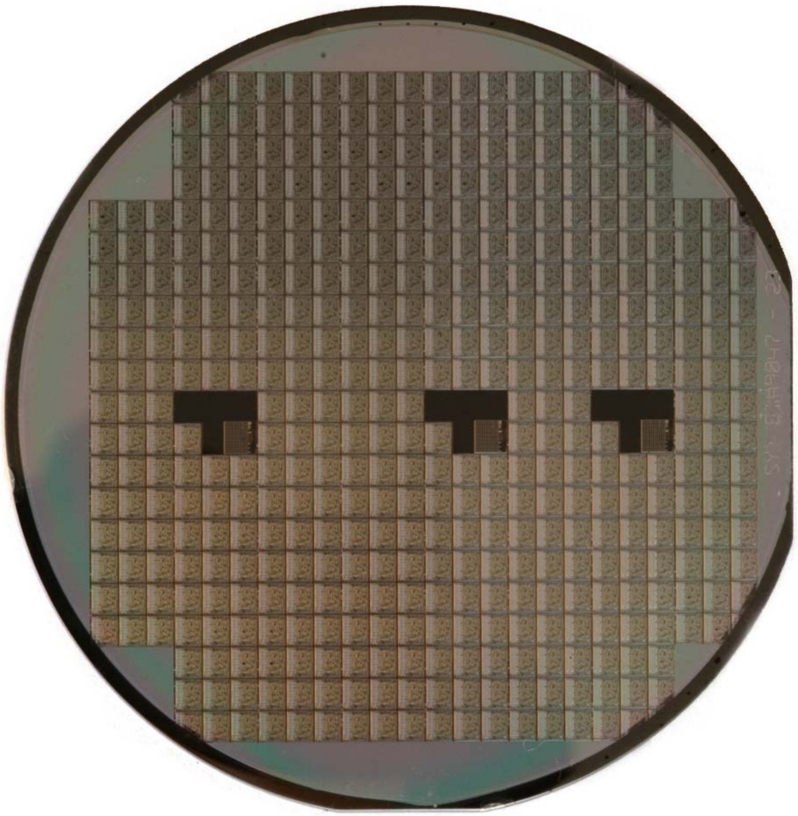


Float zone

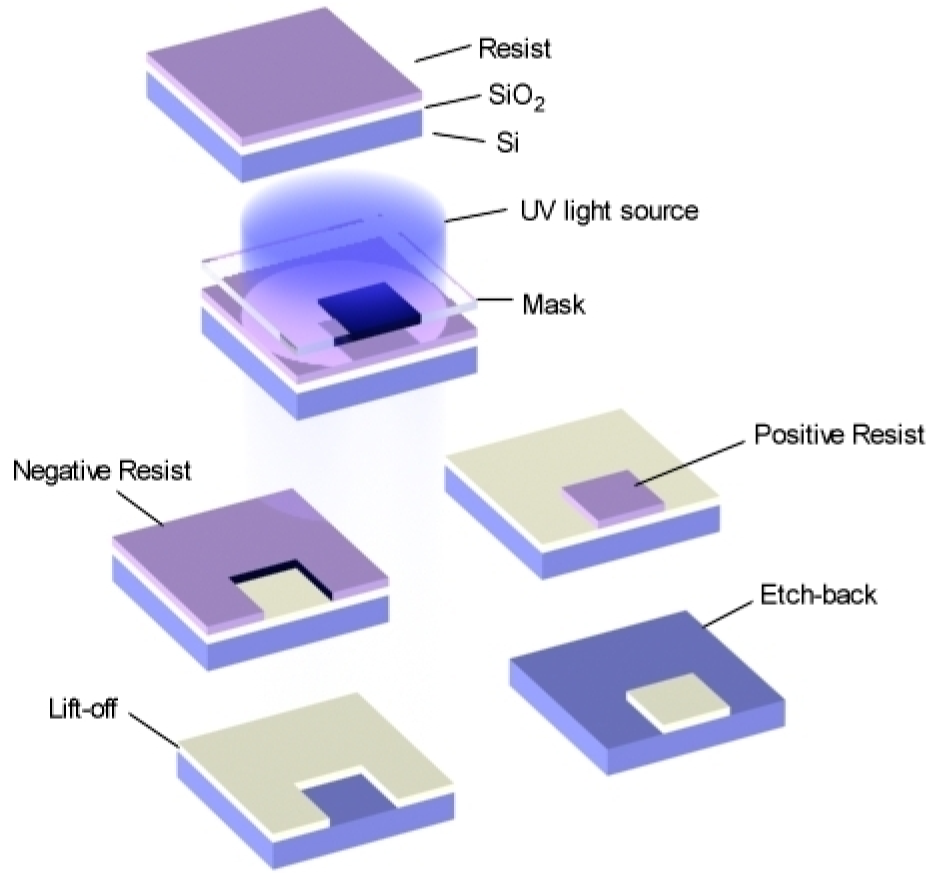
http://en.wikipedia.org/wiki/Czochralski_process

Silicon wafers

50 μm - 0.5 mm thick



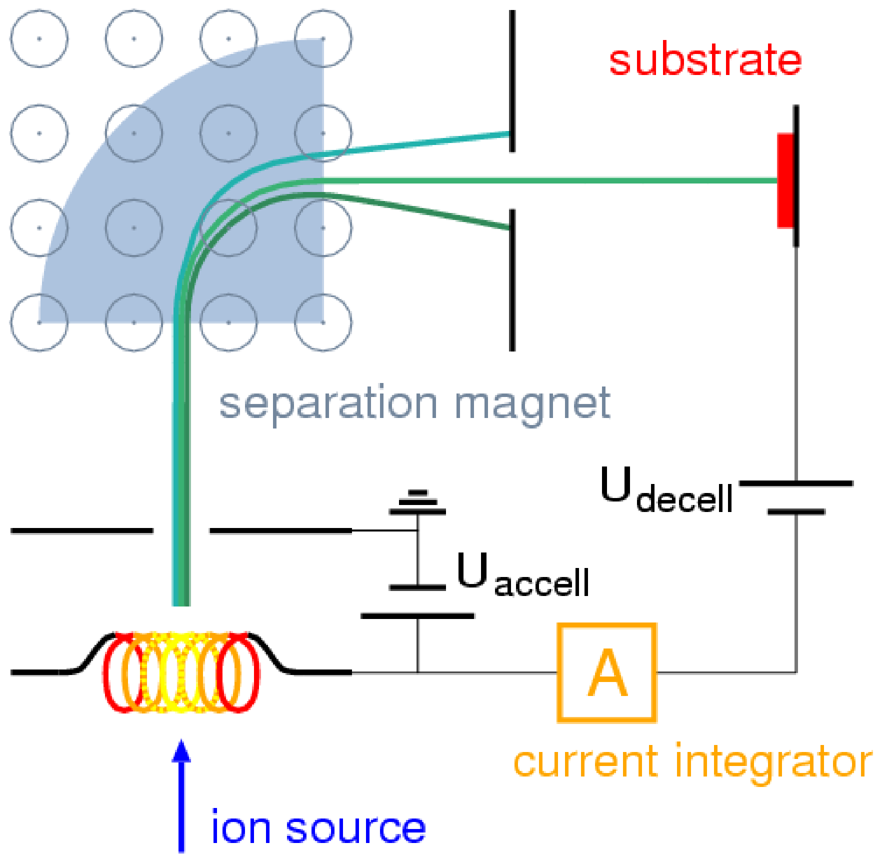
Photolithography



http://britneyspears.ac/physics/fabrication/photolithography.htm

http://cleanroom.byu.edu/lithography.parts/Lithography.html

Ion implantation



Implant at 7º to avoid channeling

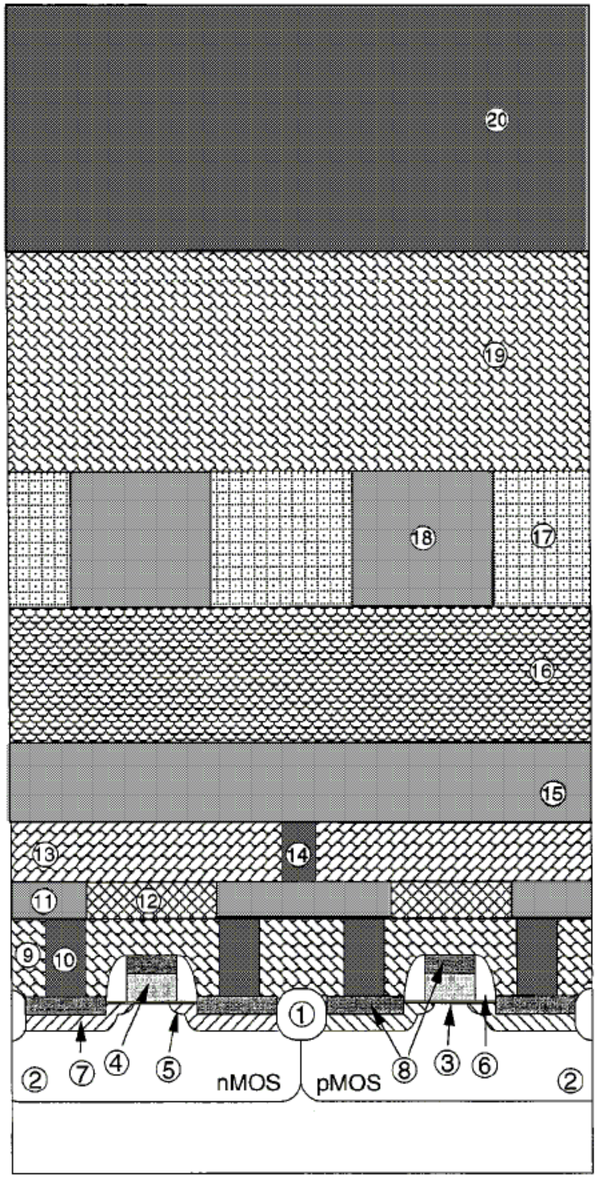
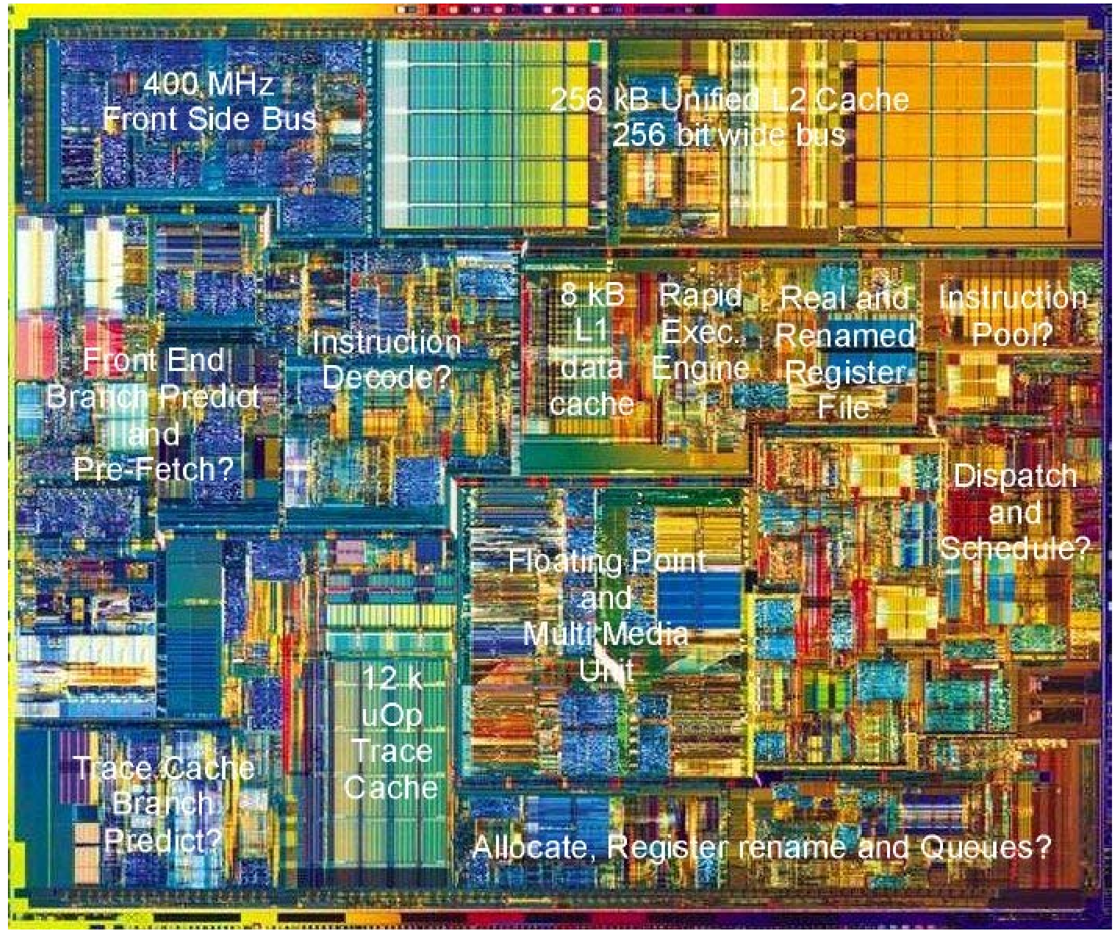
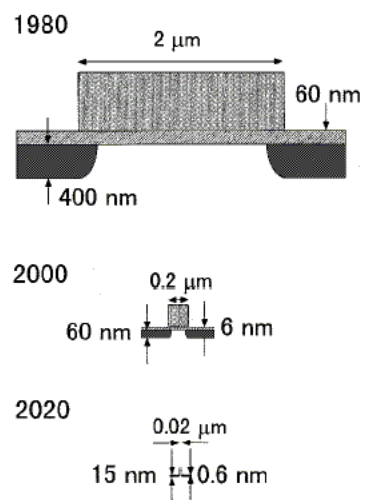


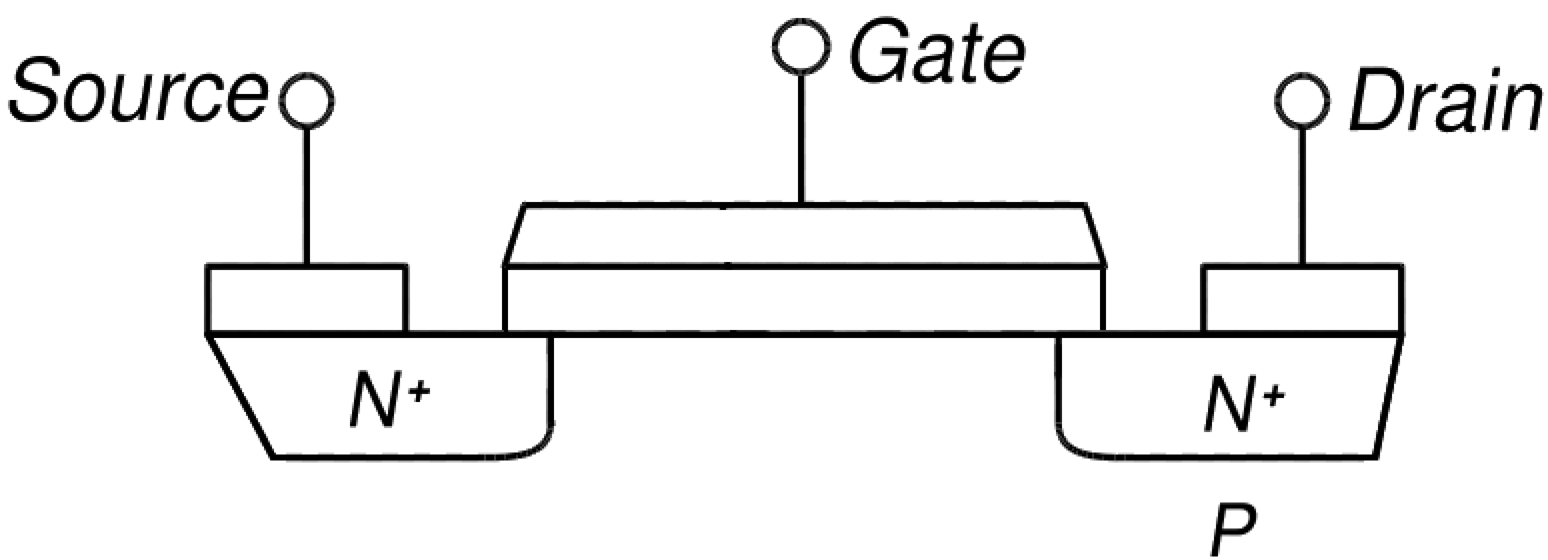
Fig. 2 Schematic cross section of present CMOS FETs with multilayered wiring.





MOSFET

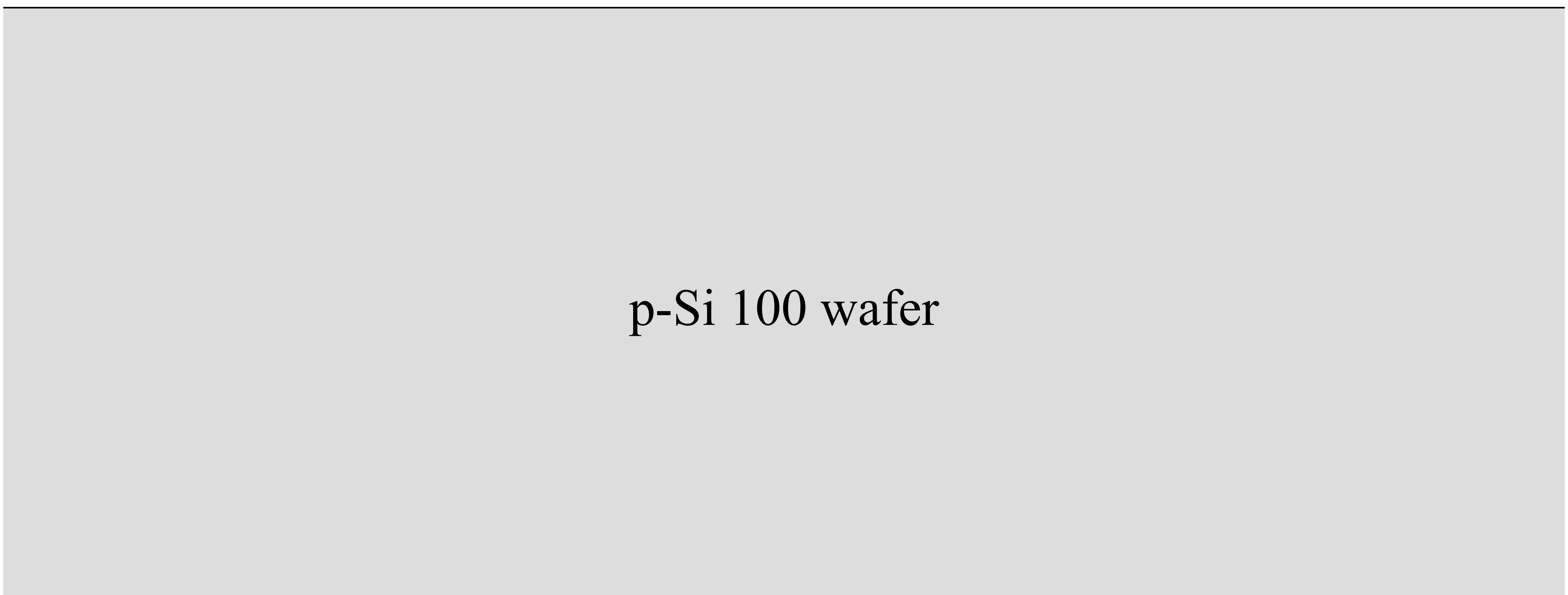
Metal Oxide Semiconductor Field Effect Transistor



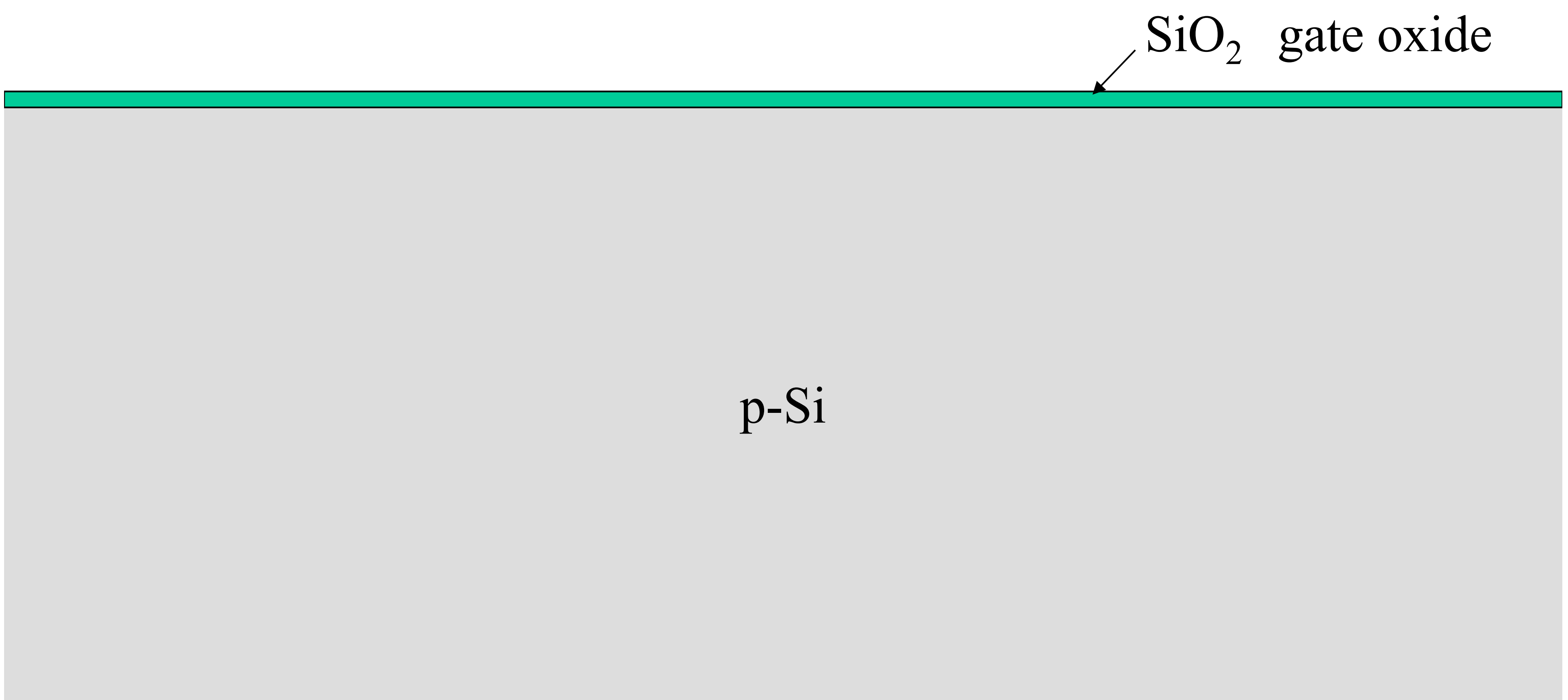
functions as a switch
~ 1 billion /chip

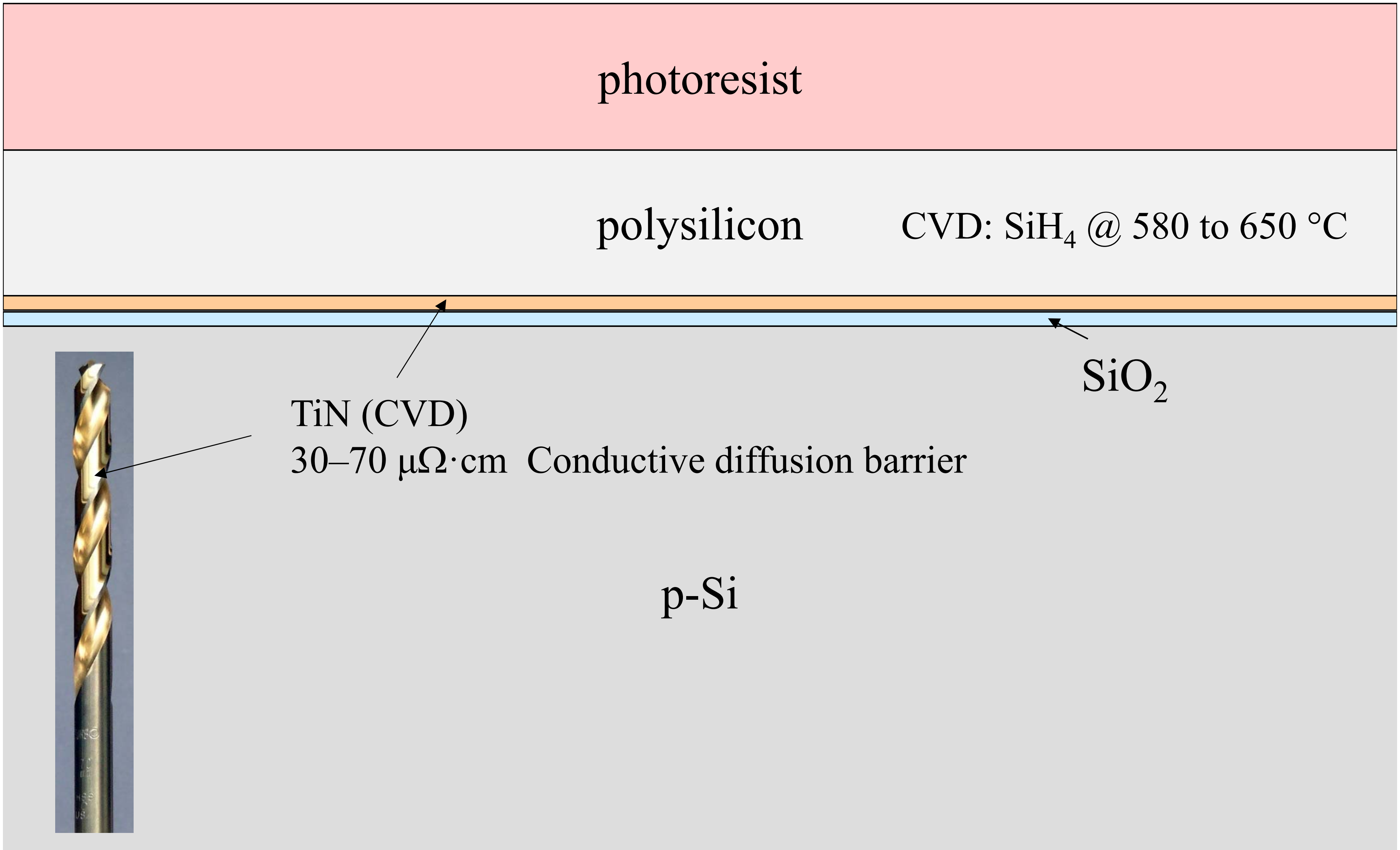
http://en.wikipedia.org/wiki/Image:Mosfet_linear.svg

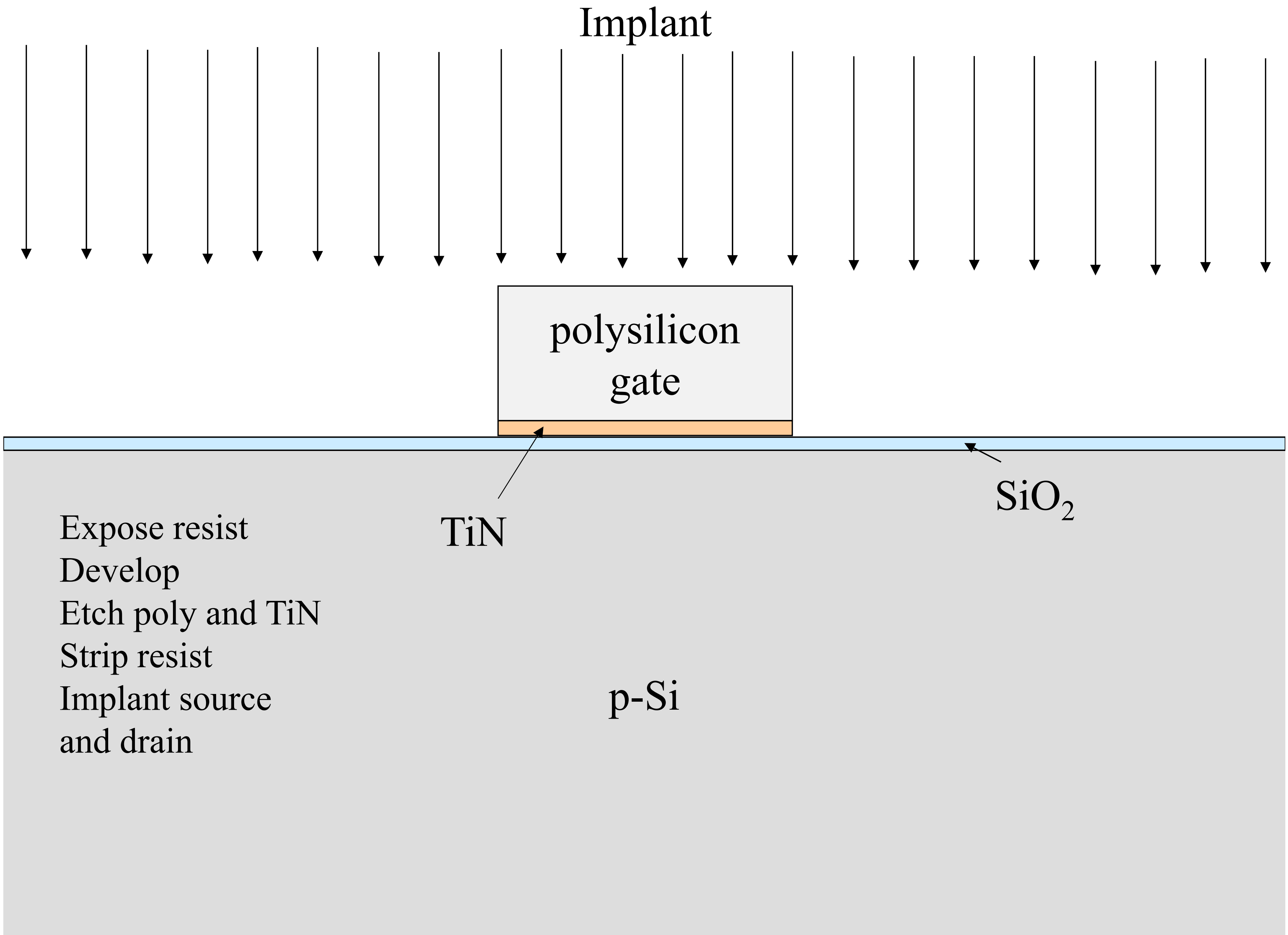
Self-aligned fabrication



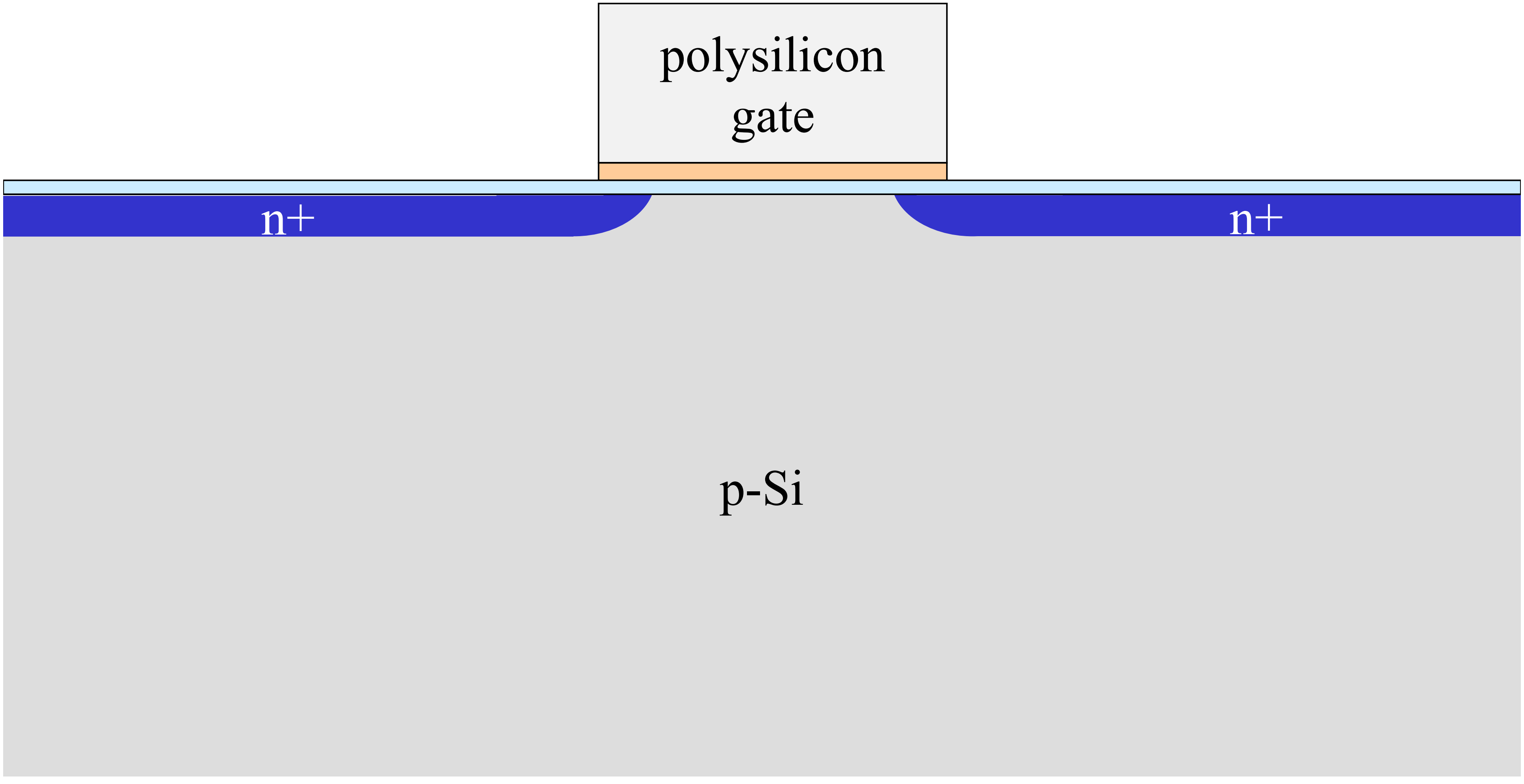
Dry oxidation



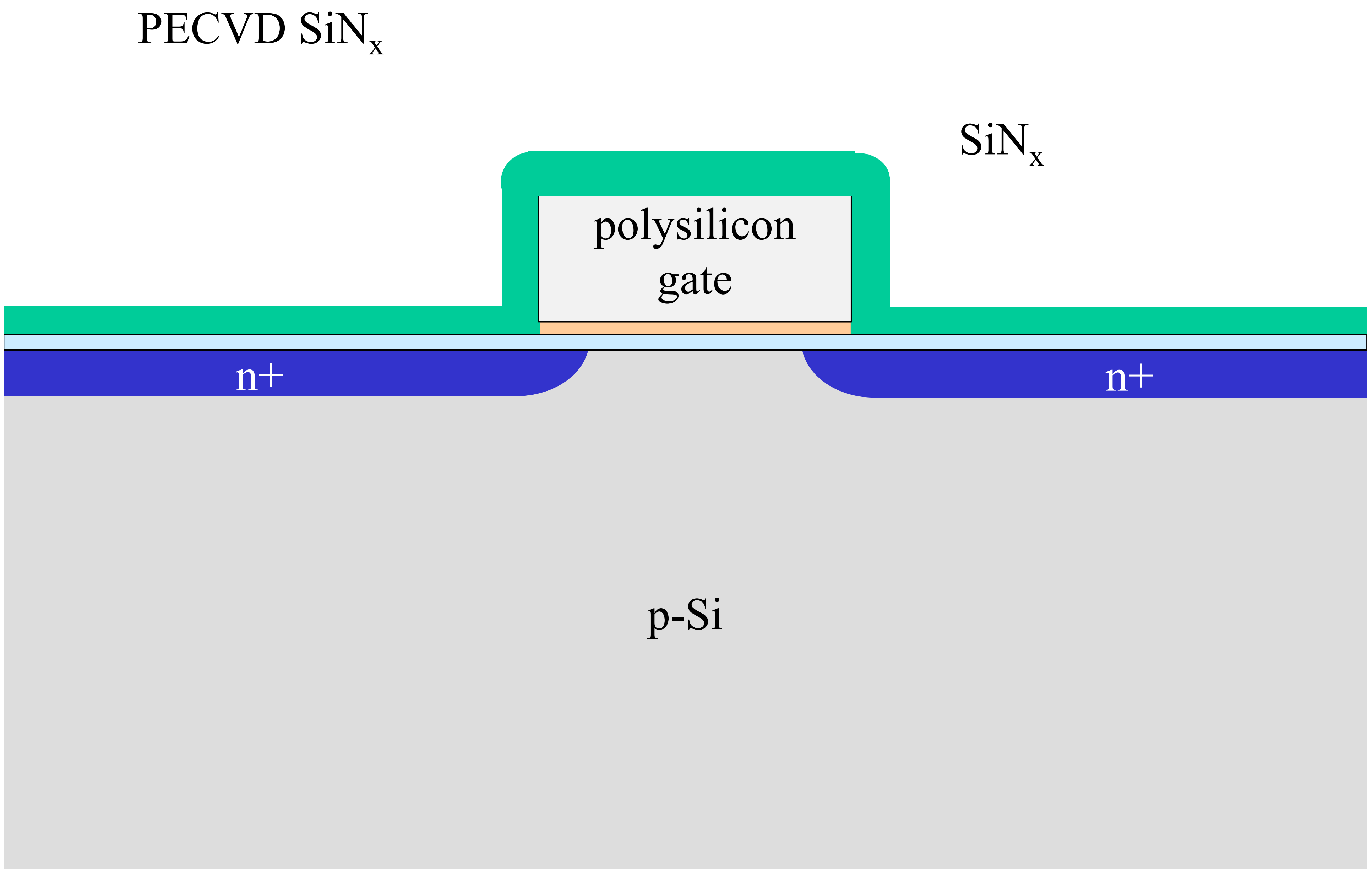

photoresist
polysilicon
CVD: SiH_4 @ 580 to 650 °C
SiO_2
TiN (CVD)
30–70 μΩ·cm Conductive diffusion barrier
p-Si


Implant
polysilicon gate
TiN
SiO_2
Expose resist
Develop
Etch poly and TiN
Strip resist
Implant source
and drain
p-Si

Self-aligned fabrication

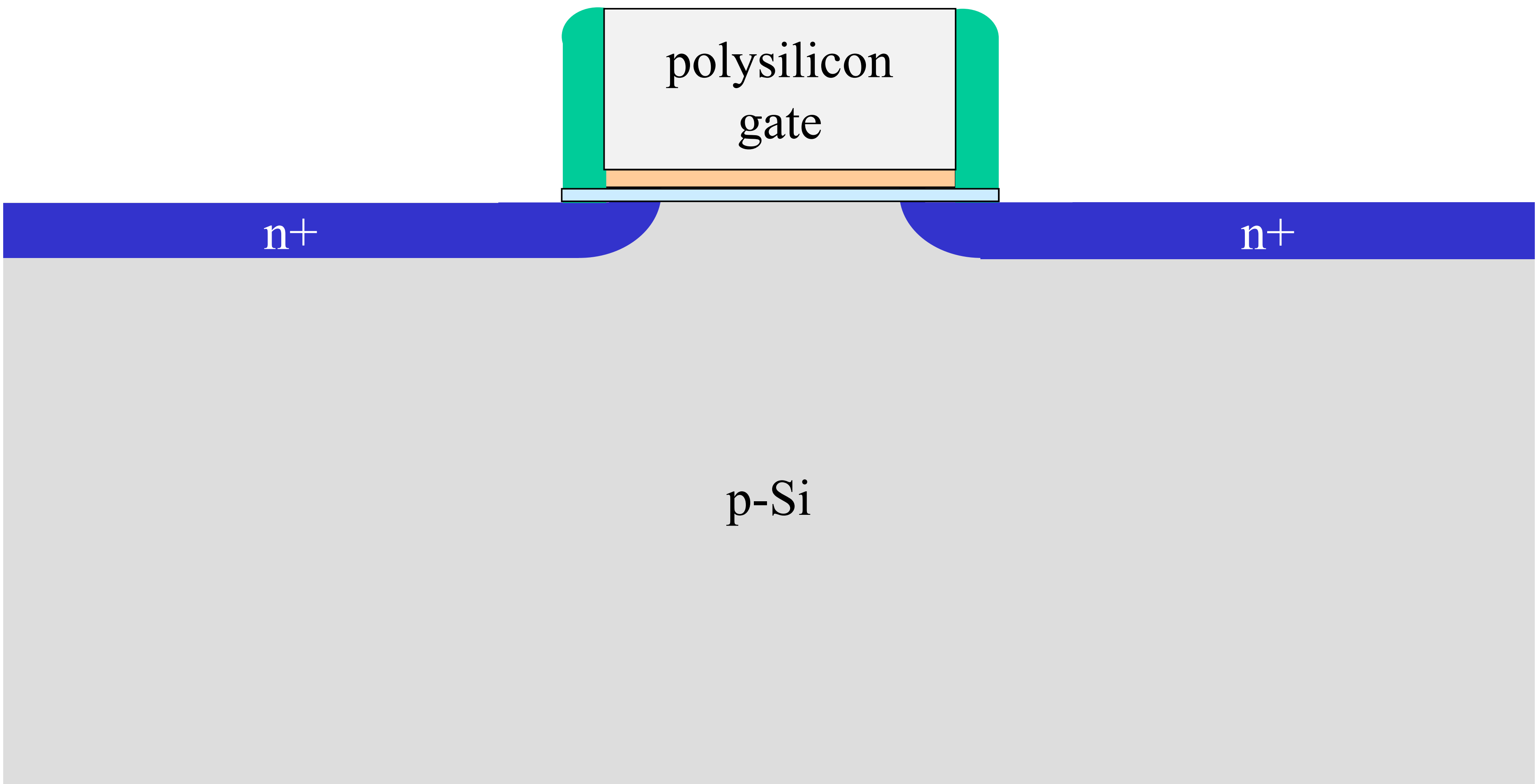


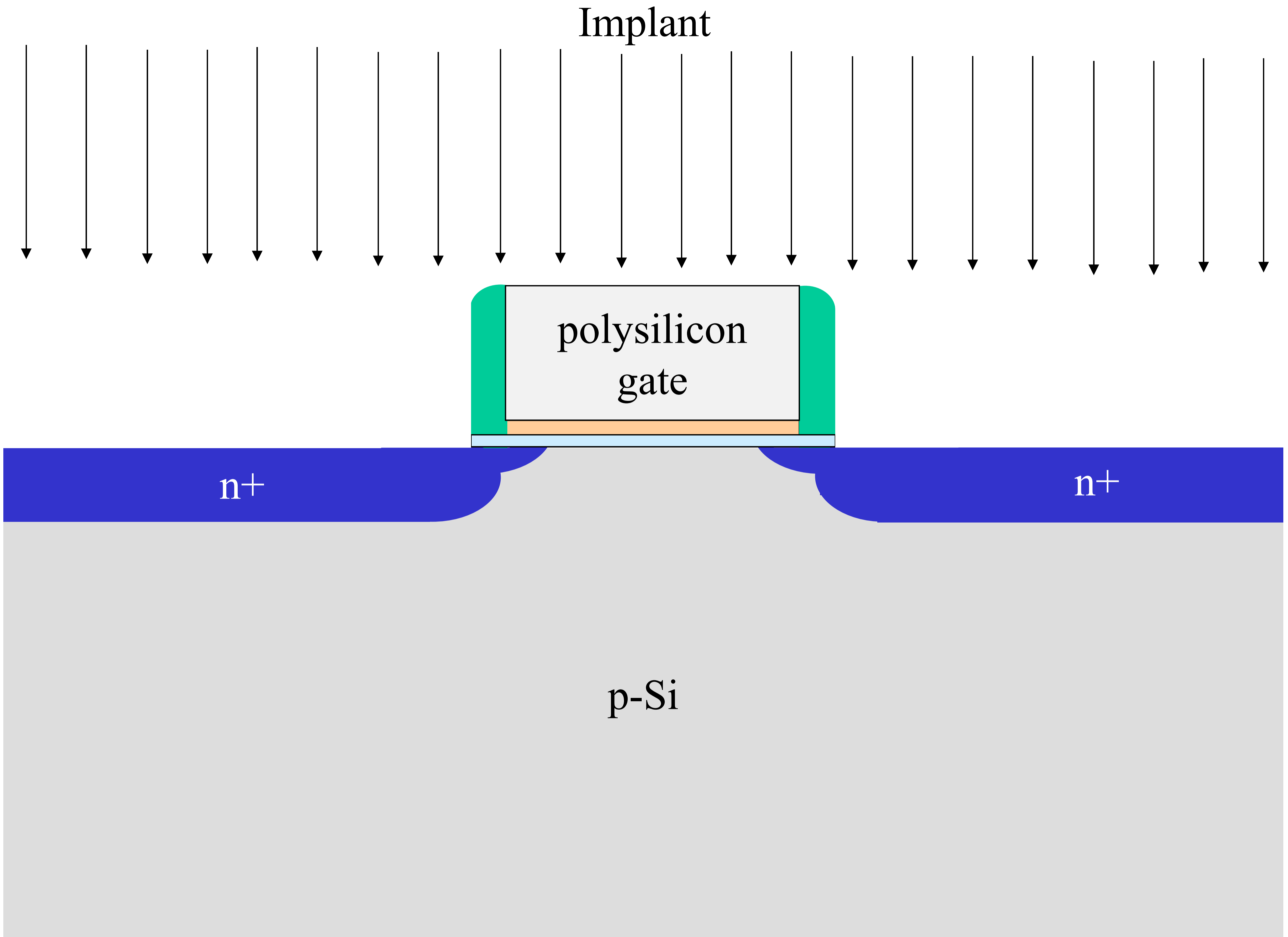
Spacer



Spacer

Etch back to leave only sidewalls




Implant
polysilicon
gate
n+
n+
p-Si

Salicide (Self-aligned silicide)

Transition metal (Ti, Co,W) is deposited (CVD). During a high temperature step is reacts to a silicide ($TiSi_2$). Not silicide is formed on nitride or oxide.