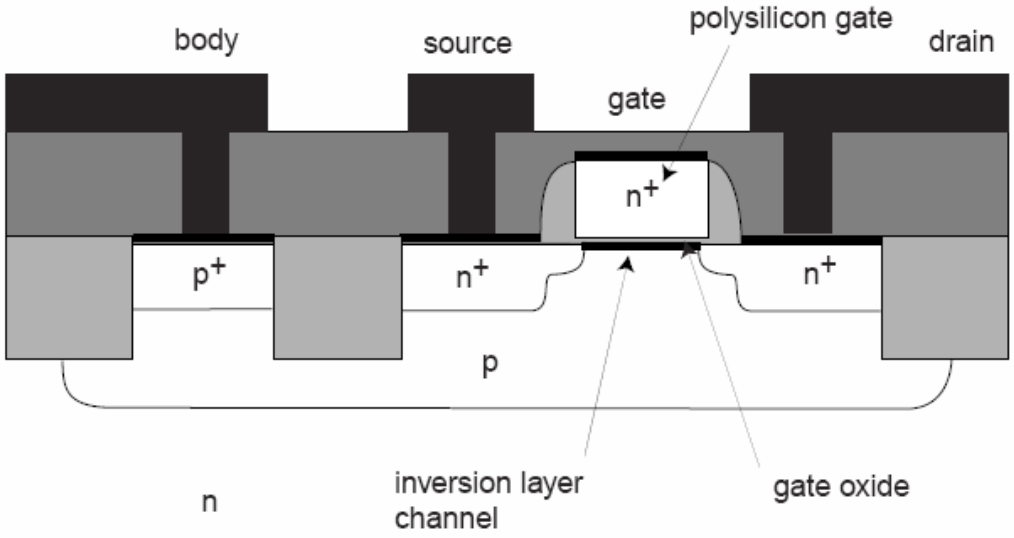
Miniaturization and scaling

Constant E-field Scaling



Gate length L, transistor width Z, oxide thickness t_{ox} are scaled down.

V_{ds}, V_{gs}, and V_T are reduced to keep the electric field constant.

Power density remains constant.

$$L \sim 45\ t_{ox}$$

1975 - 1990: "Days of happy scaling"

Constant E-field scaling

$$I_{sat} = \frac{Z}{2L}\mu_n \frac{\varepsilon_{ox}}{t_{ox}}\left(V_G - V_T\right)^2$$

$$L \Rightarrow sL, \qquad Z \Rightarrow sZ, \qquad t_{ox} \Rightarrow st_{ox}, \qquad V_{th} \Rightarrow sV_{th}$$

$$I_{sat} \Rightarrow sI_{sat} \quad \longleftarrow \quad I_{sat} \text{ gets smaller}$$

$$g_m = \frac{dI_D}{dV_G} = \frac{Z}{L}\mu_n \frac{\varepsilon_{ox}}{t_{ox}}\left(V_G - V_T\right) \quad \longleftarrow \quad \text{Transconductance stays the same.}$$

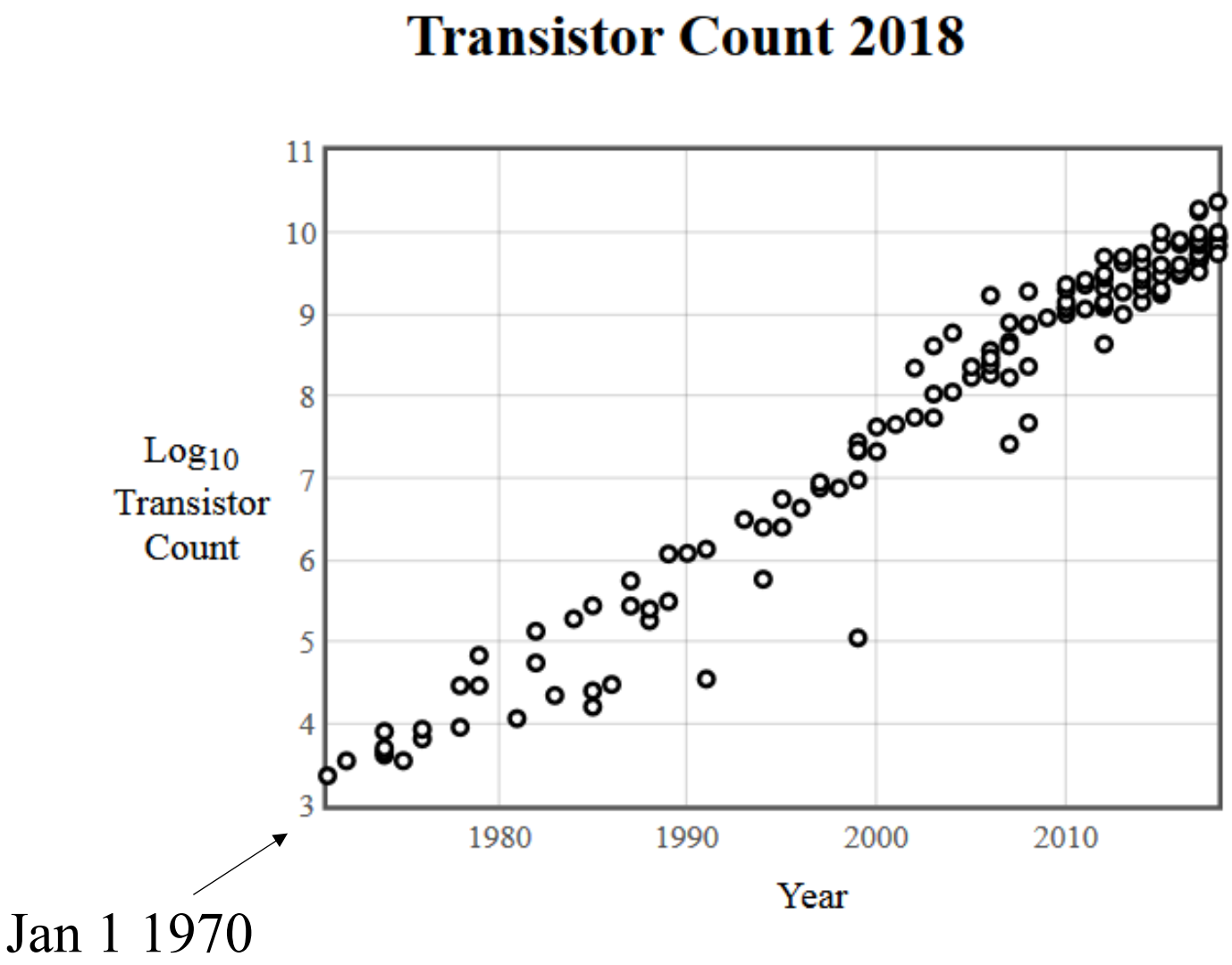
Power per transistor decreases like L^2. Power per unit area remains constant.

The heat dissipation problem

Microprocessors are hot ~ 100 C
Hotter operation will cause dopants to diffuse

When more transistors are put on a chip they must dissipate less power.

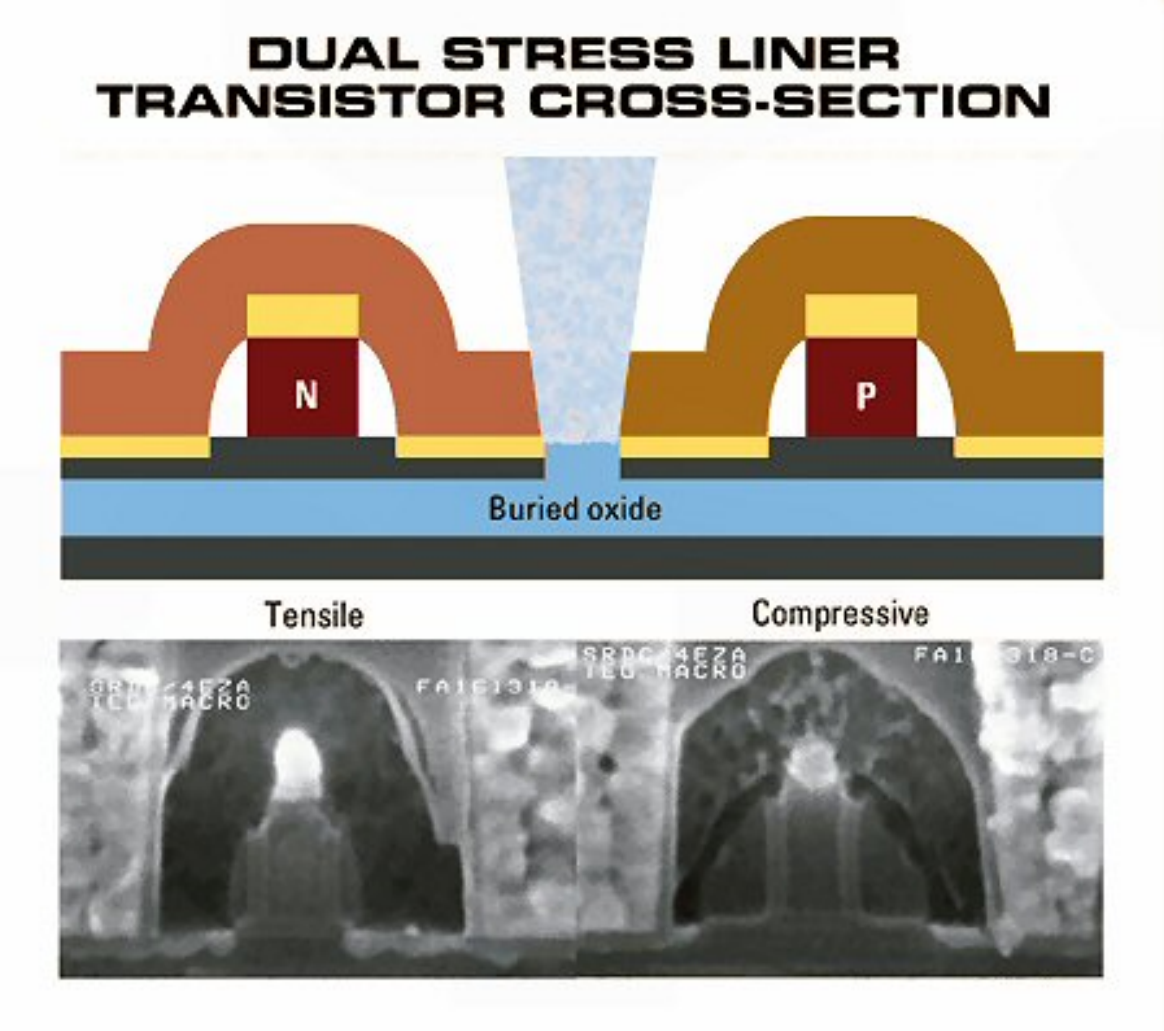
Power per transistor decreases like L^2.



Transistor count doubles about every 2 years

https://en.wikipedia.org/wiki/Transistor_count

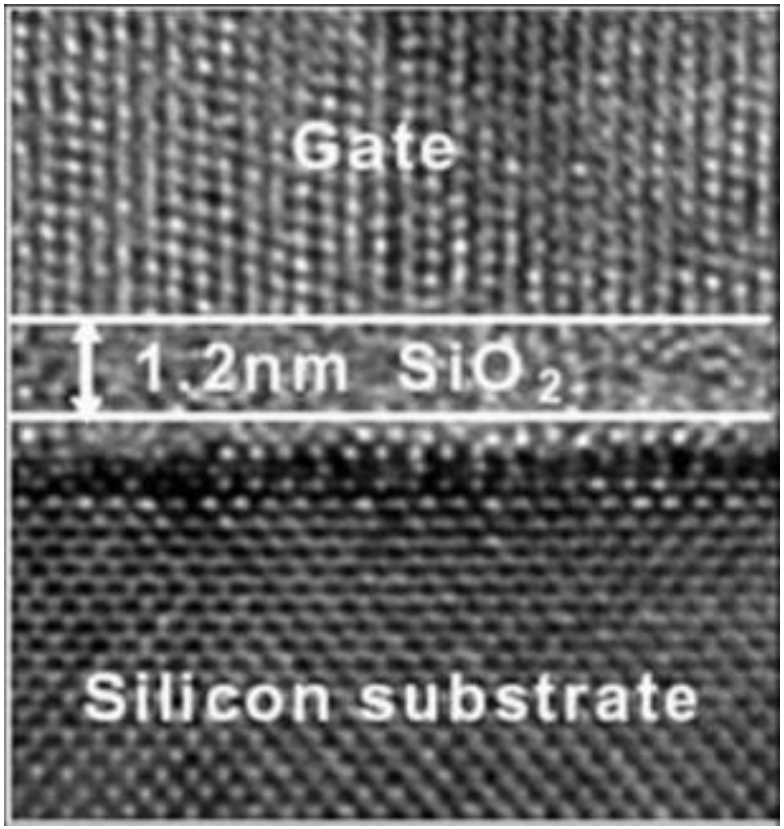
Dual stress liners



Tensile silicon nitride film over the NMOS and a compressive silicon nitride film over the PMOS improves the mobility.

http://www.xbitlabs.com/articles/cpu/display/athlon64-venice_2.html

Gate dielectric



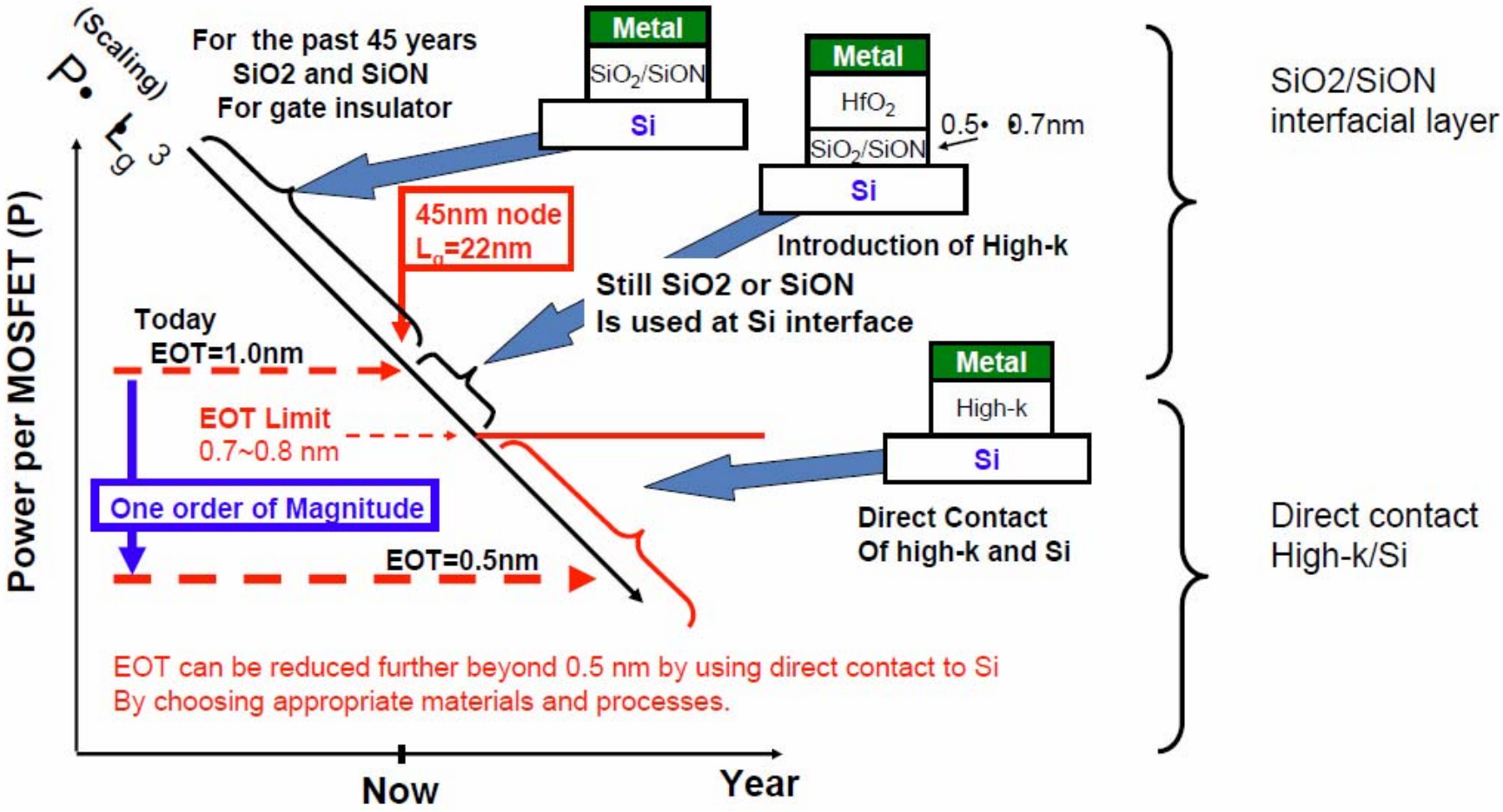
Thinner than 1 nm: electrons tunnel

Large dielectric constant desirable

$\varepsilon_r(SiO_2) \sim 4$

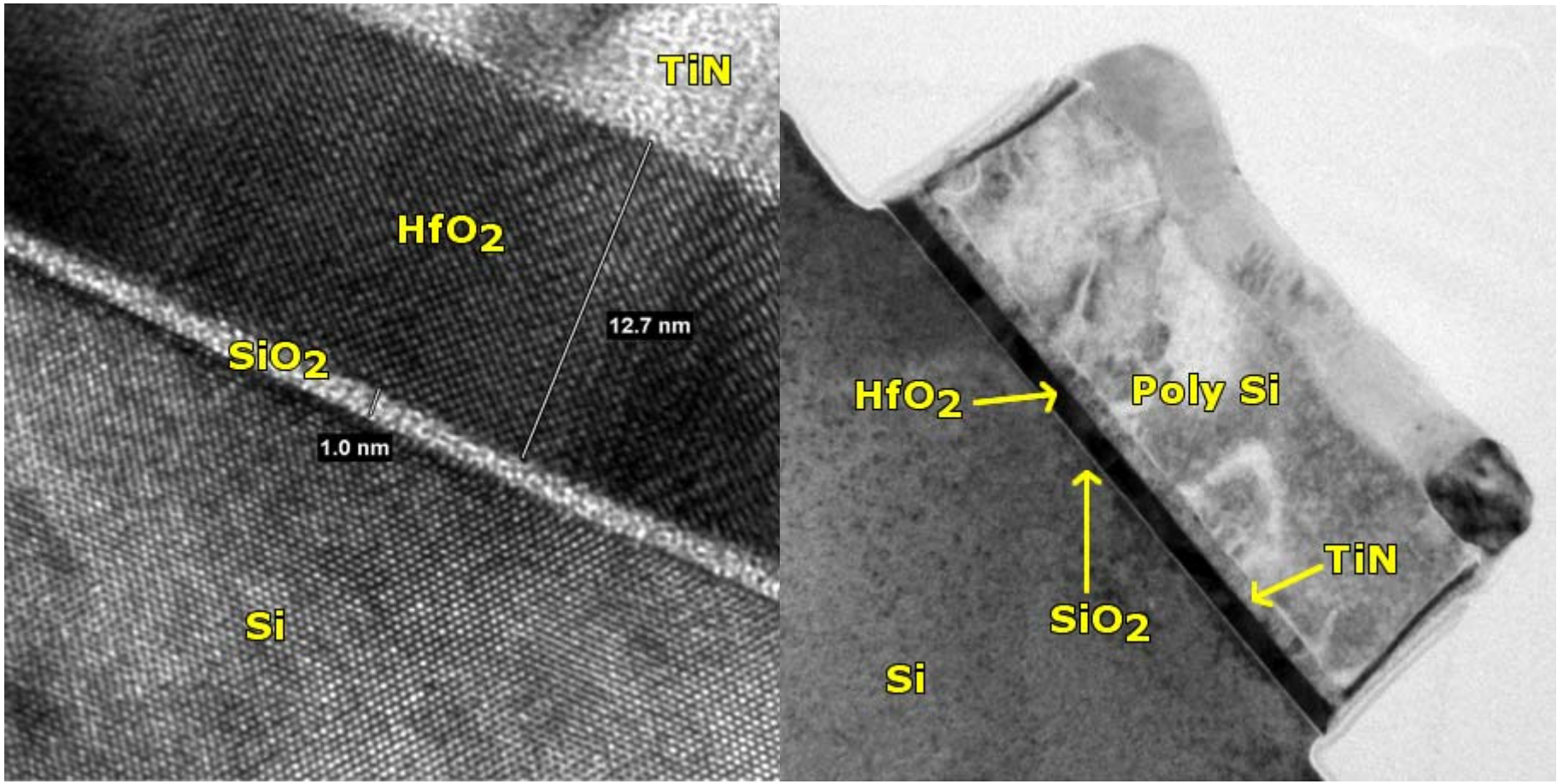
$\varepsilon_r(Si_3N_4) \sim 7$

Direct contact technology of high-k to Si



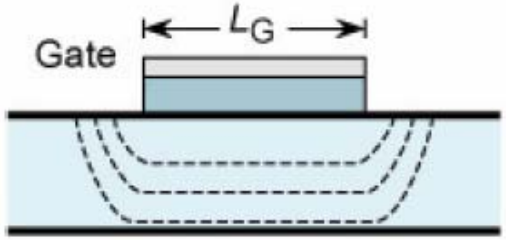
www.iwailab.ep.titech.ac.jp

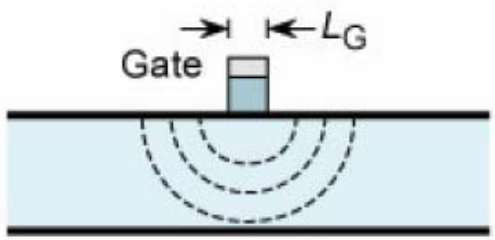
High-k dielectrics

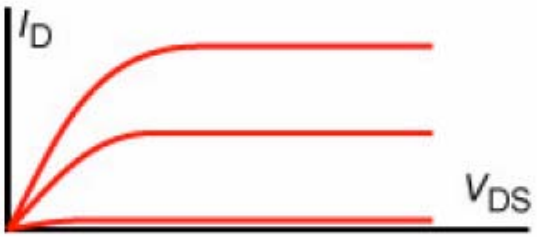


http://nano.boisestate.edu/research-areas/gate-oxide-studies/

Short channel effects







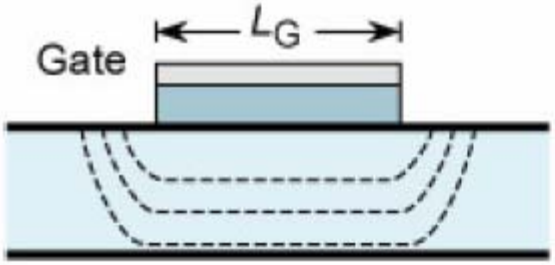
Short-channel effects:

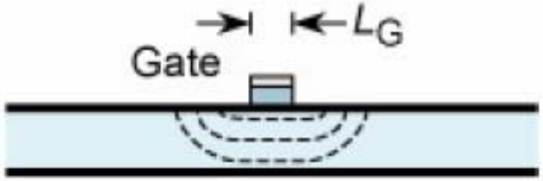
Threshold-voltage shift

Lack of pinch-off

Increased leakage current

Increase of output conductance





SOI: silicon on insulator

CMOS SOI

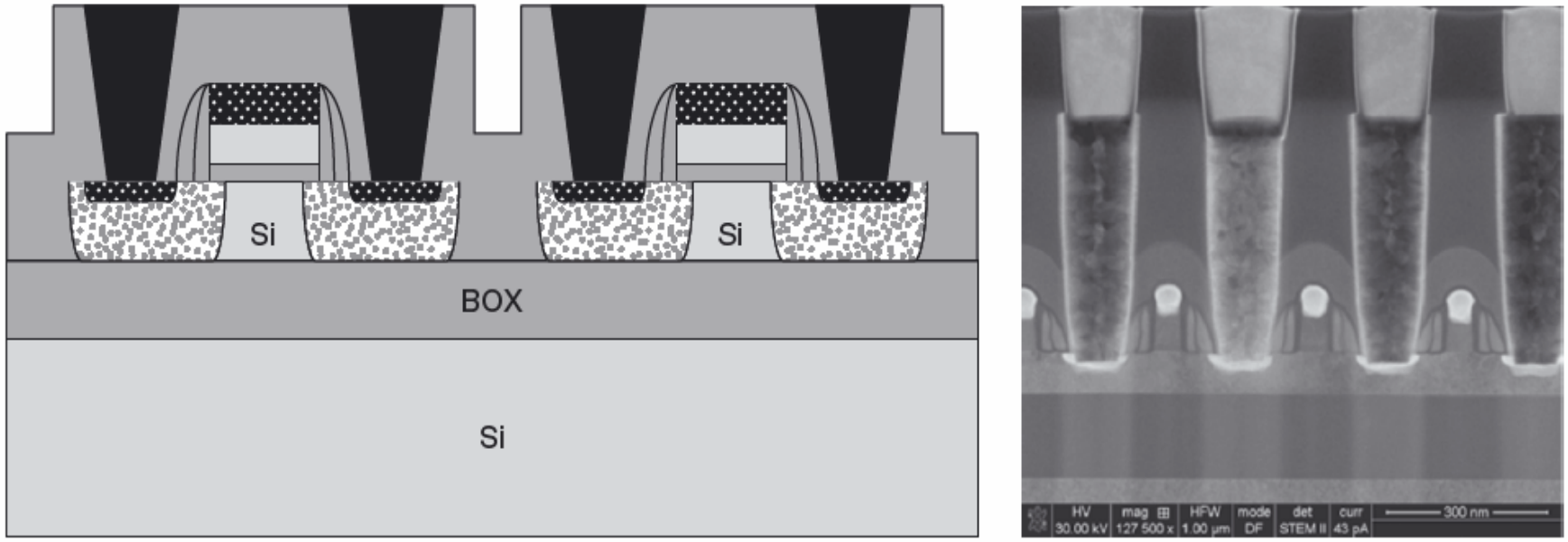


Figure 26.16 SOI MOSFET with first-level metal, schematic and TEM. Courtesy Brandon Van Leer, FEI Company4

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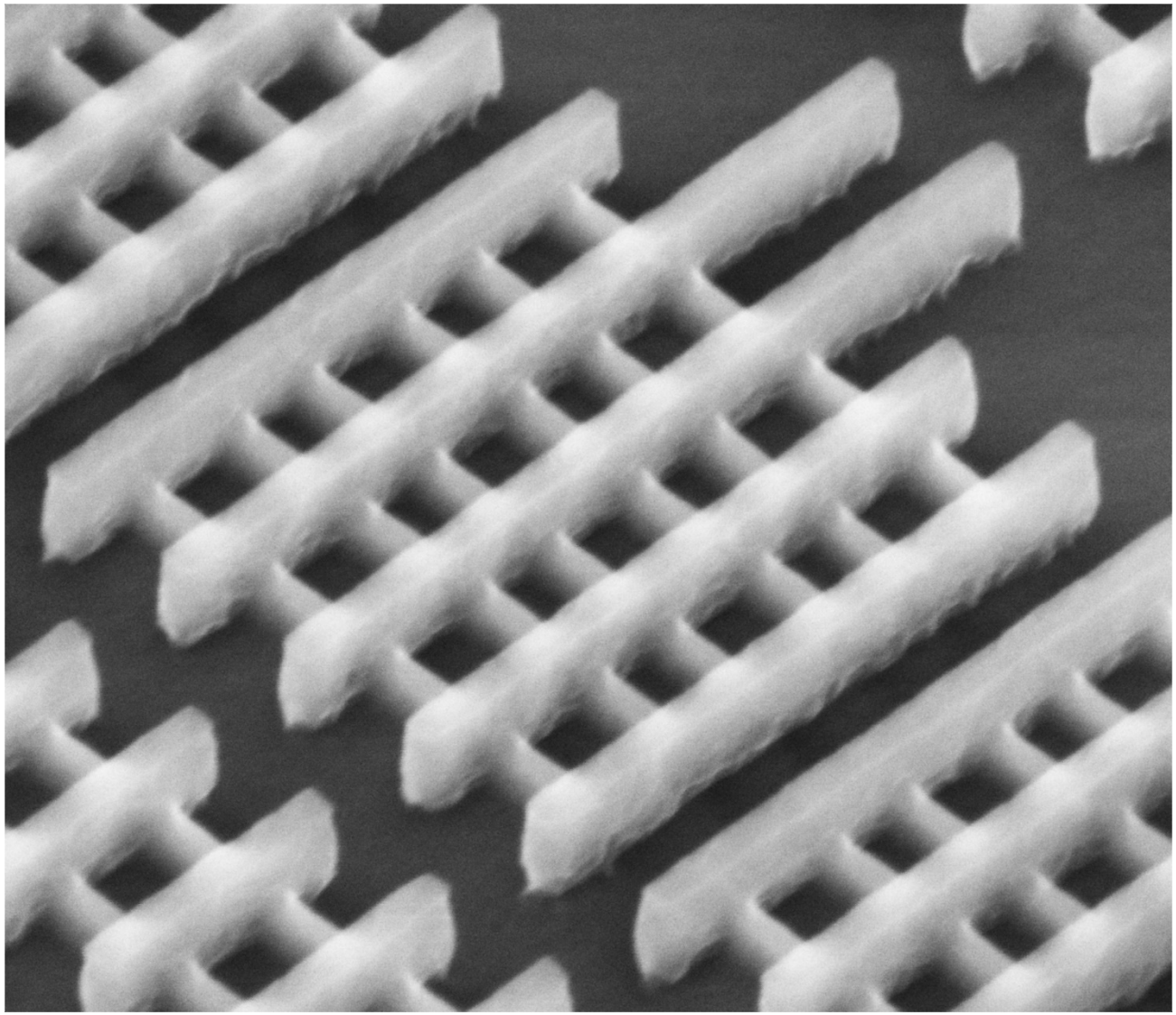
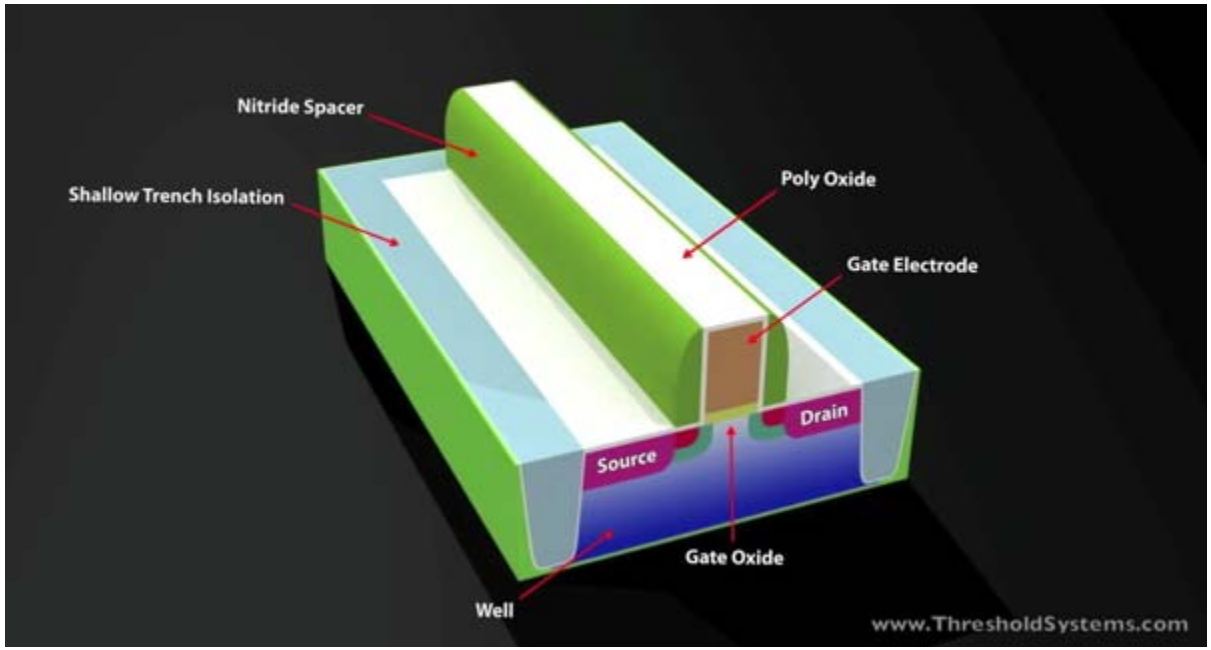
Intel® Pentium® 4	90 nm
Intel® Pentium® D	65 nm
Intel® Core™2 Duo	45 nm
Intel® Atom™ Z6xx Series	45 nm
Intel® Core™2 Celeron	45 nm
Intel® Core™ i7-900	32 nm
Intel® Xeon® 5600 Series	32 nm
Intel® Ivy bridge tri-gate	22 nm
Intel® Haswell FinFET	16 nm

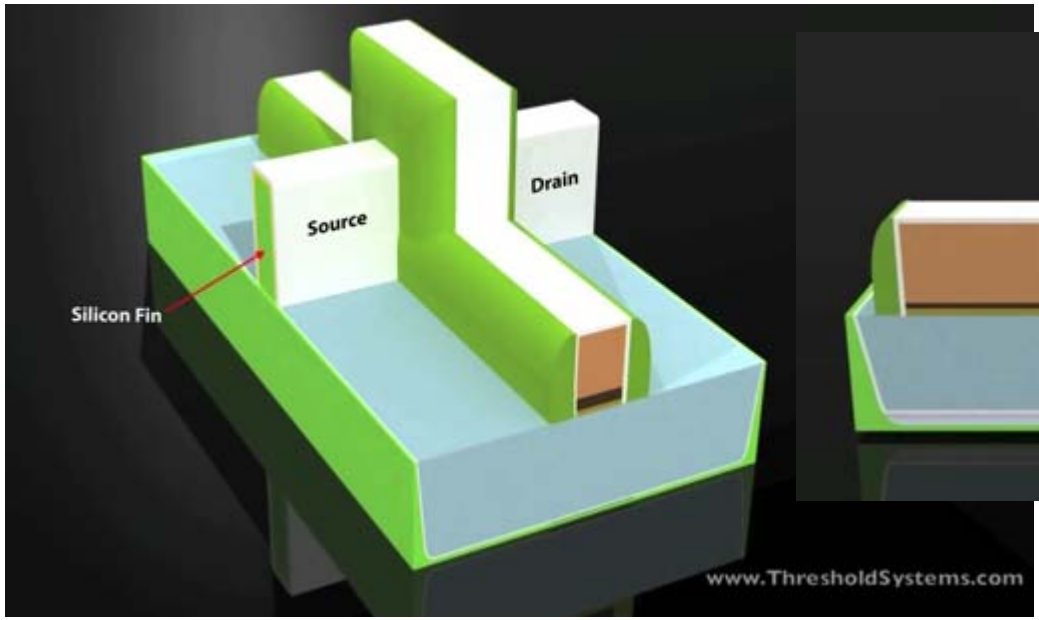
Intel 22nm 3D tri-gate transistor

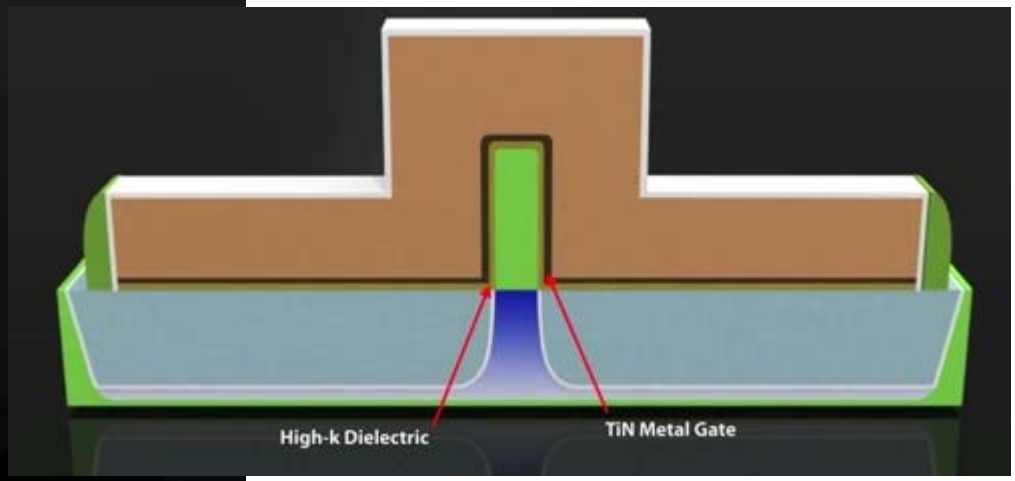


http://download.intel.com/newsroom/kits/22nm/gallery/images/Intel-22nm_Transistor.jpg

FinFET



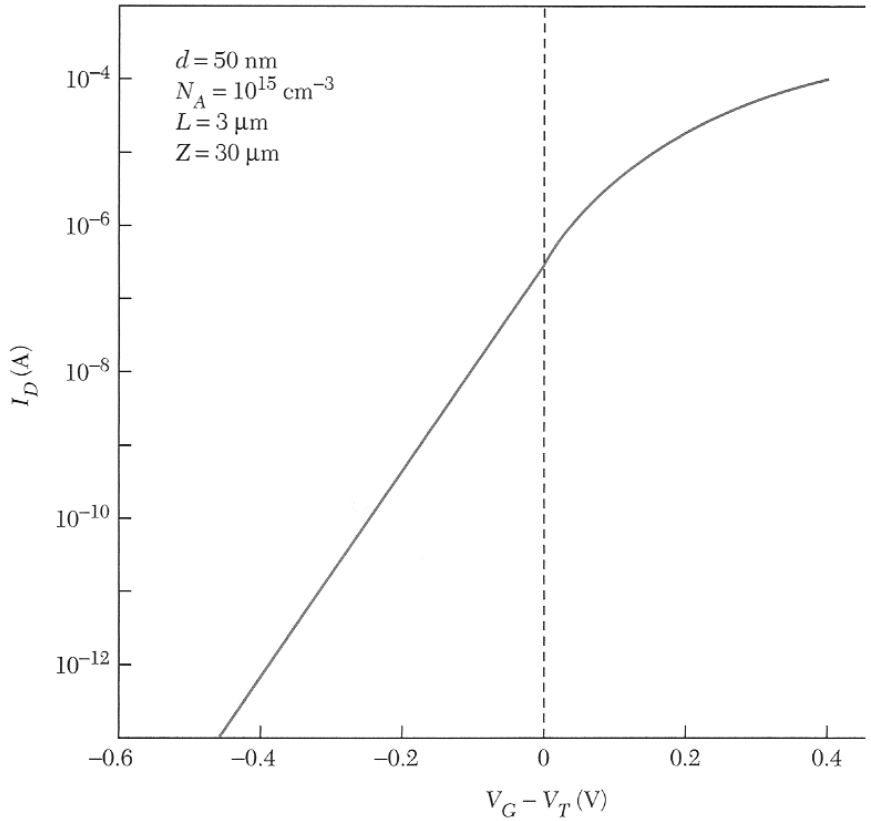




https://www.youtube.com/watch?v=Jctk0DI7YP8

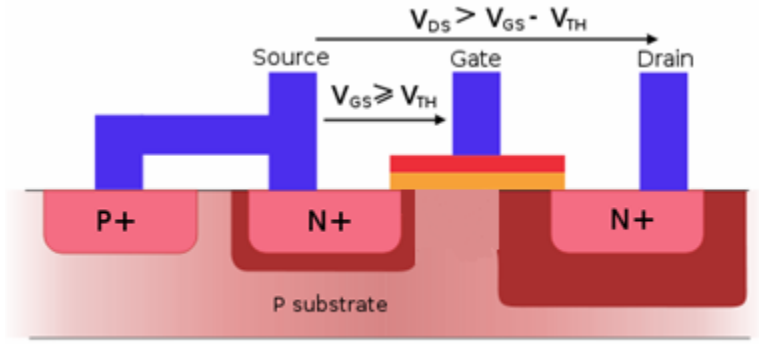
Subthreshold current

For $V_G < V_T$ the transistor should switch off but there is a diffusion current. The current is not really off until ~ 0.5 V below the threshold voltage.



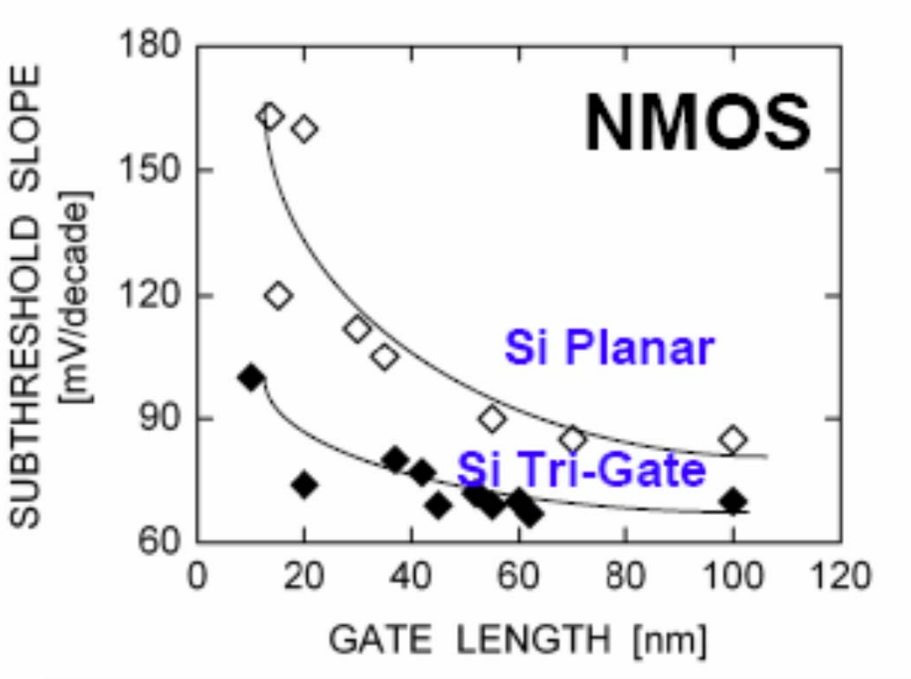
Weak inversion

$$I_D \propto \exp\left(\frac{e(V_G - V_T)}{k_B T}\right)$$

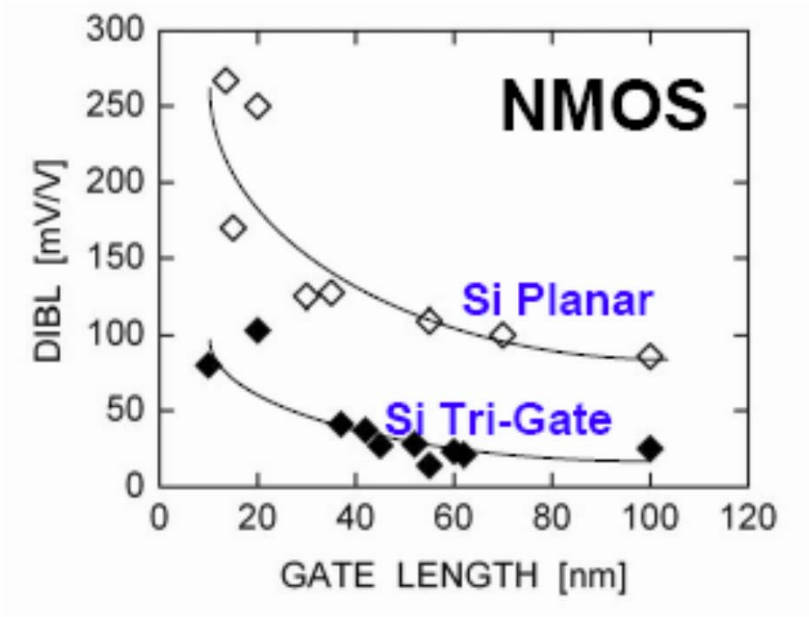


Subthreshold swing: 70-100 mV/decade

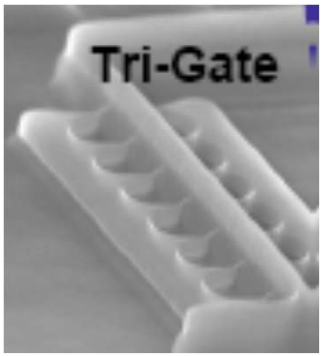
FinFET, Tri-gate



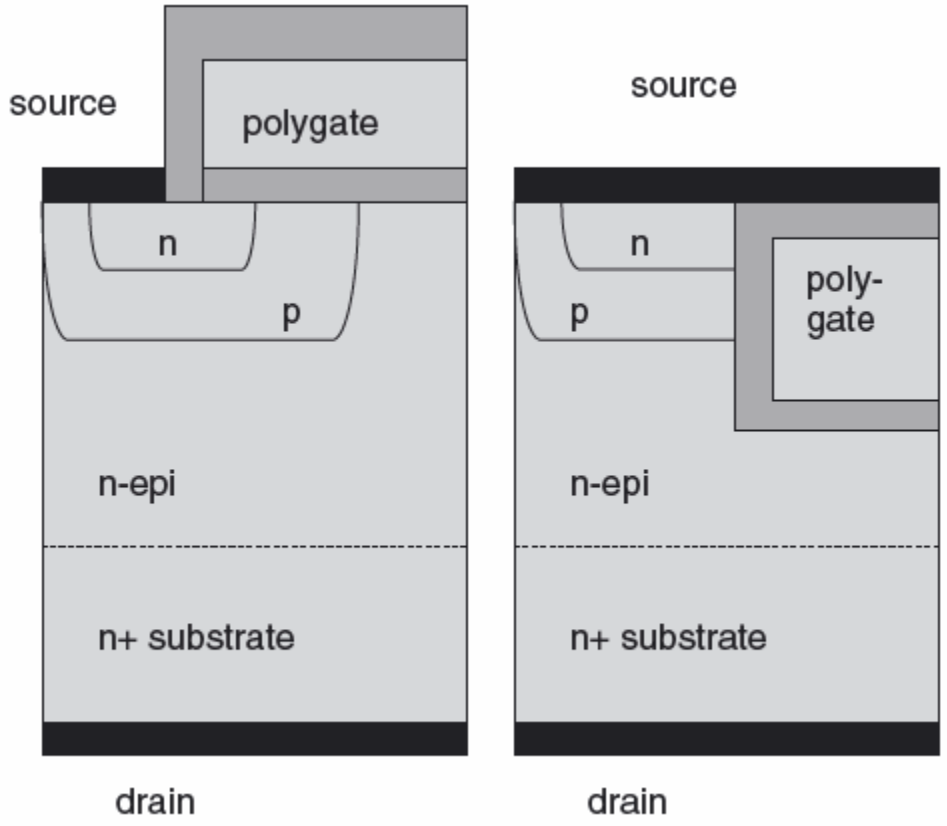
Drain induced barrier lowering



Robert Chau, Intel



U-MOSFET and D-MOSFET



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Power transistors