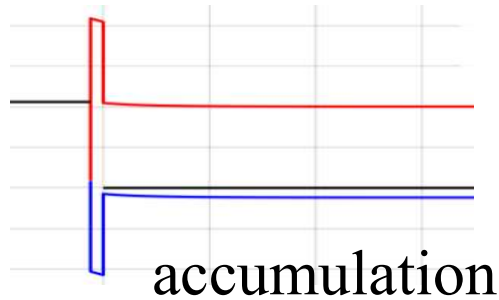


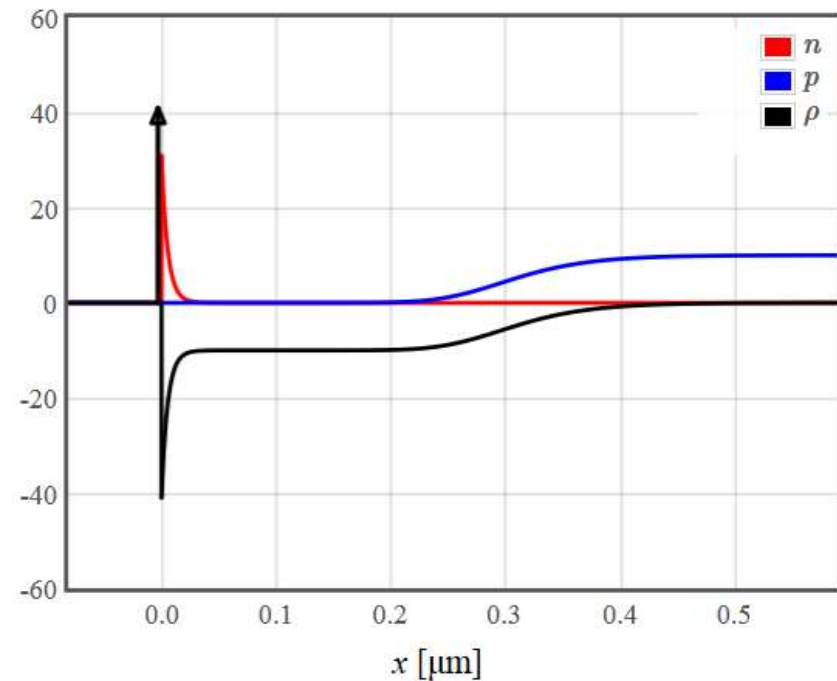
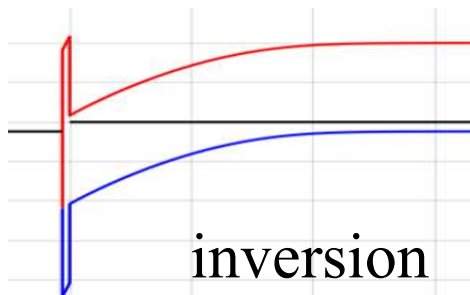
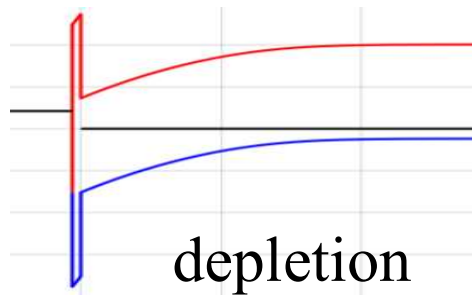
MOSFETs: Gradual Channel Approximation

Memories

Gradual channel approximation



$$Q_{\text{mobile}} = \begin{cases} 0, & \text{for } V_G - V_B < V_T \\ -C_{\text{ox}}(V_G - V_B - V_T) & \text{for } V_G - V_B > V_T \end{cases}$$

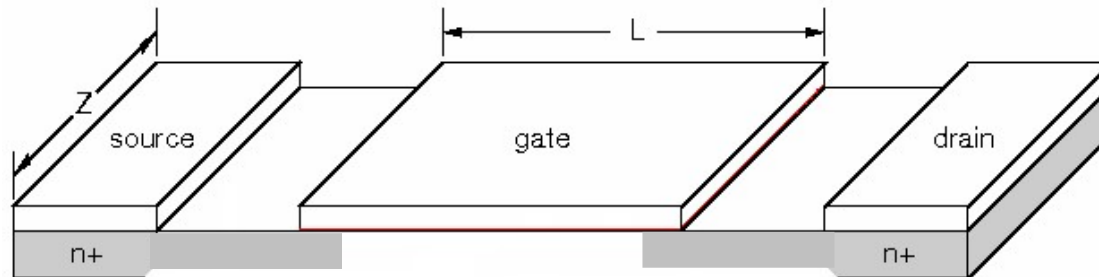


<http://lampx.tugraz.at/~hadley/psd/L10/gradualchannelapprox.php>

Gradual channel approximation

Ohm's law $\longrightarrow j = -nev_d = ne\mu_n E_y$

$$I = Ztj = Ztne\mu_n E_y = Ze\mu_n n_s E_y$$



$n_s = nt$ is the sheet charge at the interface.

$$n_s(y) = -\frac{Q}{e} = \frac{C_{ox}(V_G - V_{ch}(y) - V_T)}{e}$$

Gradual channel approximation

$$n_s(y) = -\frac{Q(y)}{e} = \frac{C_{ox}(V_G - V_{ch}(y) - V_T)}{e}$$

$$I = Ztj = Ztnev_d = Zen_s\mu_n E_y$$

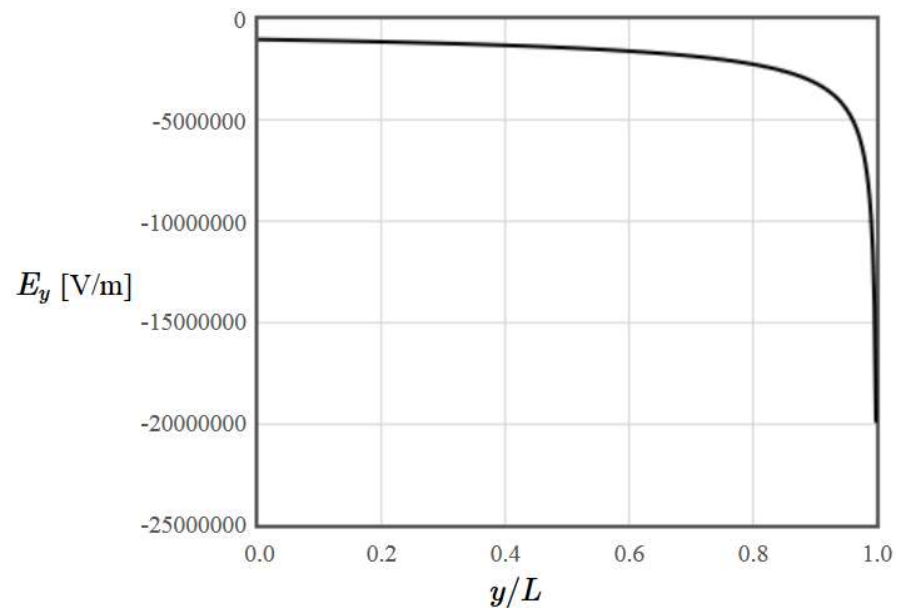
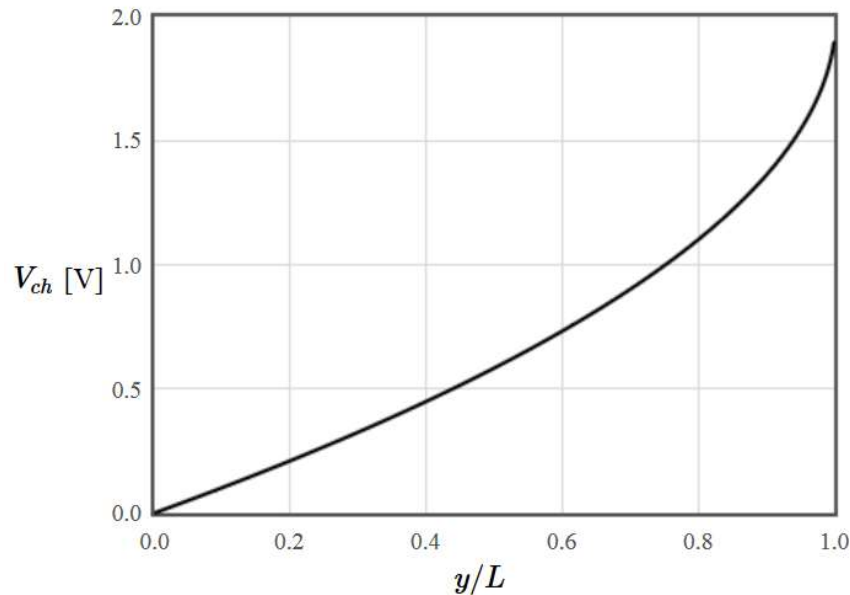
$$I_D = -Z\mu_n C_{ox}(V_G - V_{ch}(y) - V_T) \frac{dV_{ch}}{dy}$$

differential equation for V_{ch}

Gradual channel approximation

$$V_{ch}(y) = V_G - V_T - \sqrt{(V_G - V_T)^2 - \frac{2I_D y}{Z\mu_n C_{ox}}}$$

$$E_y = -\frac{dV_{ch}}{dy} = -\frac{I_D}{Z\mu_n C_{ox} \sqrt{(V_G - V_T)^2 - \frac{2I_D y}{Z\mu_n C_{ox}}}}$$

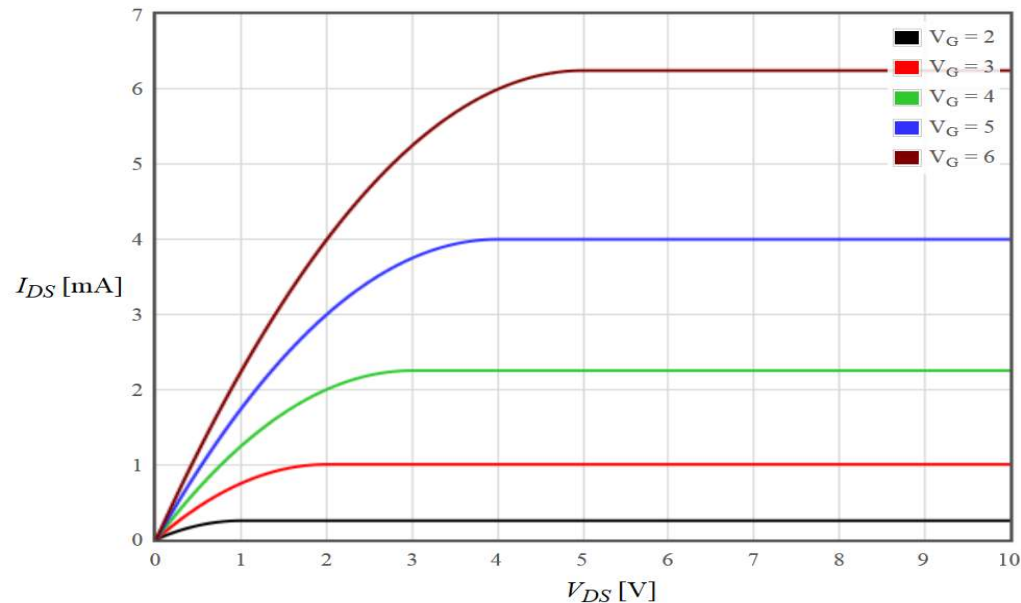


Gradual channel approximation

$$\int_0^L I_D dy = \int_0^{V_D} Z \mu_n C_{ox} (V_G - V_{ch}(y) - V_T) dV$$

$$I_D = \frac{Z}{L} \mu_n C_{ox} \left[(V_G - V_T) V_D - \frac{V_D^2}{2} \right]$$

Valid in the linear regime (until pinch-off occurs at the drain).

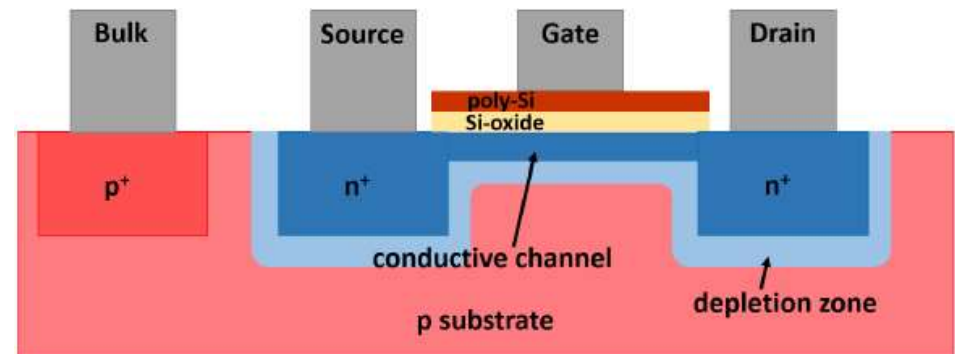
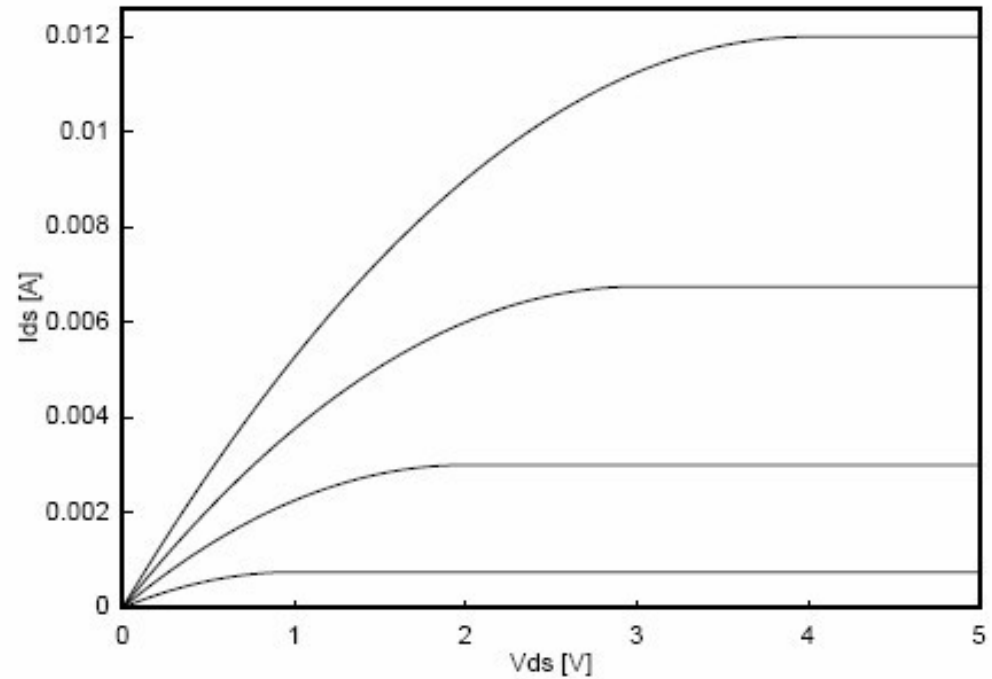


MOSFET (linear regime)

Channel conductance in the linear regime. For small V_D

$$I \approx \frac{Z}{L} \mu_n C_{ox} [(V_G - V_T) V_D]$$

$$g_D = \frac{dI_D}{dV_D} = \frac{Z}{L} \mu_n C_{ox} (V_G - V_T)$$



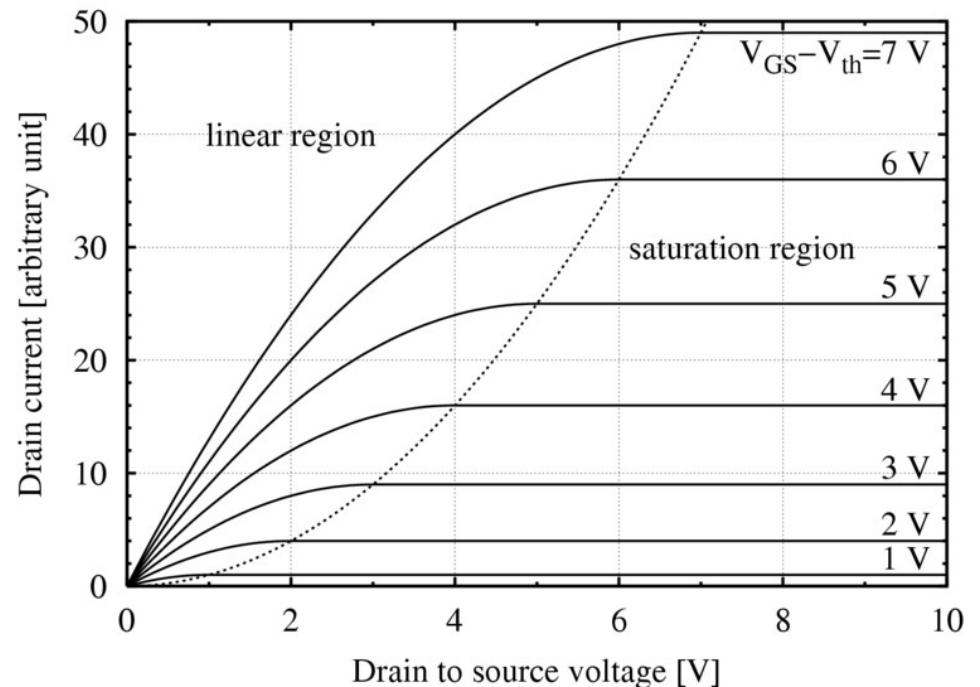
MOSFET-saturation voltage

$$I = \frac{Z}{L} \mu_n C_{ox} \left[(V_G - V_T) V_D - \frac{V_D^2}{2} \right]$$

At pinch-off, $dI_{ds}/dV_{ds} = 0$

$$\frac{dI}{dV_D} = \frac{Z}{L} \mu_n C_{ox} \left[(V_G - V_T) - V_D \right] = 0 \quad V_{sat} = (V_G - V_T)$$

A MOSFET in saturation is a voltage controlled current source.



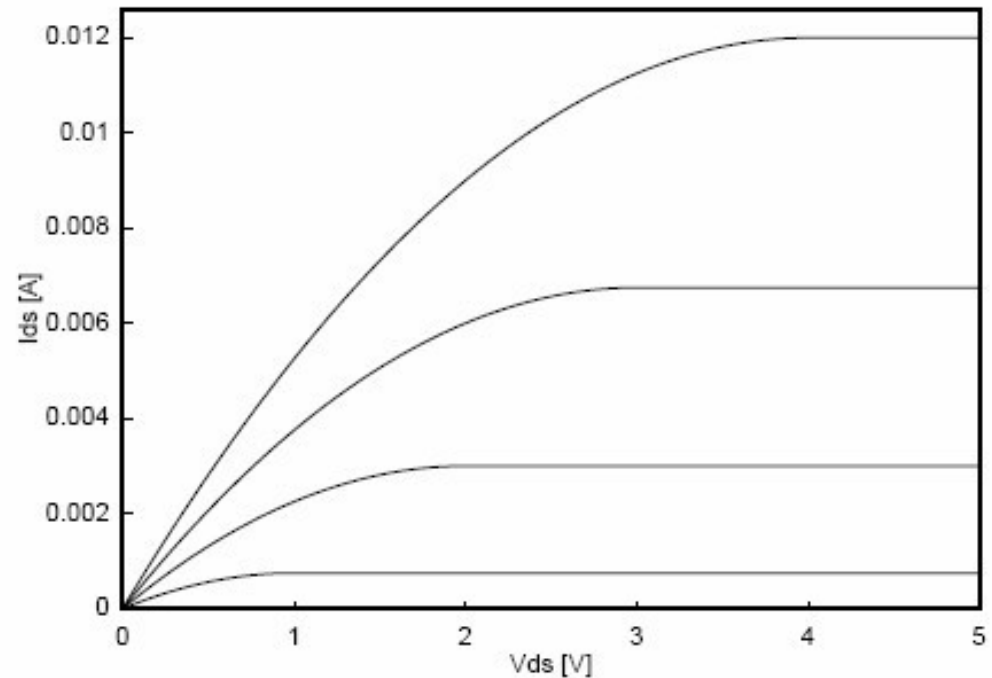
MOSFET - saturation current

Use the saturation voltage at pinch-off to determine the saturation current

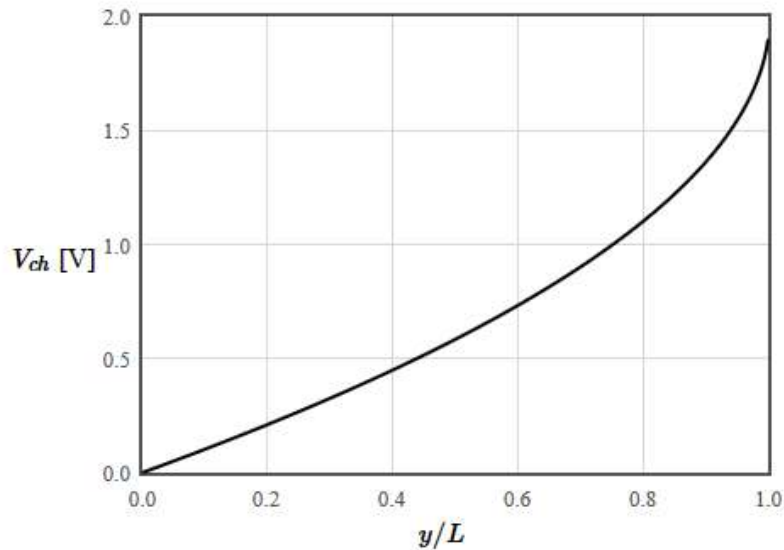
$$V_{sat} = (V_G - V_T)$$

$$I = \frac{Z}{L} \mu_n C_{ox} \left[(V_G - V_T) V_D - \frac{V_D^2}{2} \right]$$

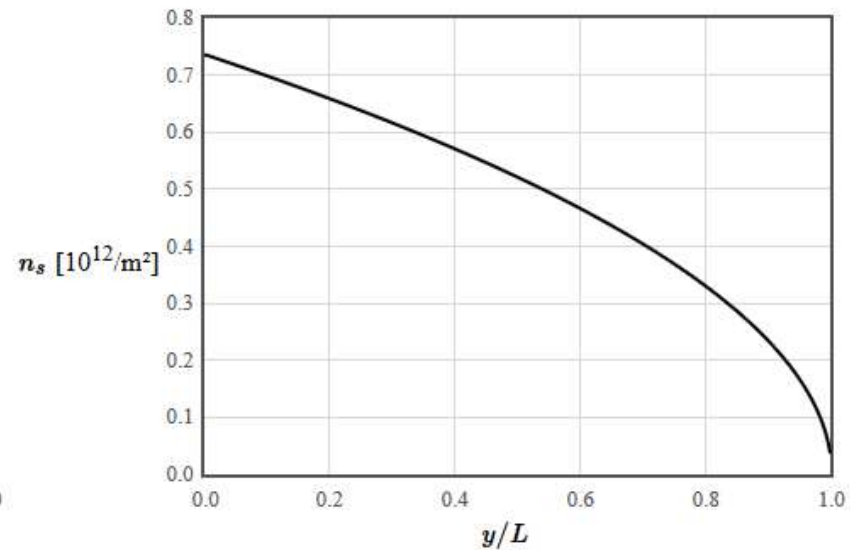
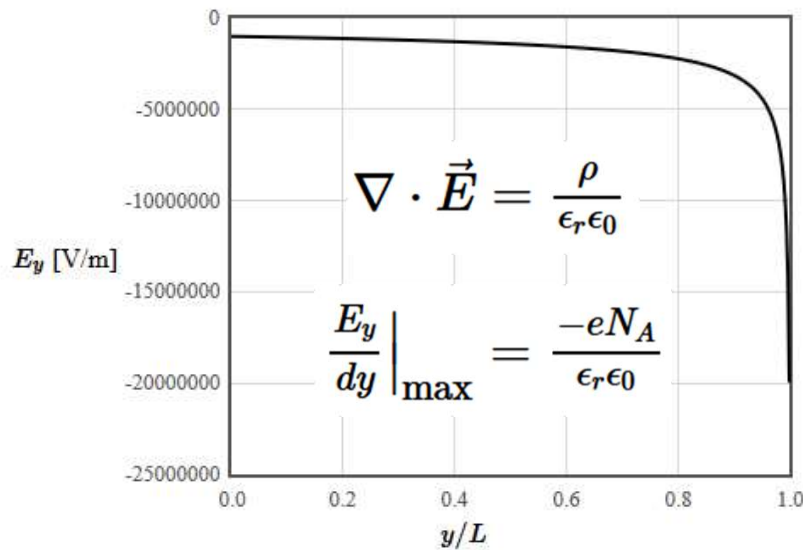
$$I_{sat} = \frac{Z}{2L} \mu_n C_{ox} (V_G - V_T)^2$$



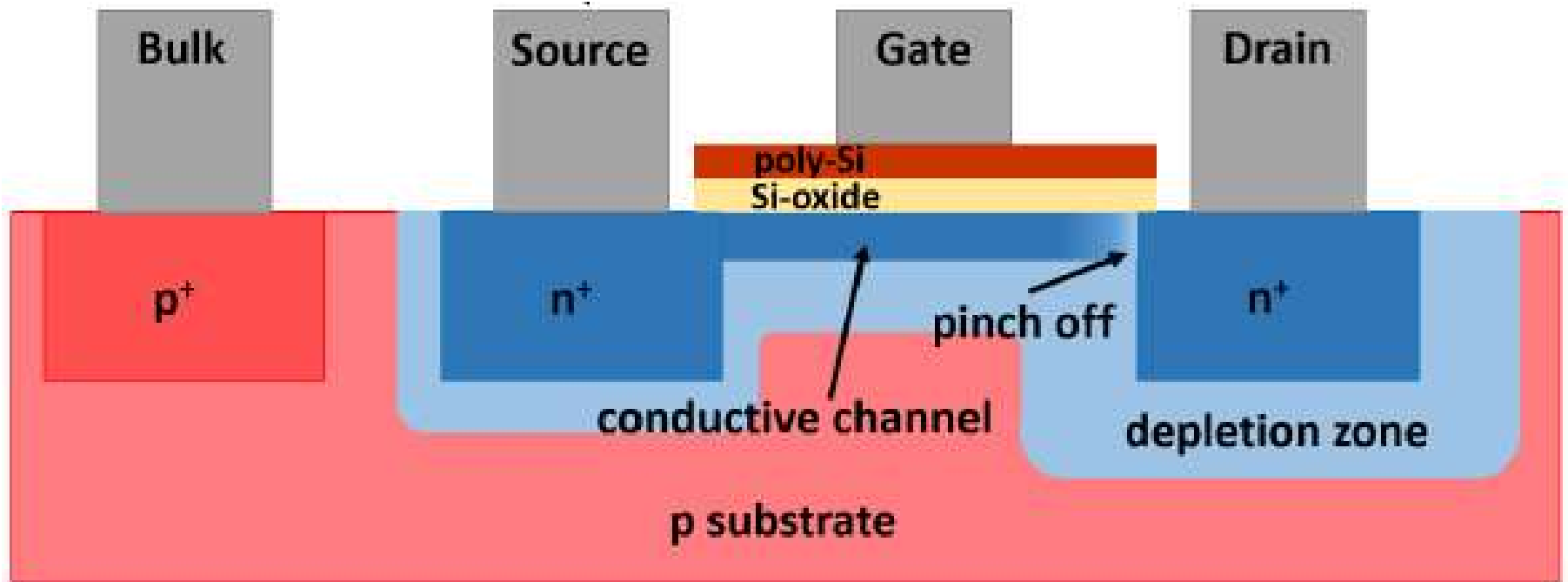
MOSFET Gradual Channel Approximation



Z	<input type="text" value="1E-5"/>	m
L	<input type="text" value="1E-6"/>	m
μ_n	<input type="text" value="1500"/>	cm ² /Vs
ϵ_r	<input type="text" value="4"/>	
t_{ox}	<input type="text" value="3E-9"/>	m
V_D	<input type="text" value="1.9"/>	V
V_G	<input type="text" value="3"/>	V
V_T	<input type="text" value="1"/>	V
<input type="button" value="Replot"/>		

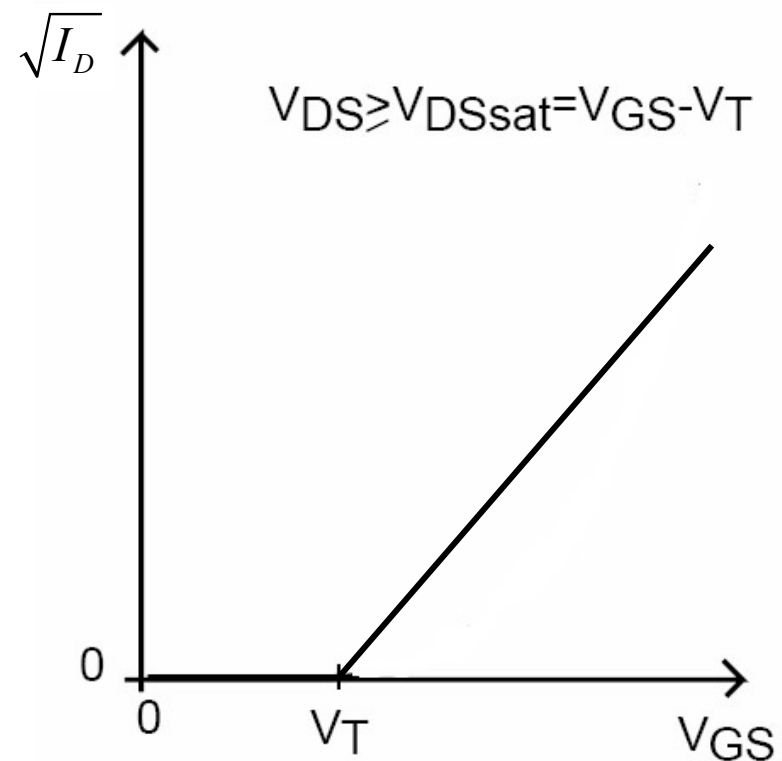
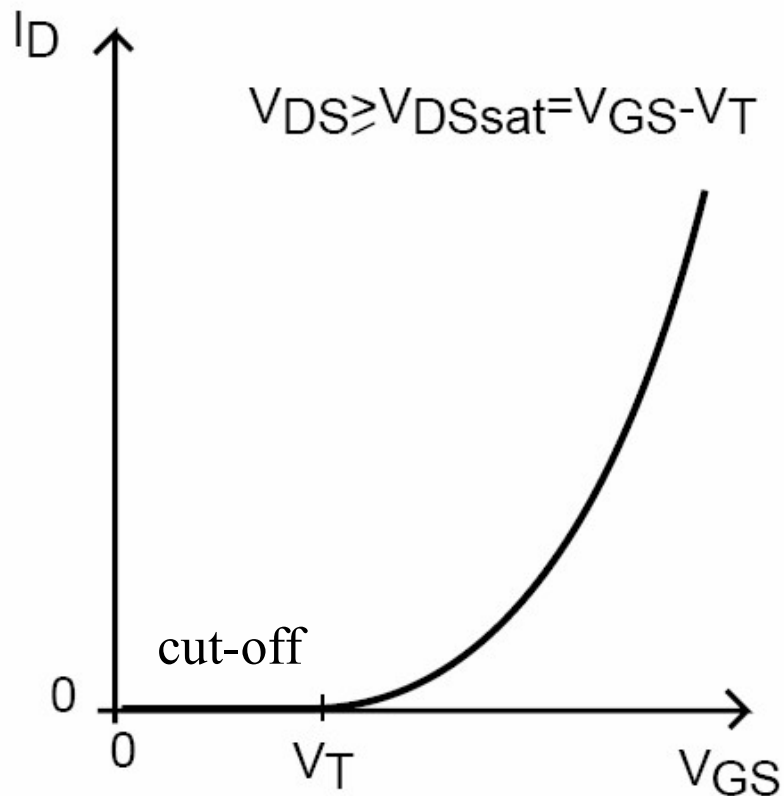
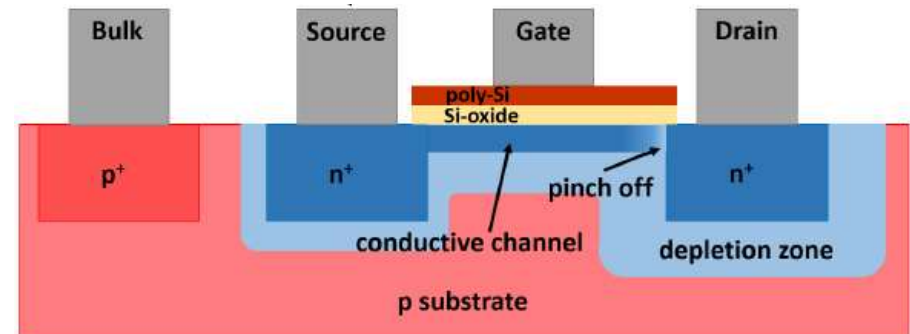


MOSFET (saturation regime)

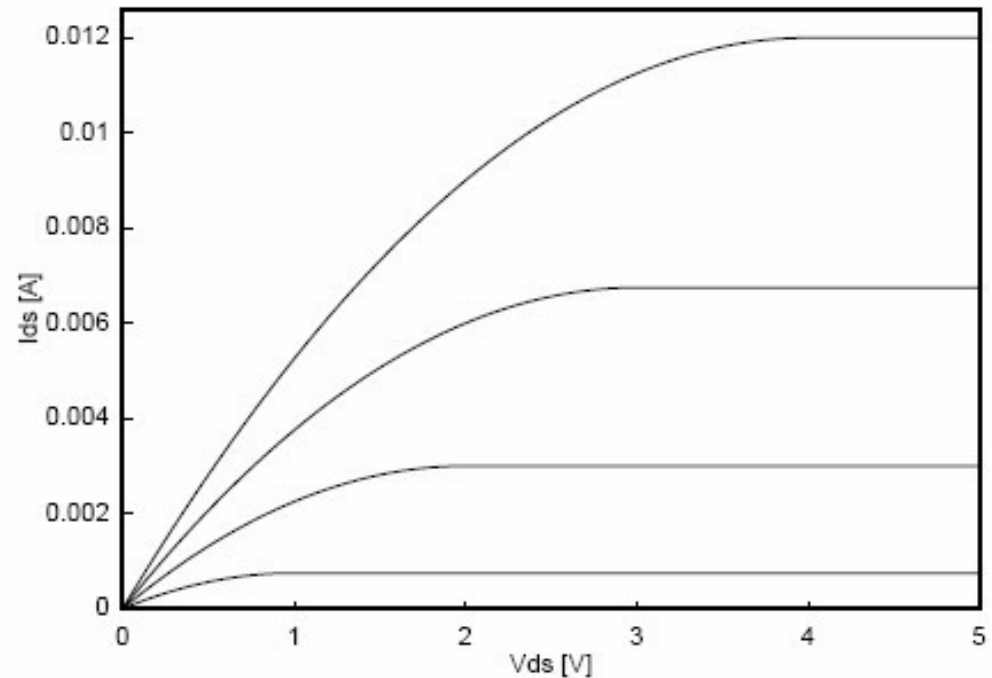
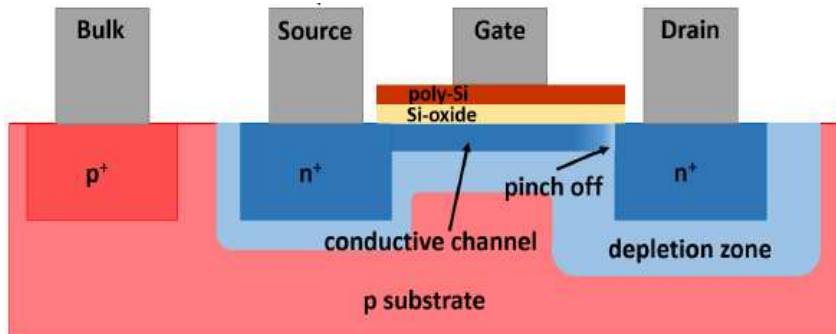


MOSFET (saturation regime)

$$I_{sat} = \frac{Z}{2L} \mu_n C_{ox} (V_{GS} - V_T)^2$$



MOSFET (saturation regime)



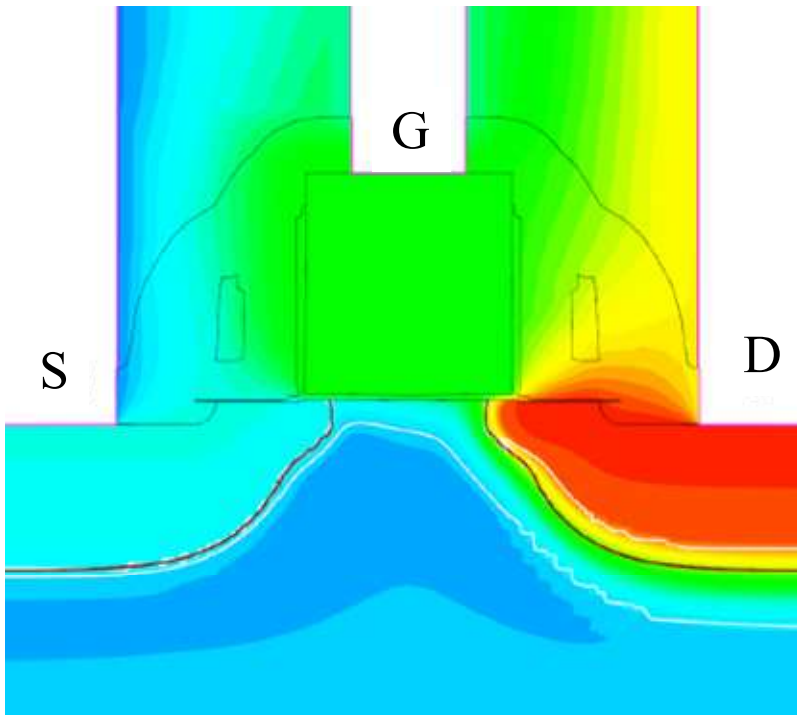
$$I_{sat} = \frac{Z}{2L} \mu_n C_{ox} (V_G - V_T)^2$$

Transconductance

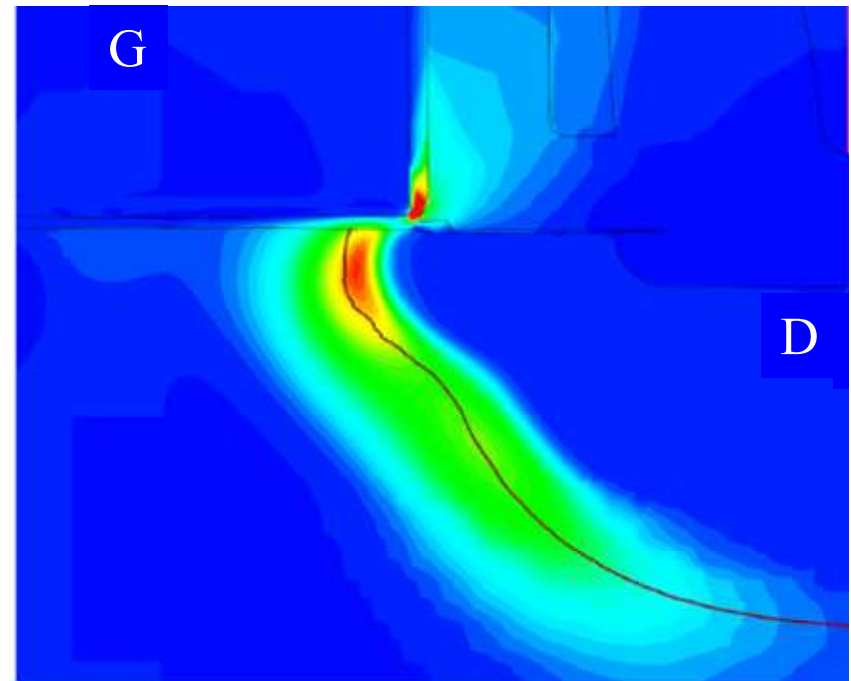
$$g_m = \frac{dI_D}{dV_G} = \frac{Z}{L} \mu_n C_{ox} (V_G - V_T)$$

A MOSFET in the saturation regime acts like a voltage controlled current source.

Saturation



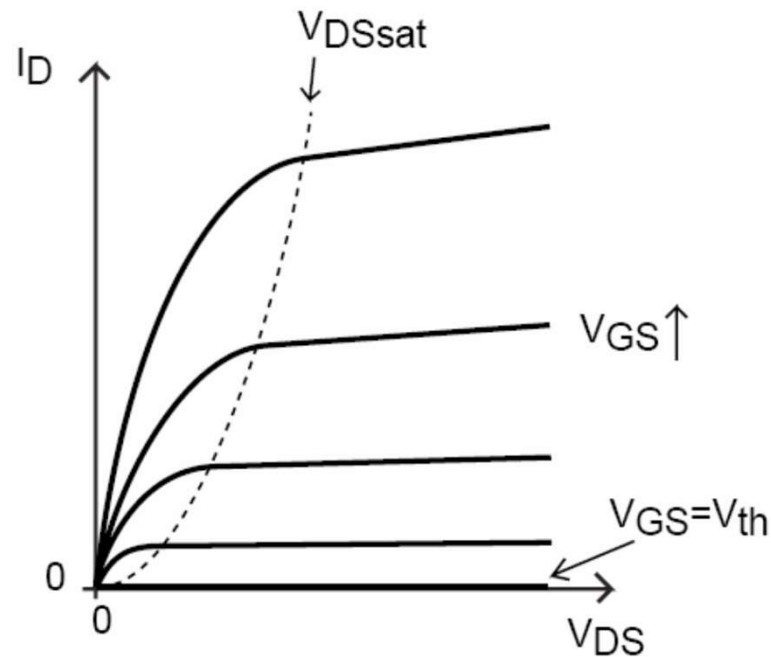
Potential



Electric field strength

MOSFET (saturation regime)

$$I_{sat} = \frac{Z}{2L} \mu_n C_{ox} (V_G - V_T)^2 (1 - \lambda (V_D - V_{sat}))$$



Experimentally: channel length modulation

$$\lambda \propto \frac{1}{L}$$

High frequencies

$$\tilde{i}_{in} = 2\pi f C_G \tilde{v}_G$$

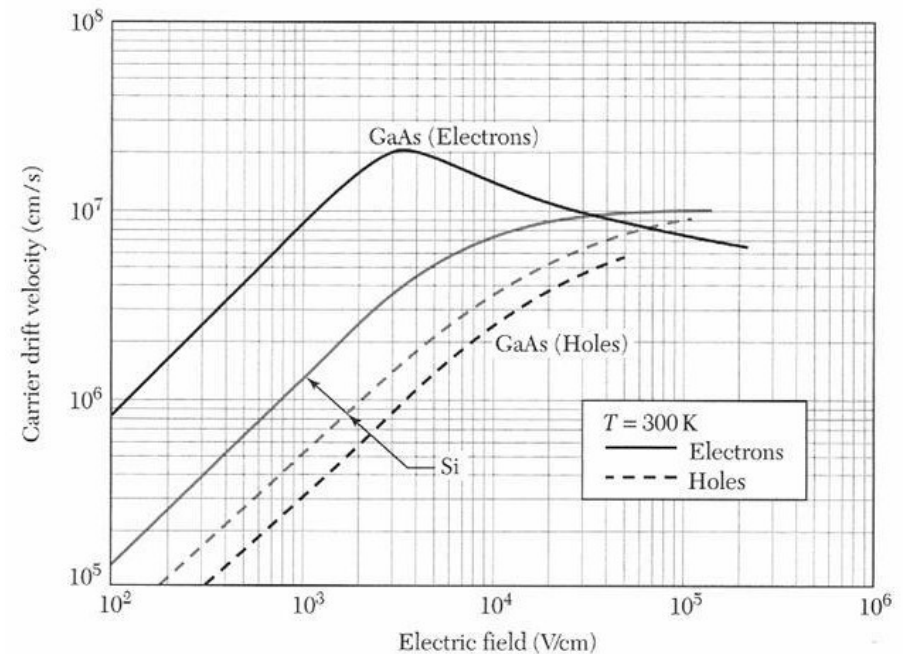
$$\tilde{i}_{out} = g_m \tilde{v}_G$$

$$\tilde{i}_{in} < \tilde{i}_{out}$$

$$f < \frac{g_m}{2\pi C_G} \propto \frac{1}{L^2} = f_T$$

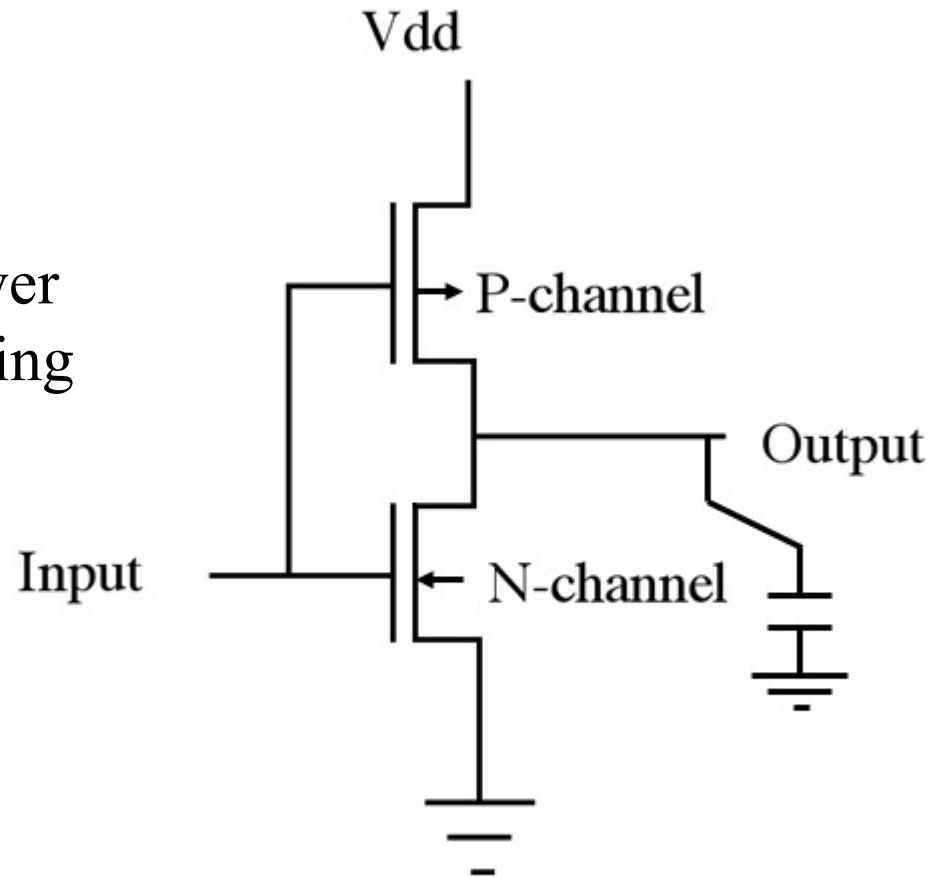
For large E , Ohm's law ($j = ne\mu E$) is not valid. The electron velocity saturates. For velocity saturation:

$$f_T \approx \frac{v_s}{L}$$



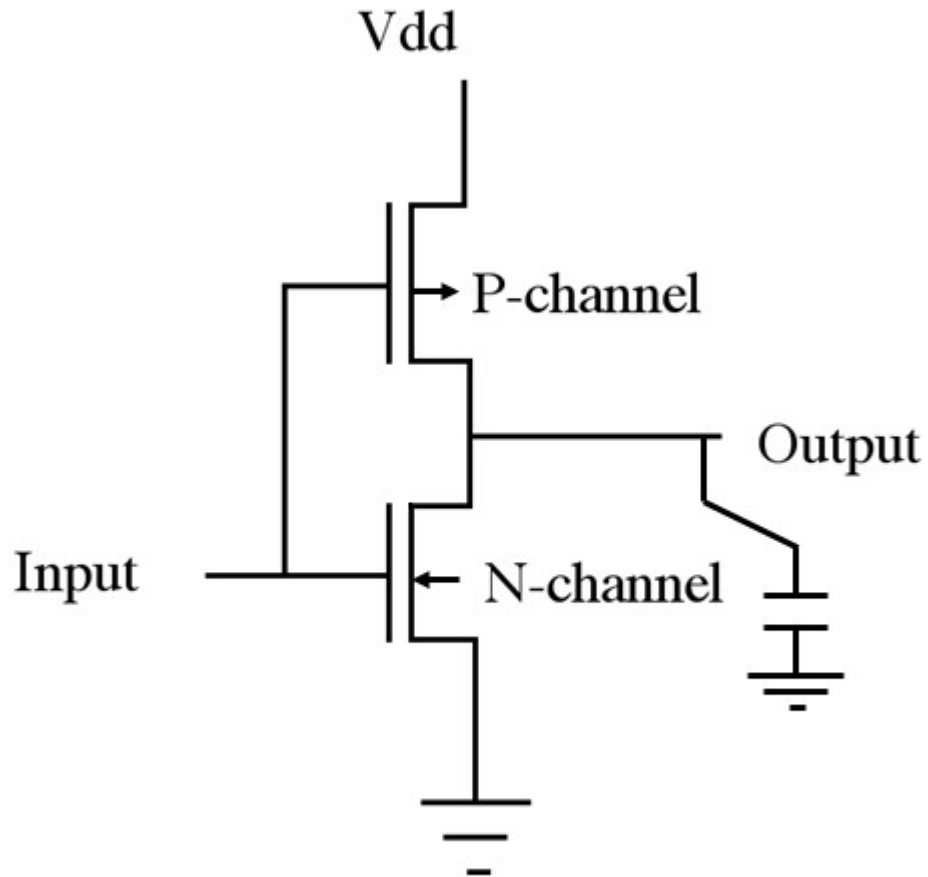
CMOS inverter

Dissipates little power
except when switching

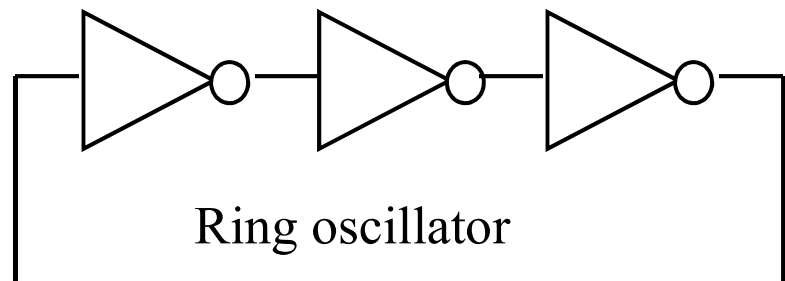


$$E = QV_{dd} = CV_{dd}^2$$

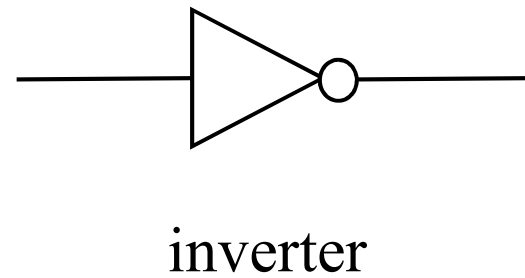
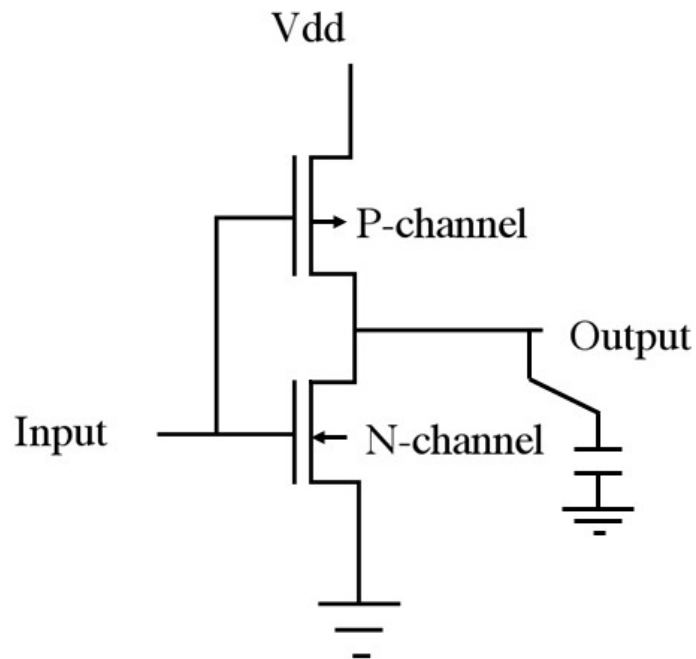
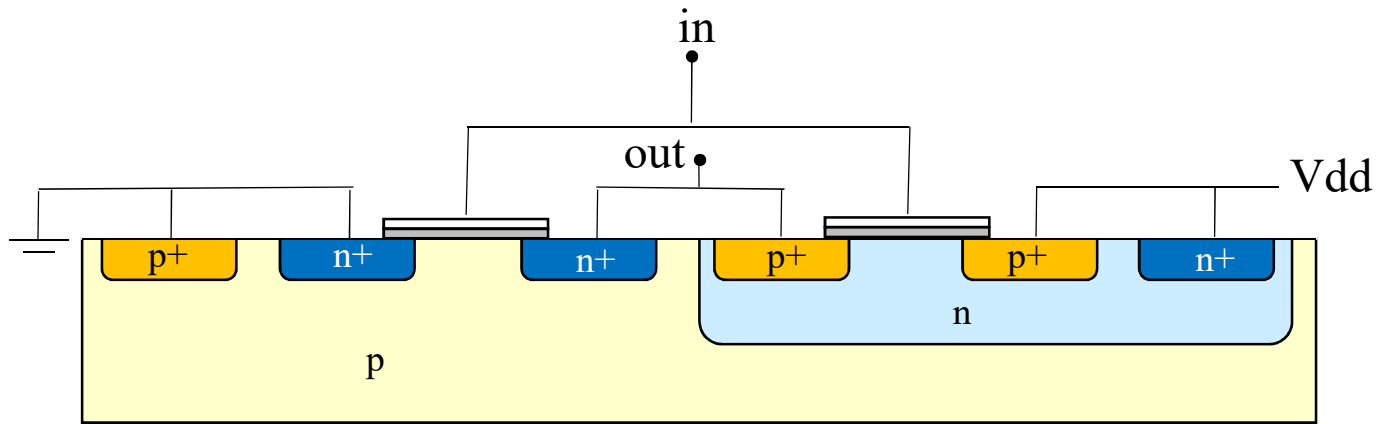
Gate delay



Gate delay is limited by $C_{gate}V_{dd}/I$.



CMOS inverter

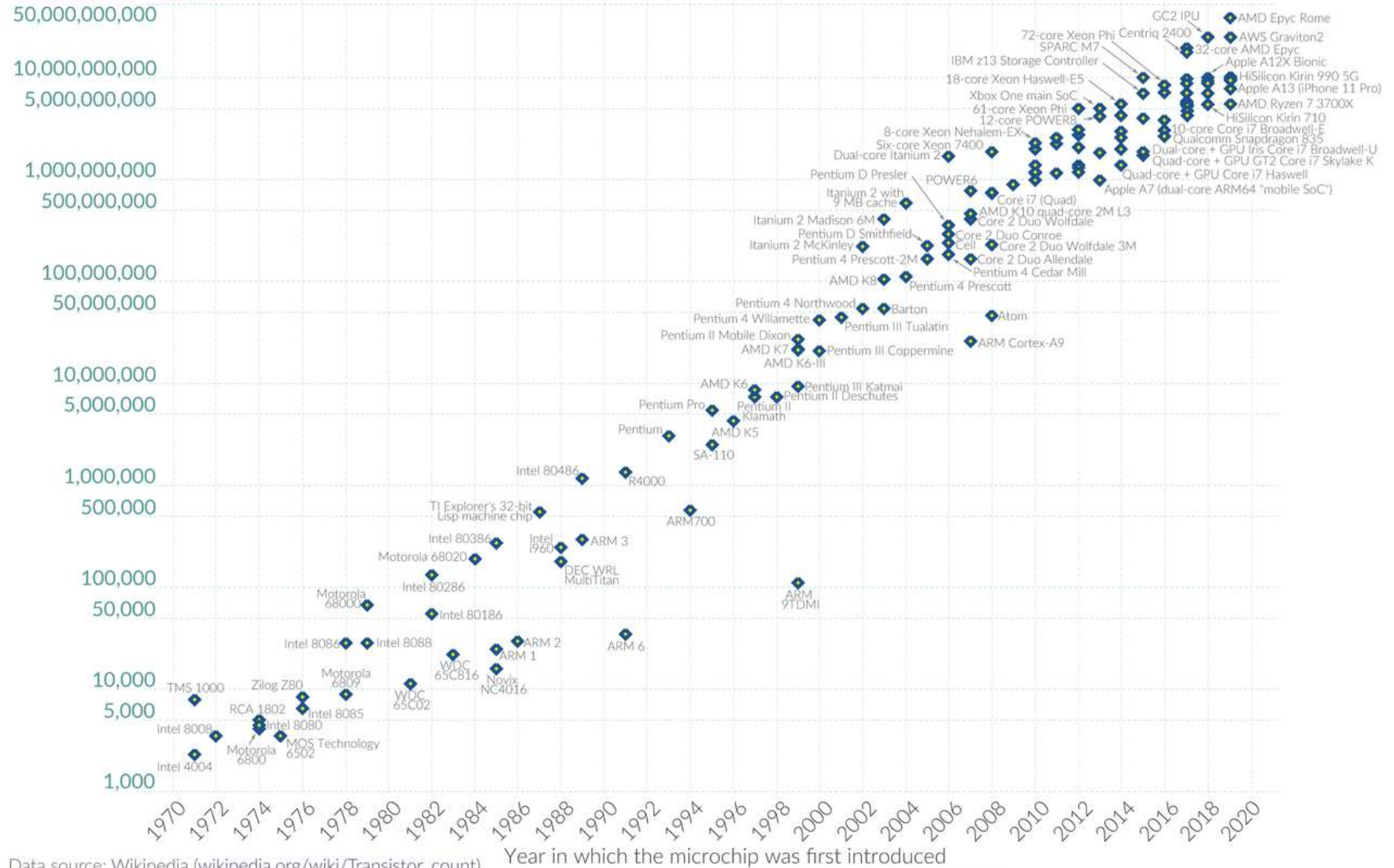


Moore's Law: The number of transistors on microchips doubles every two years



Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important for other aspects of technological progress in computing – such as processing speed or the price of computers.

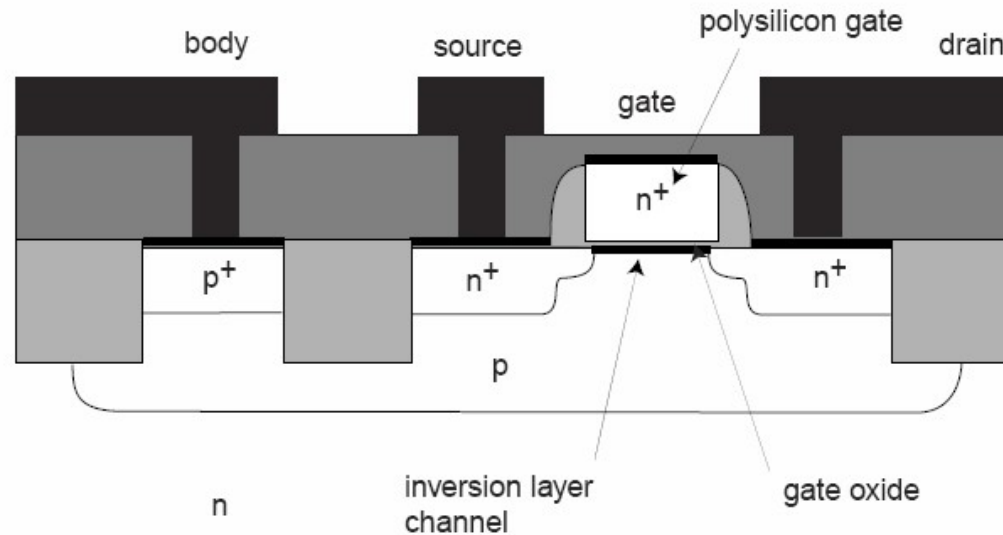
Transistor count



Data source: Wikipedia (wikipedia.org/wiki/Transistor_count)
OurWorldinData.org – Research and data to make progress against the world's largest problems. Licensed under CC-BY by the authors Hannah Ritchie and Max Roser.

By Max Roser, Hannah Ritchie - <https://ourworldindata.org/uploads/2020/11/Transistor-Count-over-time.png>, CC BY 4.0, <https://commons.wikimedia.org/w/index.php?curid=98219918>

Constant E-field Scaling



Gate length L , transistor width Z , oxide thickness t_{ox} are scaled down.

V_{ds} , V_{gs} , and V_T are reduced to keep the electric field constant.

Power density remains constant.

$$L \sim 45 t_{ox}$$

1975 - 1990: "Days of happy scaling"

Constant E-field scaling

$$I_{sat} = \frac{Z}{2L} \mu_n \frac{\epsilon_{ox}}{t_{ox}} (V_G - V_T)^2$$

$$L \Rightarrow sL, \quad Z \Rightarrow sZ, \quad t_{ox} \Rightarrow st_{ox}, \quad V_{th} \Rightarrow sV_{th}$$

$$I_{sat} \Rightarrow sI_{sat} \quad \longleftarrow \quad I_{sat} \text{ gets smaller}$$

$$g_m = \frac{dI_D}{dV_G} = \frac{Z}{L} \mu_n \frac{\epsilon_{ox}}{t_{ox}} (V_G - V_T) \quad \longleftarrow \quad \text{Transconductance stays the same.}$$

Power per transistor decreases like L^2 . Power per unit area remains constant.

The heat dissipation problem

Microprocessors are hot ~ 100 C

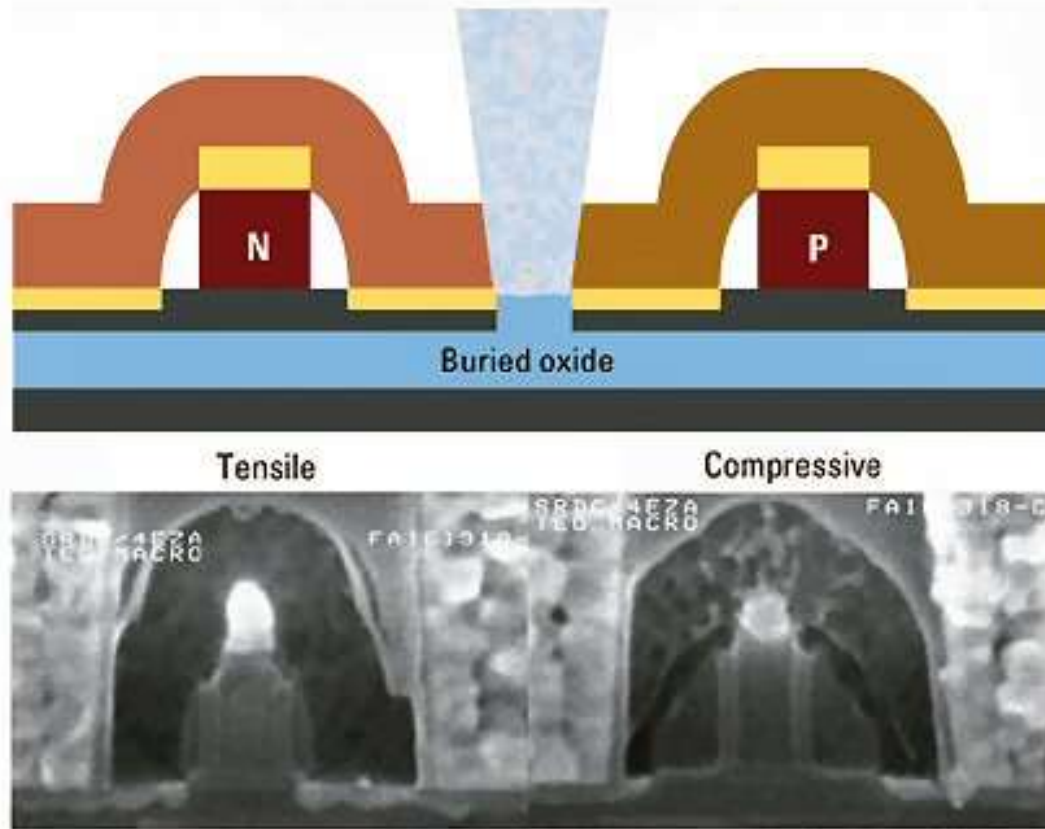
Hotter operation will cause dopants to diffuse

When more transistors are put on a chip they must dissipate less power.

Power per transistor decreases like L^2 .

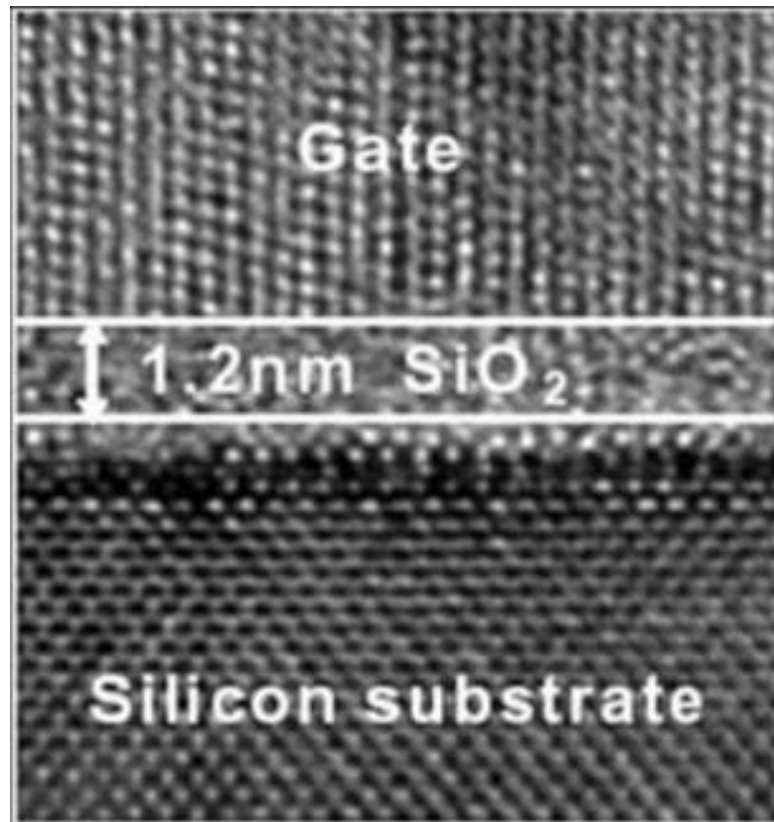
Dual stress liners

DUAL STRESS LINER TRANSISTOR CROSS-SECTION



Tensile silicon nitride film over the NMOS and a compressive silicon nitride film over the PMOS improves the mobility.

Gate dielectric

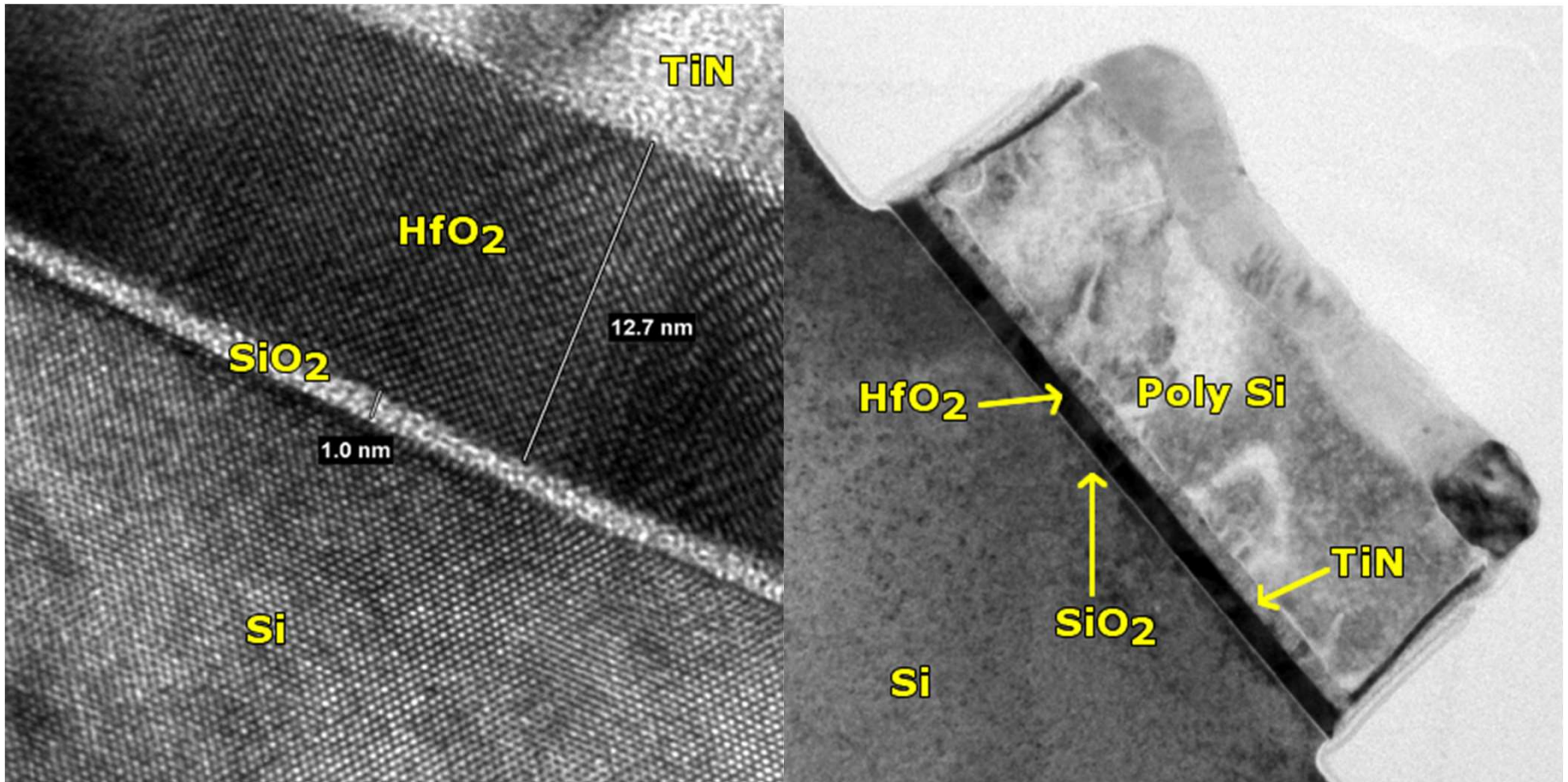


Thinner than 1 nm:
electrons tunnel

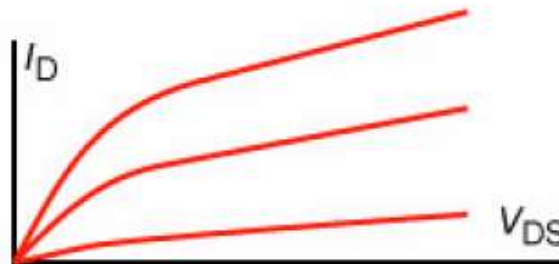
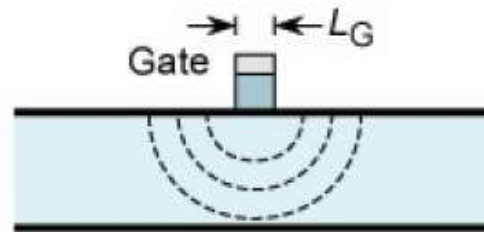
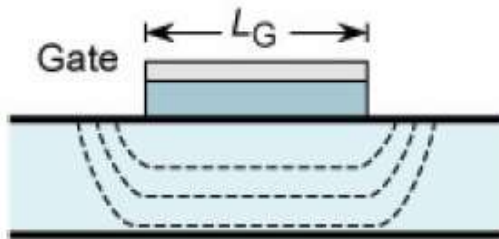
Large dielectric
constant desirable
 $\epsilon_r(\text{SiO}_2) \sim 4$

$\epsilon_r(\text{Si}_3\text{N}_4) \sim 7$

High-k dielectrics



Short channel effects



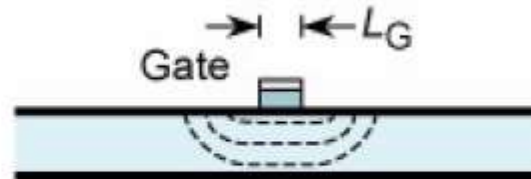
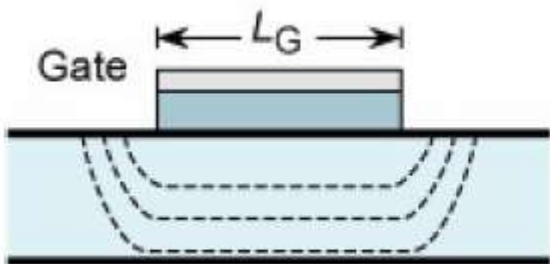
Short-channel effects:

Threshold-voltage shift

Lack of pinch-off

Increased leakage current

Increase of output conductance



SOI: silicon on insulator

CMOS SOI

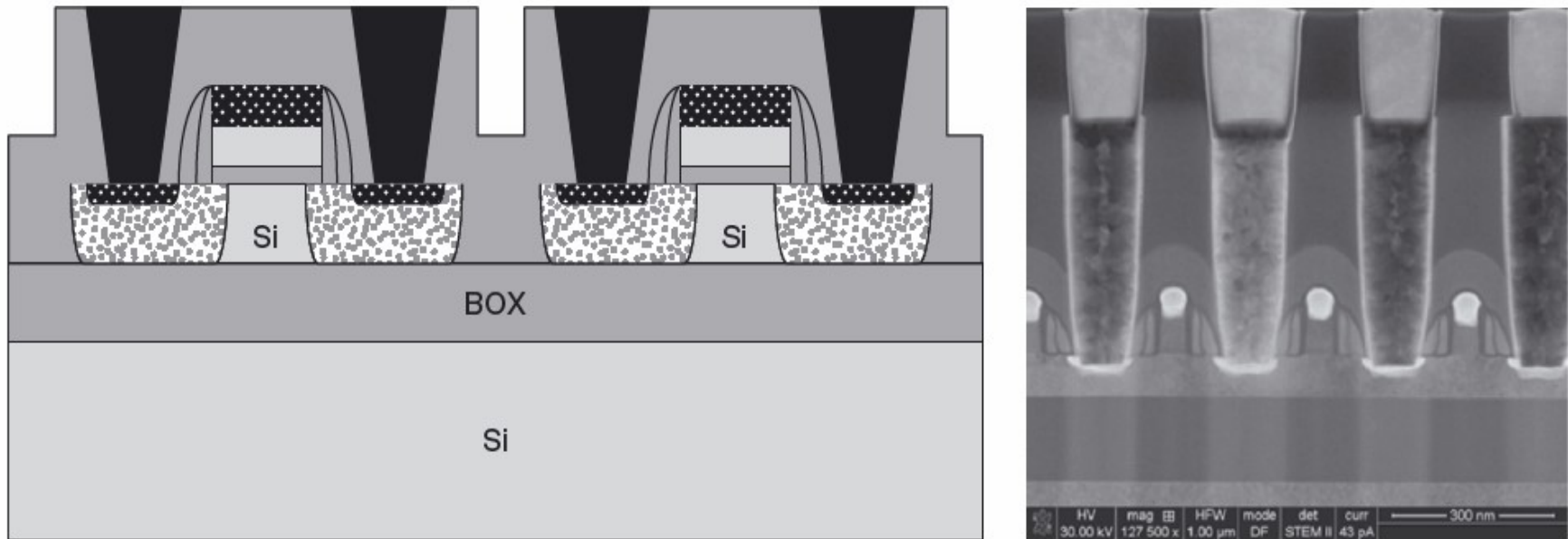
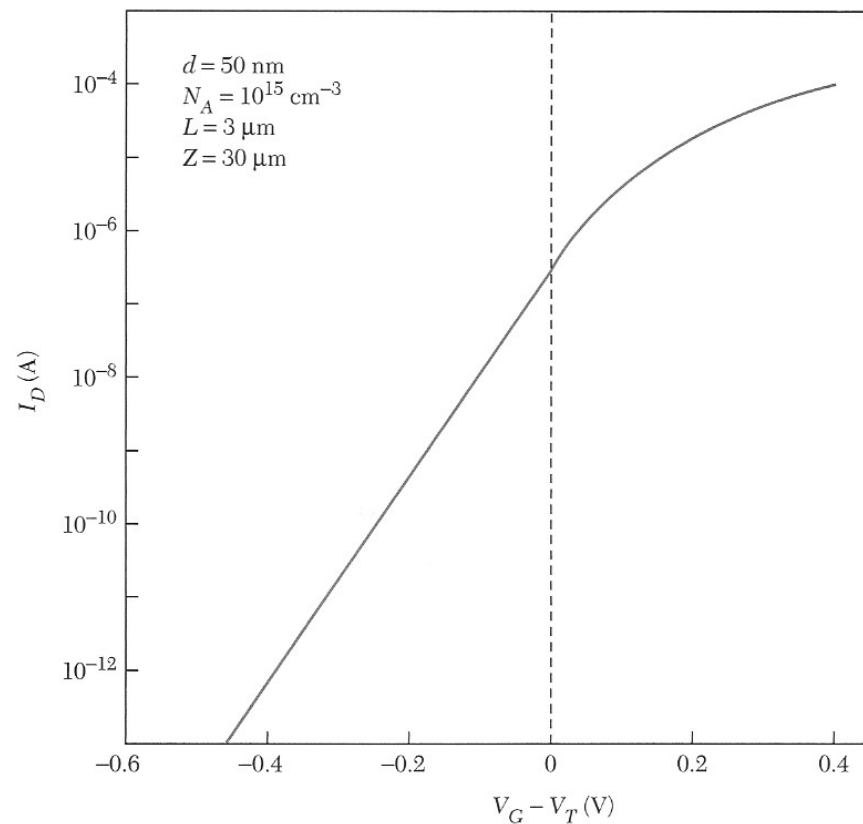


Figure 26.16 SOI MOSFET with first-level metal, schematic and TEM. Courtesy Brandon Van Leer, FEI Company⁴

Fransila

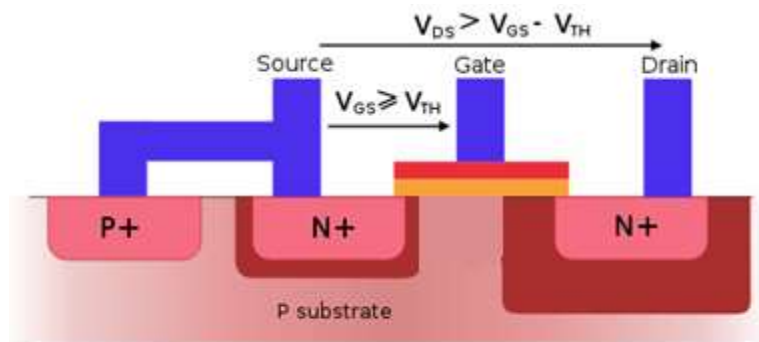
Subthreshold current

For $V_G < V_T$ the transistor should switch off but there is a diffusion current. The current is not really off until ~ 0.5 V below the threshold voltage.



Weak inversion

$$I_D \propto \exp\left(\frac{e(V_G - V_T)}{k_B T}\right)$$

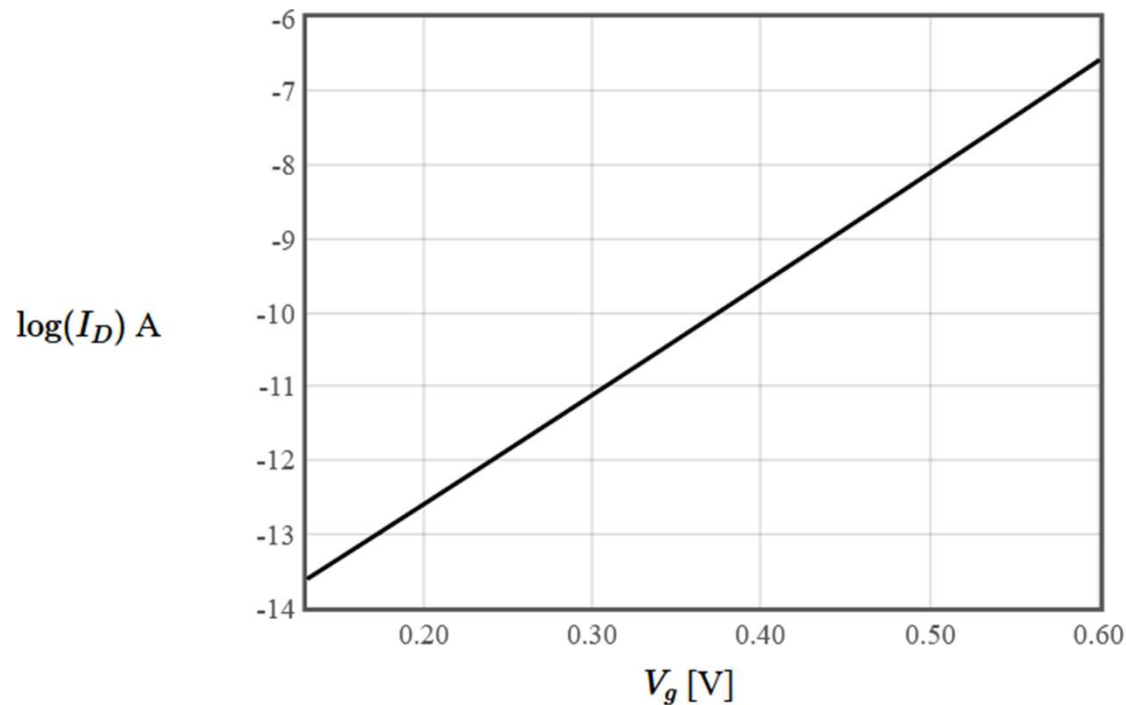


Subthreshold slope: 70-100 mV/decade

Subthreshold current

$$x_p = -\frac{\epsilon_s}{\epsilon_{ox}} t_{ox} + \sqrt{\left(\frac{\epsilon_s}{\epsilon_{ox}} t_{ox}\right)^2 + \frac{2\epsilon_s}{eN_A} (V_g - V_{fb})}$$

$$I_D \approx \frac{k_B T \mu W n_{2d}}{L} = \frac{n_i^2 \mu \epsilon_s k_B^2 T^2 W}{e^2 N_A^2 x_p L} \exp\left(\frac{e^2 N_A x_p^2}{2\epsilon_s k_B T}\right)$$

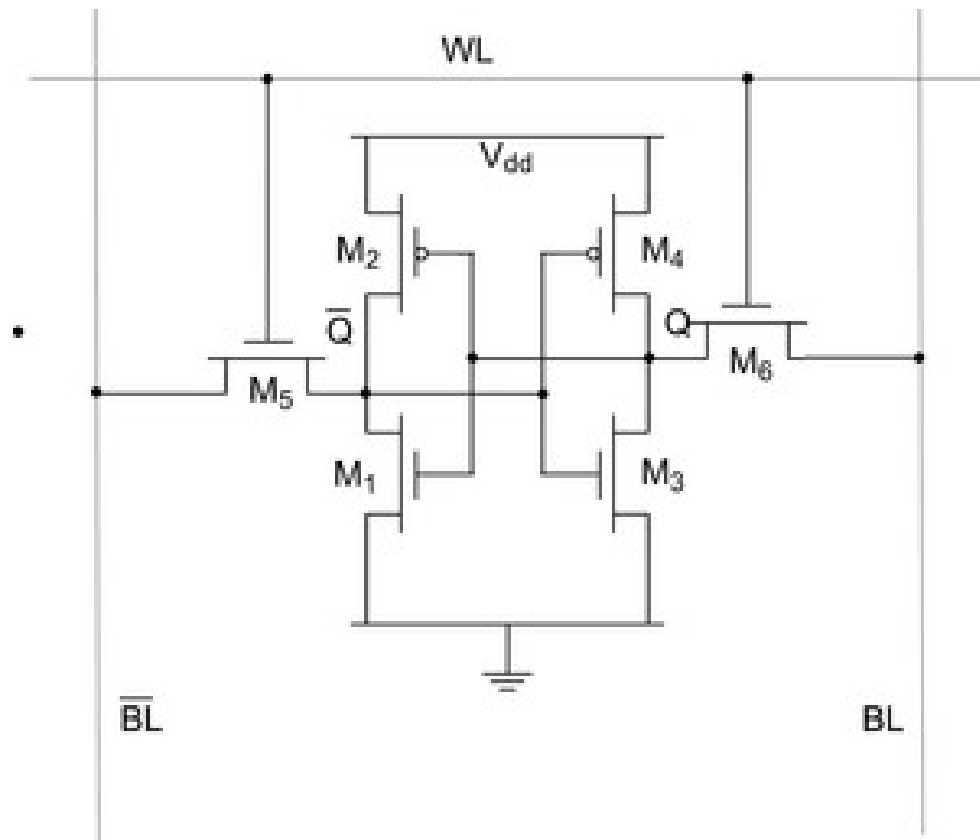
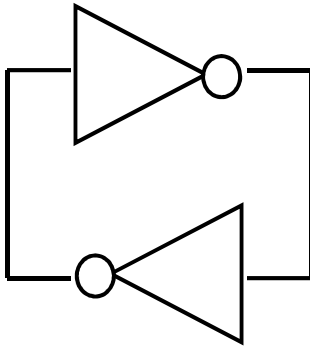


Subthreshold slope: 66 mV/decade

Memories

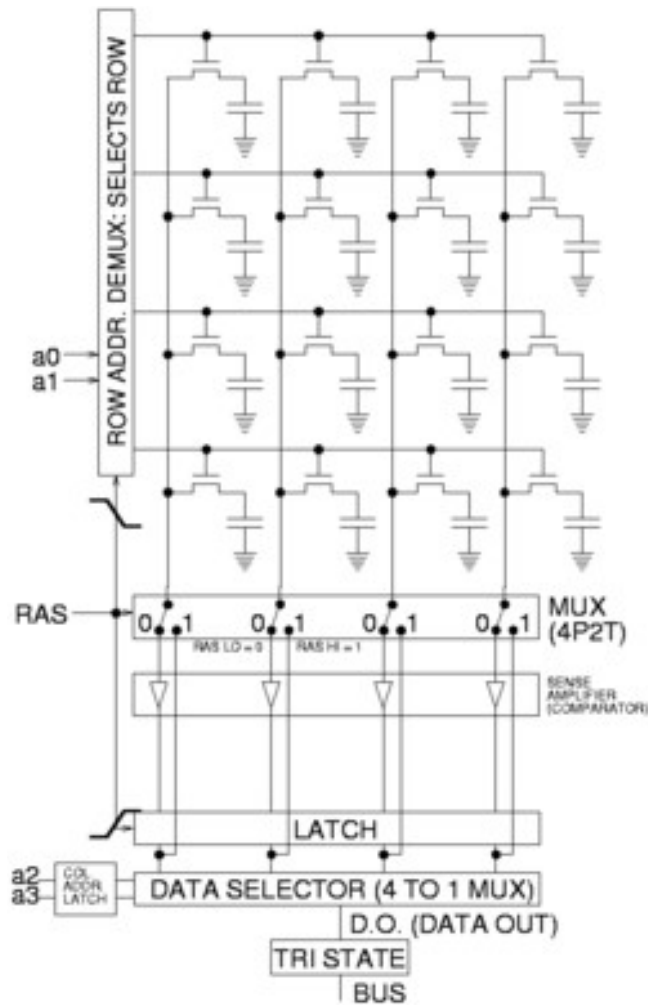
SRAM

Static random access memory



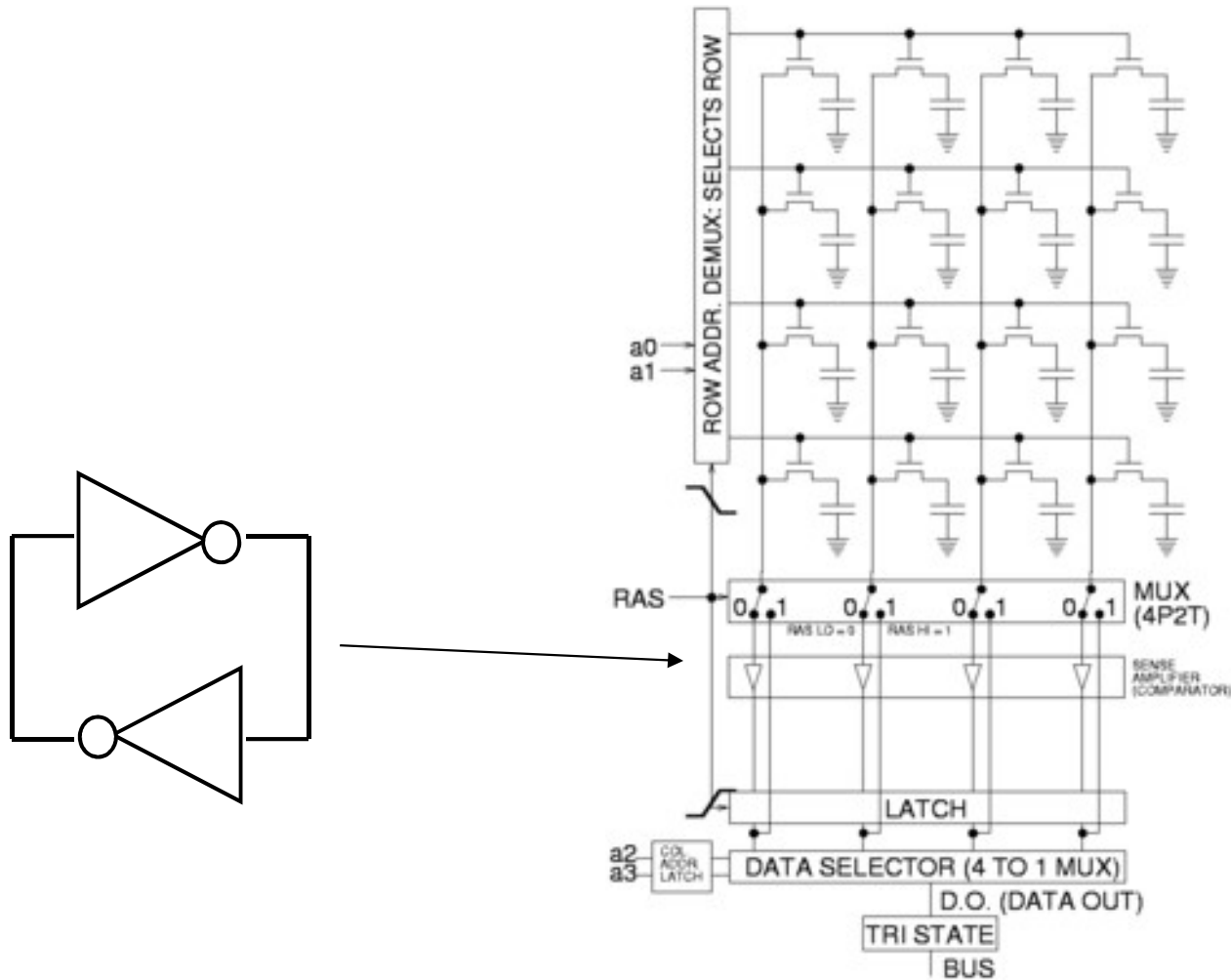
DRAM

Dynamic random access memory

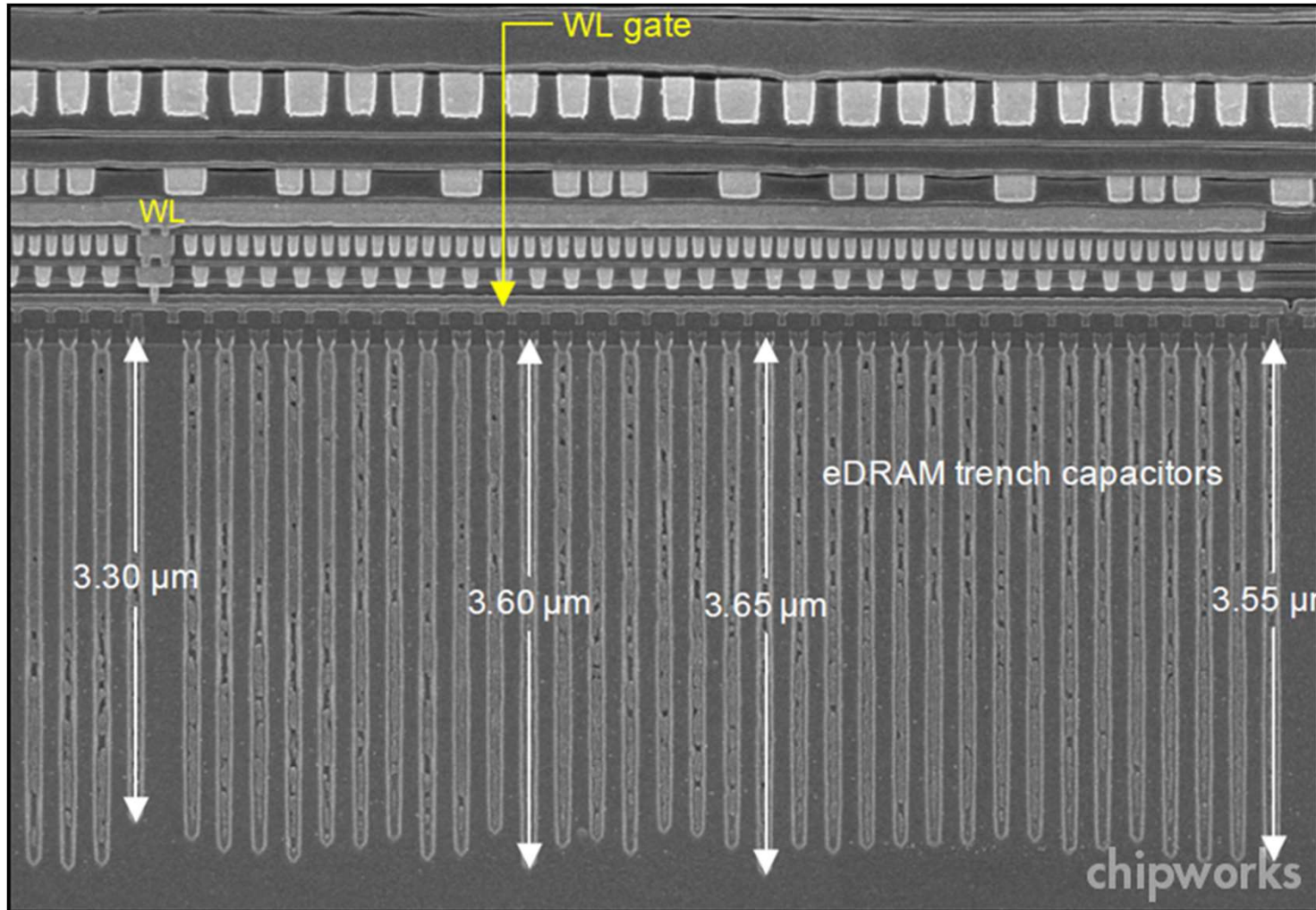


DRAM

Read and refresh DRAM with a SRAM cell



DRAM

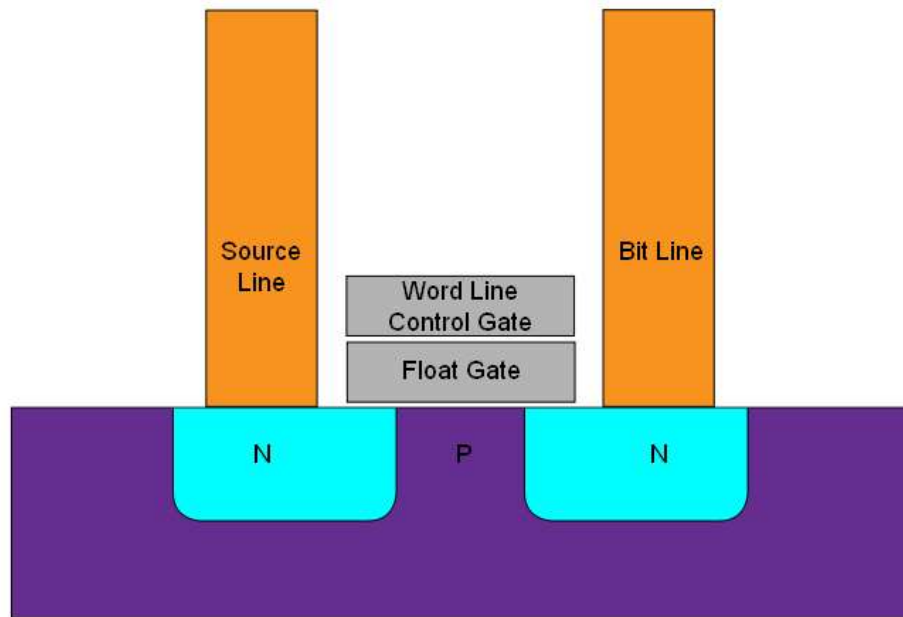


75:1

Silicon oxynitride SiO_xN_y dielectric

http://electroi.com/chipworks_real_chips_blog/

Flash memory



Charge is stored on a floating gate

nonvolatile