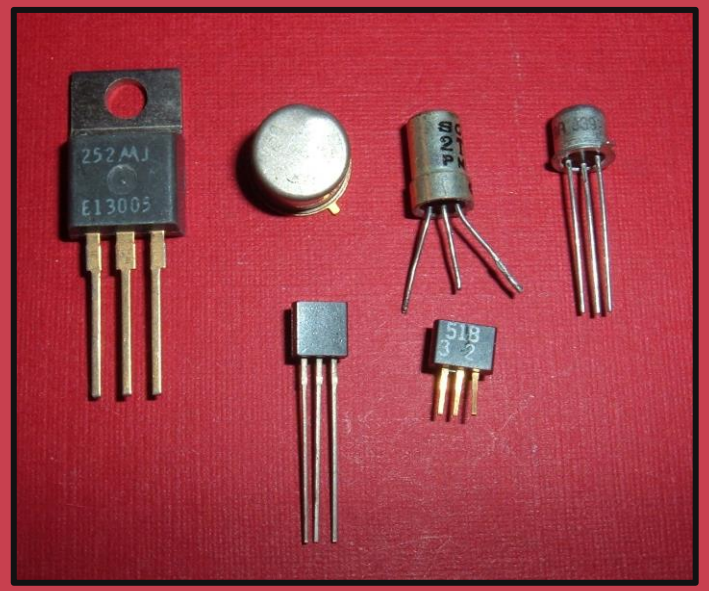
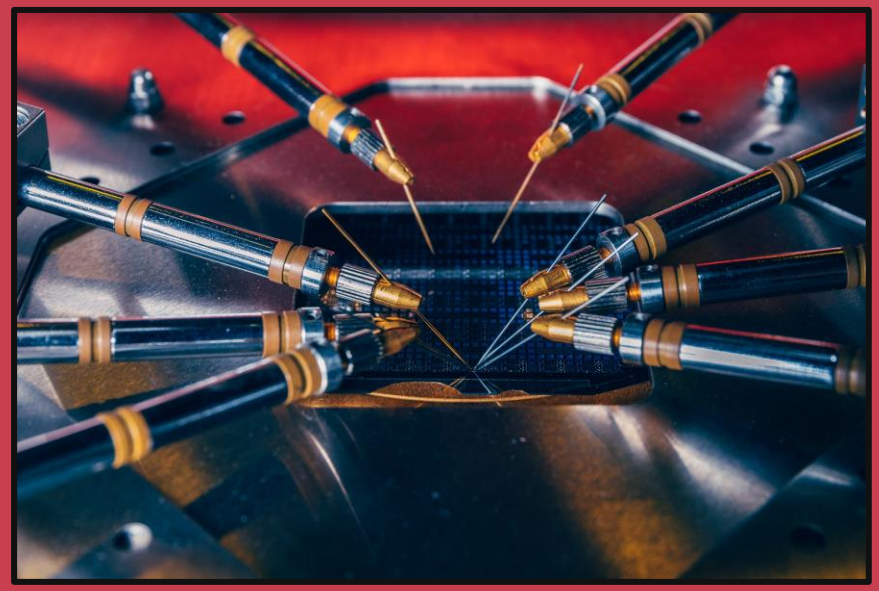


https://commons.wikimedia.org/wiki/File:Transistors.agr.jpg



https://www.k-ai.at/wp-content/uploads/2023/11/K-AI_imagebilder_30082023_519.jpg

Physics of semiconductor devices

Karin Zojer

October 1, 2025

Physics of semiconductor devices

- Diodes, solid state lasers, transistors
- Computing, communications
- Controllers: vacuum cleaners, coffee makers, etc.
- Transportation, autonomous driving, electric cars
- Efficient lighting, solar cells, displays
- Lasers

course material online

http://lampz.tugraz.at/~hadley/psd/outline/outline.php

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PHT.301 Physics of Semiconductor Devices

Outline

- **Introduction**
  - Semiconductors, transistors, and the electronics industry
- **Semiconductor crystals**
  - Energy bands W
    - Crystal structure W
    - Bravais lattice W
    - Miller indices W
    - Examples of crystal structures W
      - silicon, GaN (wurzite), SiC 4H, ZnO (wurzite), diamond
      - simple cubic, fcc, bcc, hcp, zincblende
    - Wave and particle nature of electrons
    - k-space
    - Density of states W Some examples: Al fcc, Au fcc, Cu fcc, Pt fcc, W bcc, Si diamond, Grap
    - Pauli exclusion principle W
    - Fermi function W
    - Fermi energy W
    - Metals, semiconductors, and insulators
    - Metal band structure
    - Semiconductor band structure
  - Absorption and emission of photons
  - Direct and indirect band gaps W
- **Intrinsic semiconductors**
  - Conduction band
  - Valence band
  - Effective mass W
  - Holes W
  - Boltzmann approximation
  - Law of mass action W
  - Fermi energy of an intrinsic semiconductor ▶ EN 2:36
  - Intrinsic semiconductors with a split-off band

Examination

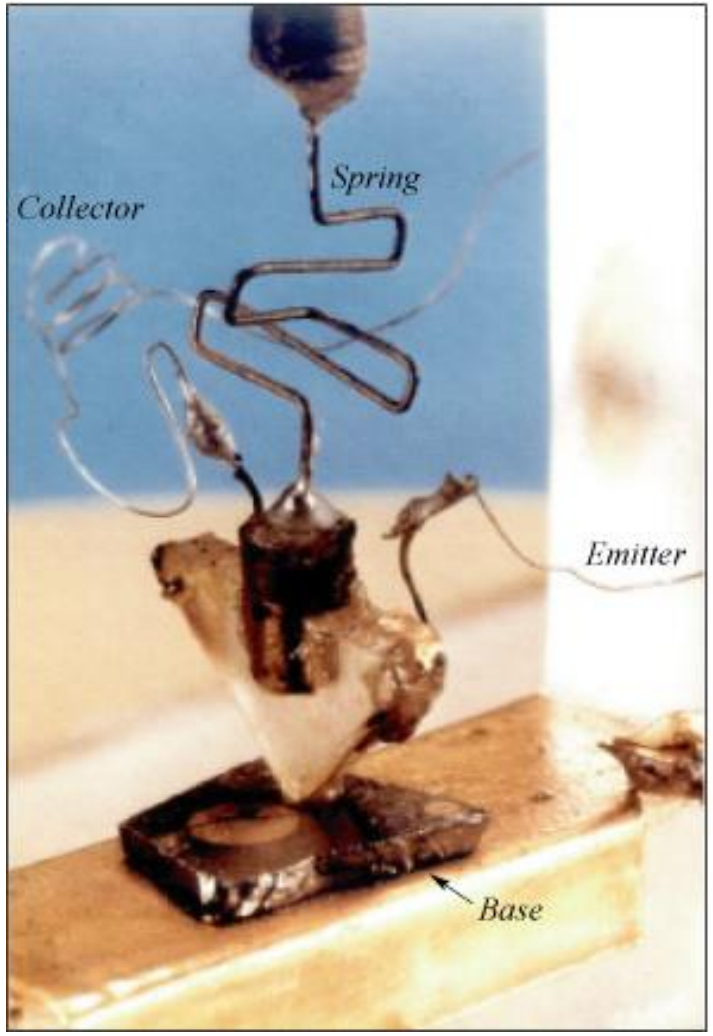
1 hour written exam

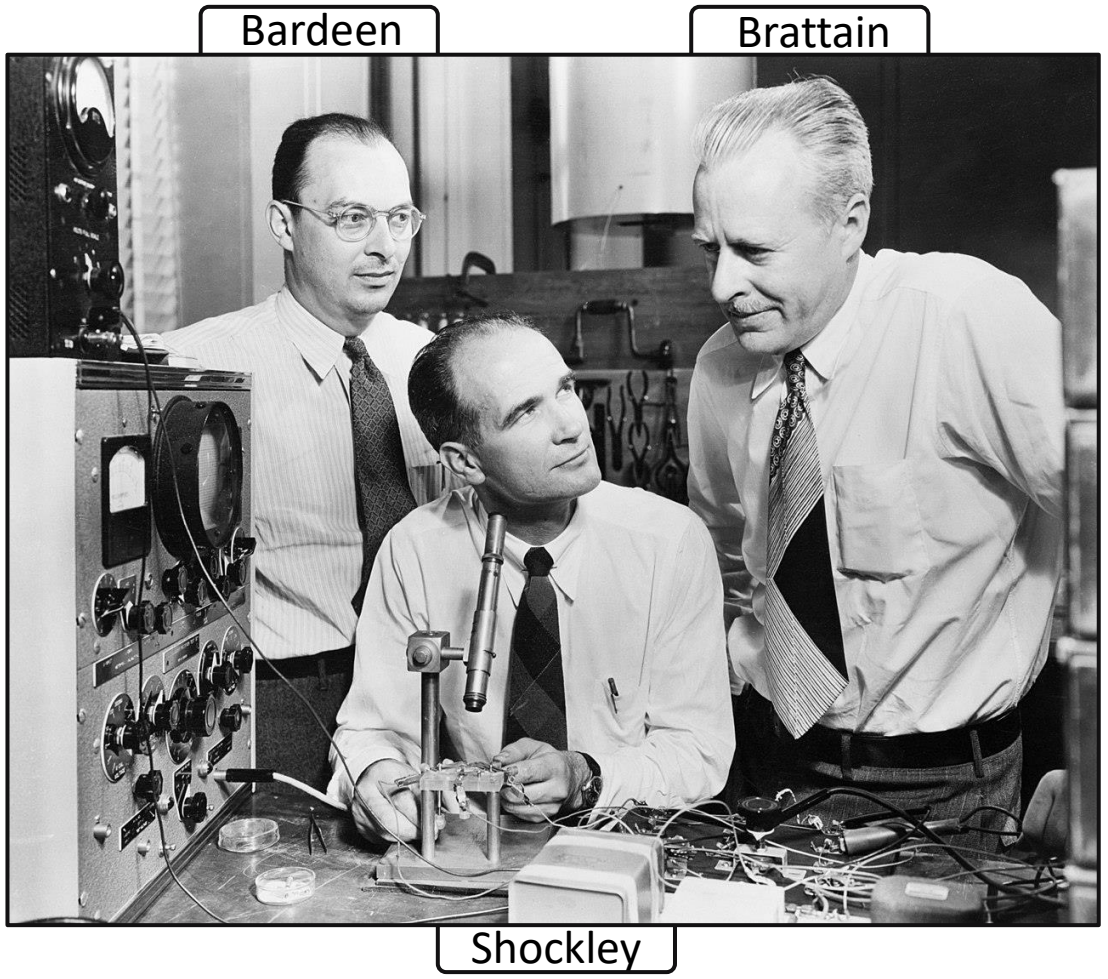
one page of handwritten notes

Oral exam

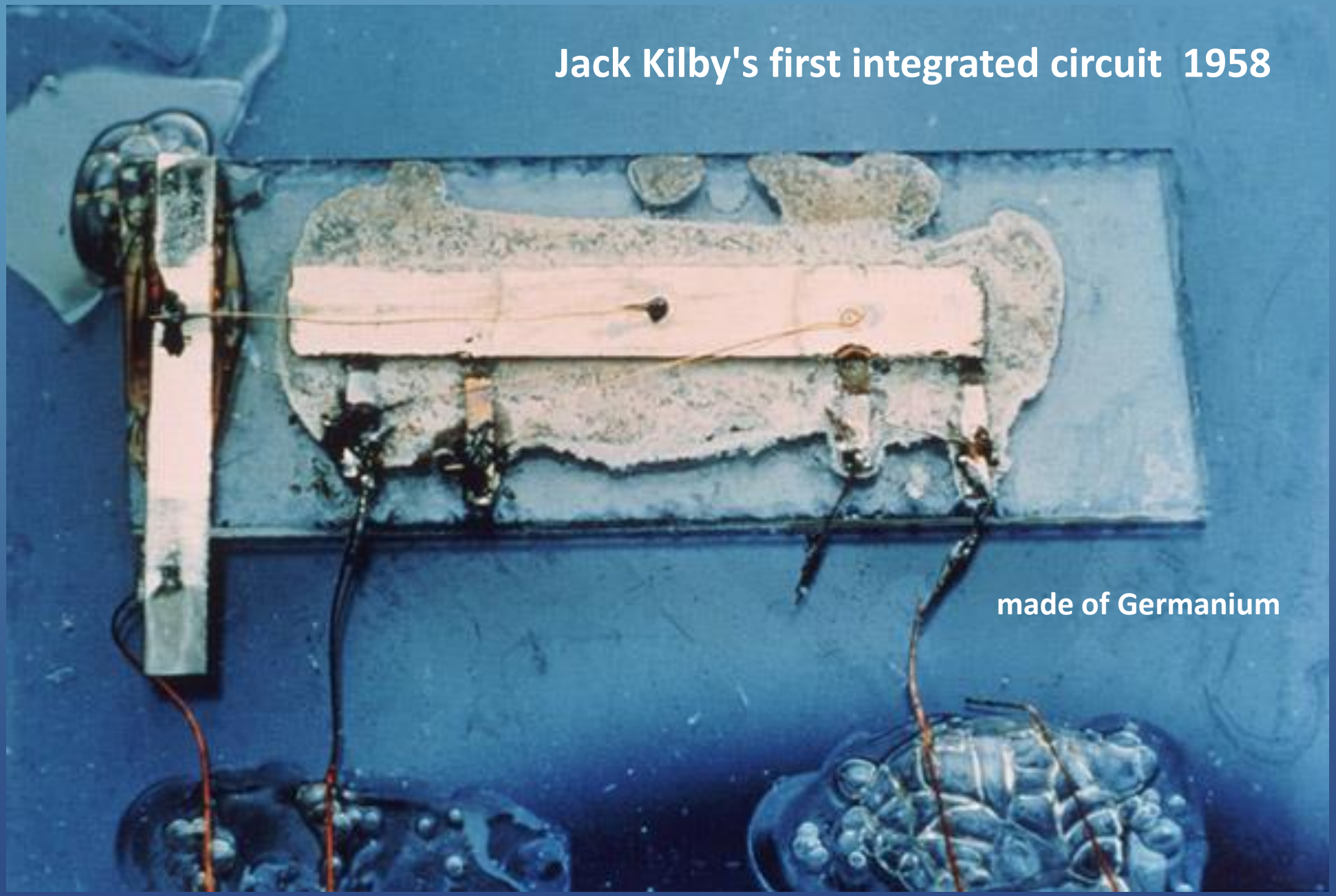
The first point contact transistor

William Shockley, John Bardeen, and Walter Brattain
Bell Laboratories, Murray Hill, New Jersey (1947)



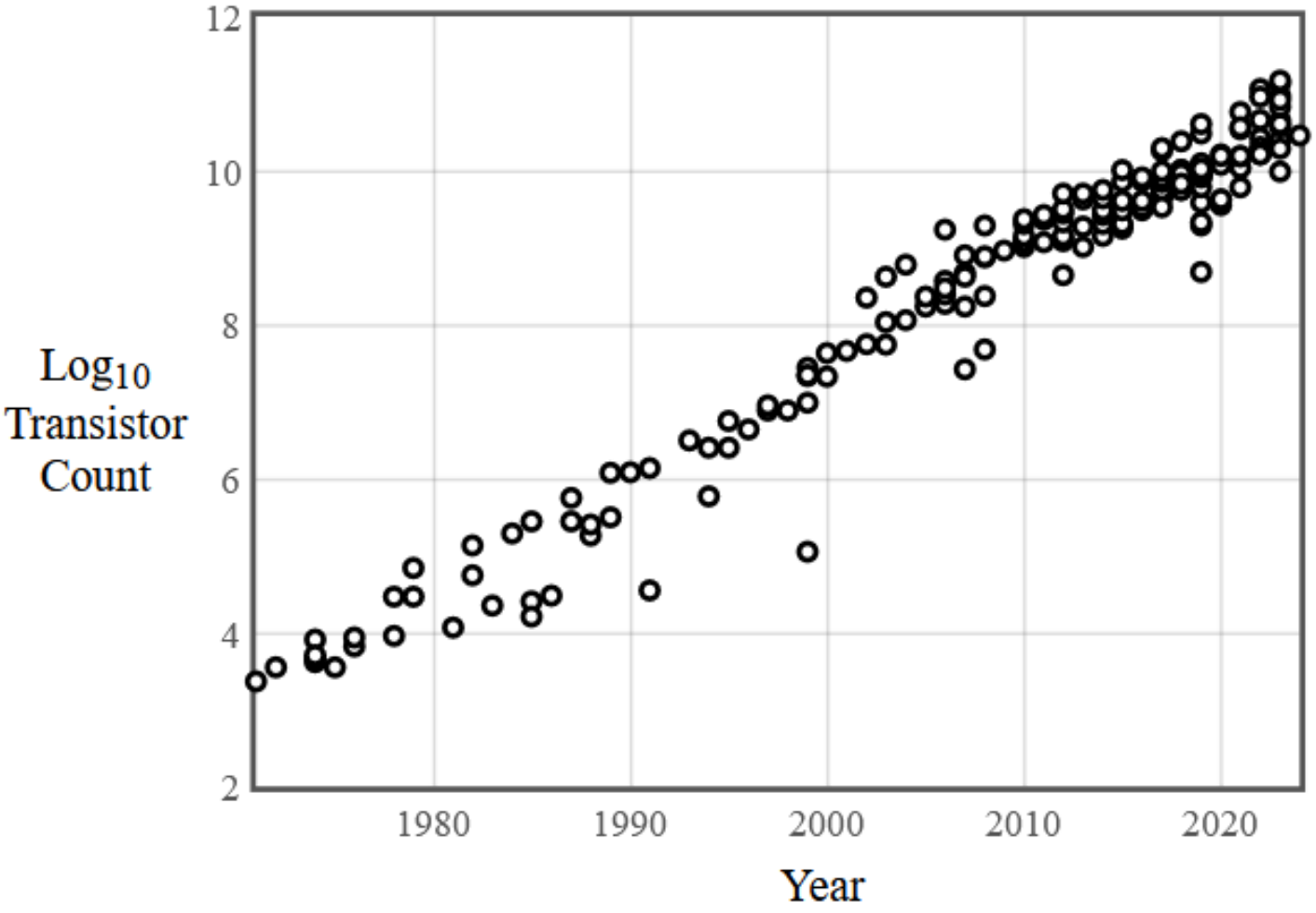


https://upload.wikimedia.org/wikipedia/commons/thumb/c/c2/Bardeen_Shockley_Brattain_1948.JPG/1280px-Bardeen_Shockley_Brattain_1948.JPG



https://education.ti.com/-/media/ti/education/images/education/success-story/jkd_jack-kilby.jpg?rev=36d0400f-168f-4250-b39d-1fe578d6ea93&la=en&h=302&w=450&hash=1C1E153346E70FEA65FE87001EC7E12E

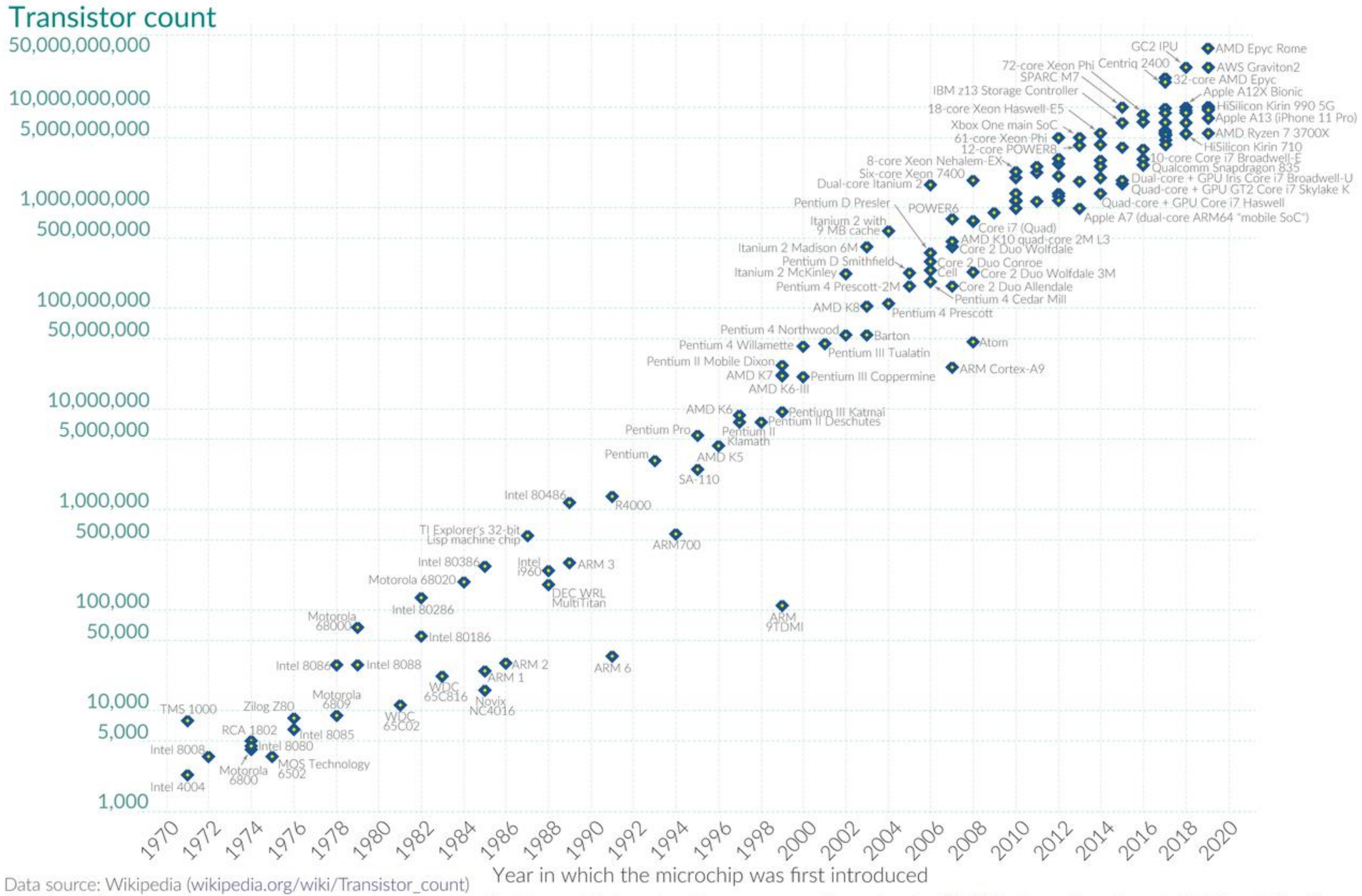
Transistor Count 2023



Data from Wikipedia: Transistor Count (no data released for 2025 yet)

Moore's Law: The number of transistors on microchips doubles every two years

Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important for other aspects of technological progress in computing – such as processing speed or the price of computers.

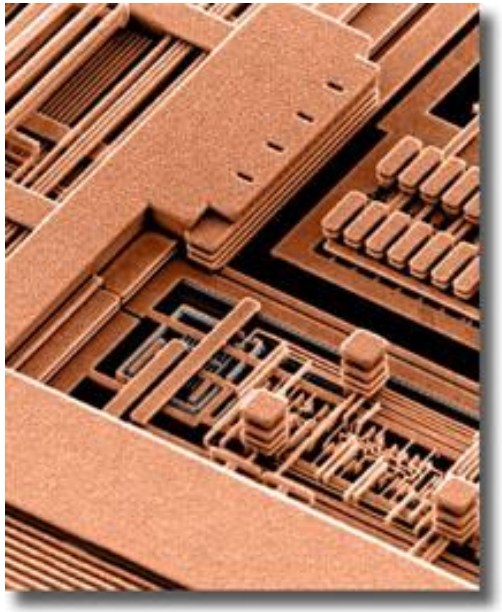


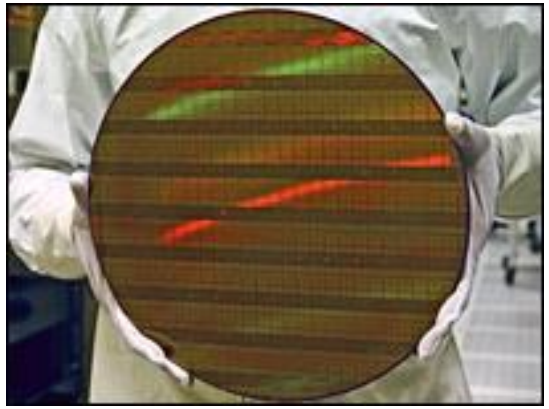
Data source: Wikipedia (wikipedia.org/wiki/Transistor_count)

OurWorldinData.org – Research and data to make progress against the world's largest problems.

Licensed under CC-BY by the authors Hannah Ritchie and Max Roser.

A lot of transistors – tightly packed





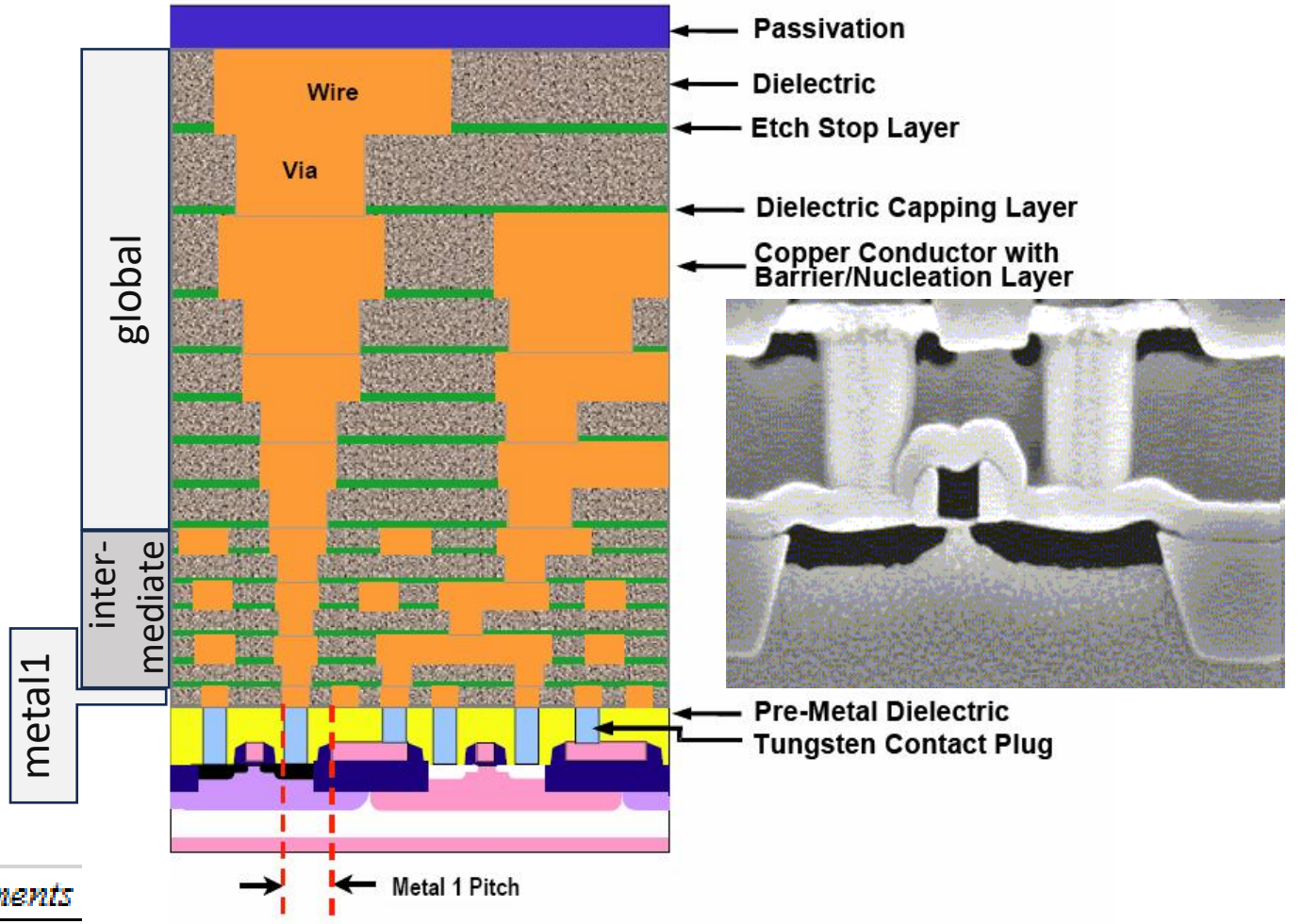
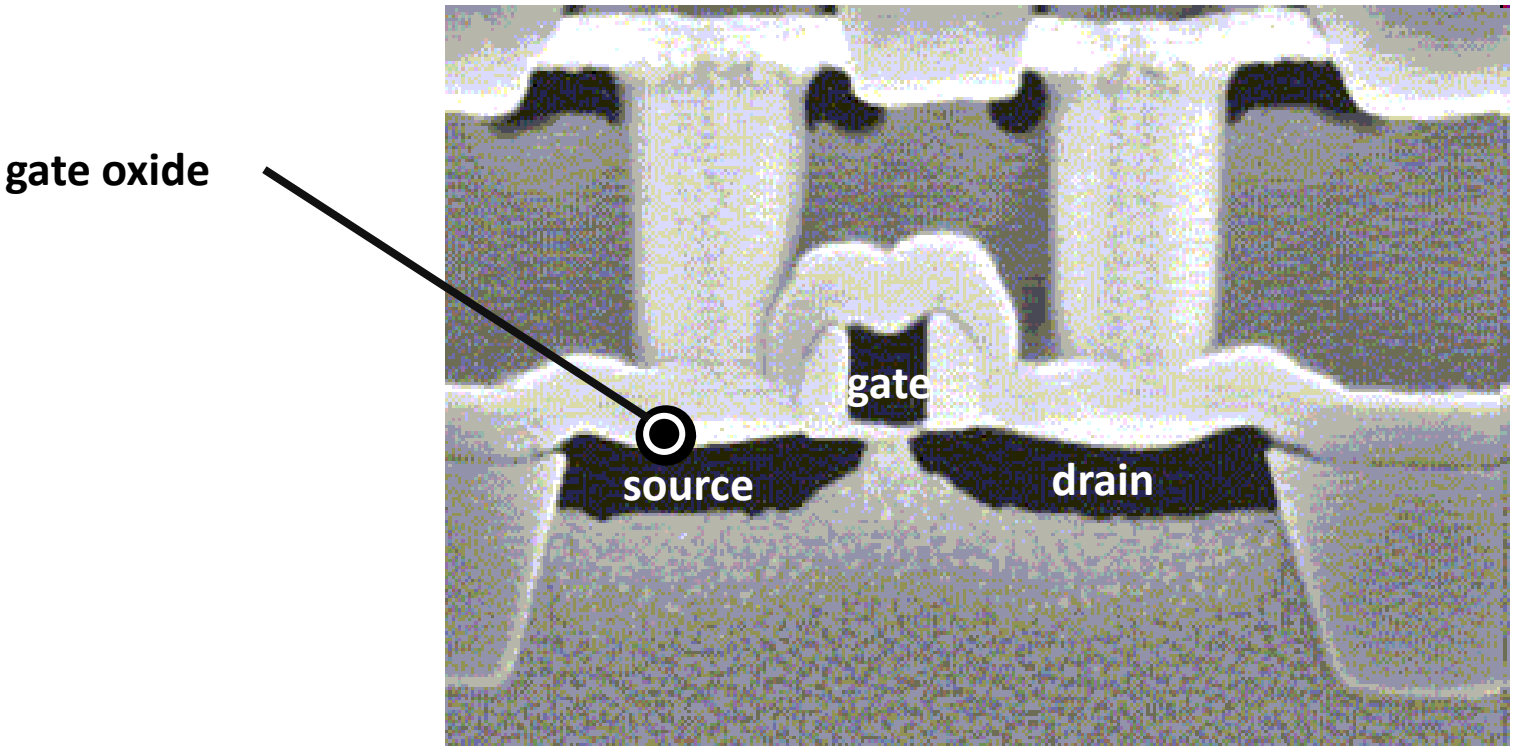
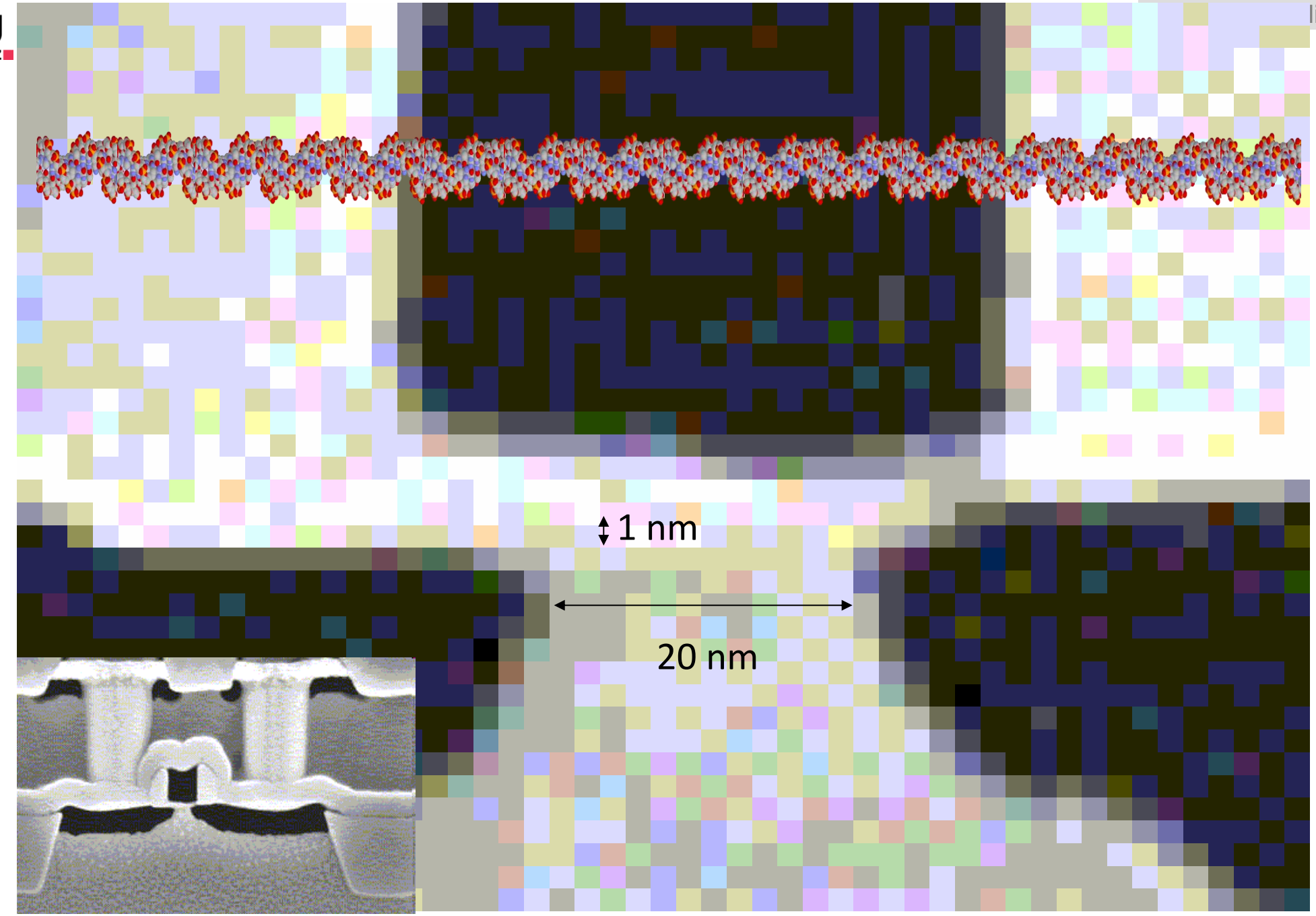


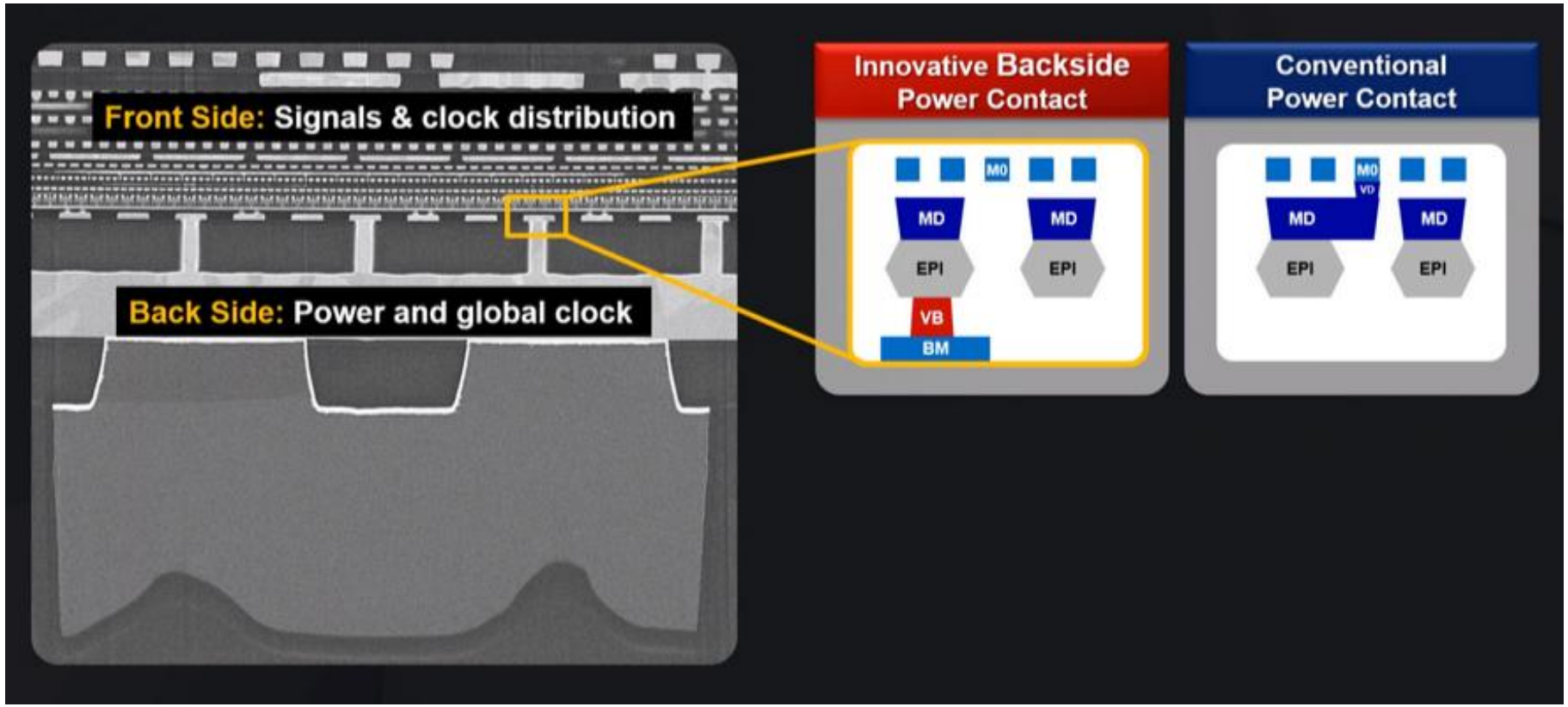
Table PIDS2a High-performance (HP) Logic Technology Requirements

	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028
	"16/14"		"11/10"		"8/7"		"6/5"		"4/3"		"3/2.5"		"2/1.5"		"1/0.75"	
node	40	32	32	28.3	25.3	22.5	20.0	17.9	15.9	14.2	12.6	11.3	10.0	8.9	8	7.1
metal 1/2 pitch	20	18	16.7	15.2	13.9	12.7	11.6	10.6	9.7	8.8	8.0	7.3	6.7	6.1	5.6	5.1
gate length	16.0	14.4	13.4	12.2	11.1	10.2	9.3	8.5	7.8	7.0	6.4	5.8	5.4	4.9	4.5	4.1

MOSFET are very small already




DNA
MOSFET
1 nm
20 nm


Front Side: Signals & clock distribution
Back Side: Power and global clock
Innovative Backside Power Contact
MD
MD
MD
EPI
EPI
VB
BM
Conventional Power Contact
MD
VD
MD
MD
EPI
EPI

https://irds.ieee.org

INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS™

INTERNATIONAL
ROADMAP
FOR
DEVICES AND SYSTEMS

2017 EDITION

EXECUTIVE SUMMARY

1. Application Benchmarking (AB)
2. Systems and Architectures (SA)
3. Outside System Connectivity (OSC)
4. More Moore (MM) ⬅
5. Beyond CMOS (BC) ⬅
6. Packaging Integration (PI)
7. Factory Integration (FI)
8. Lithography (L)
9. Emerging Research Materials (ERM) ⬅
10. Yield Enhancement (YE)
11. Metrology (M)
12. Environment, Safety, Health (ESH/S), and Sustainability

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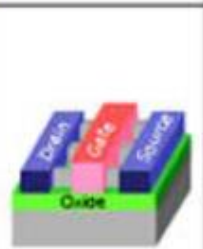
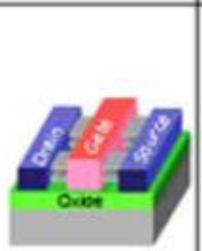
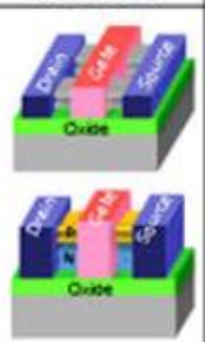
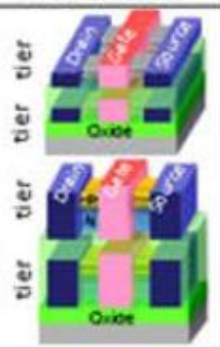
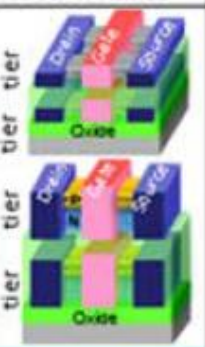
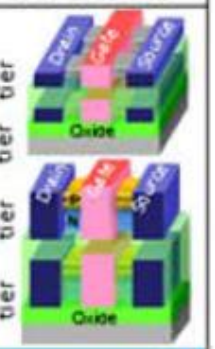
INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS™

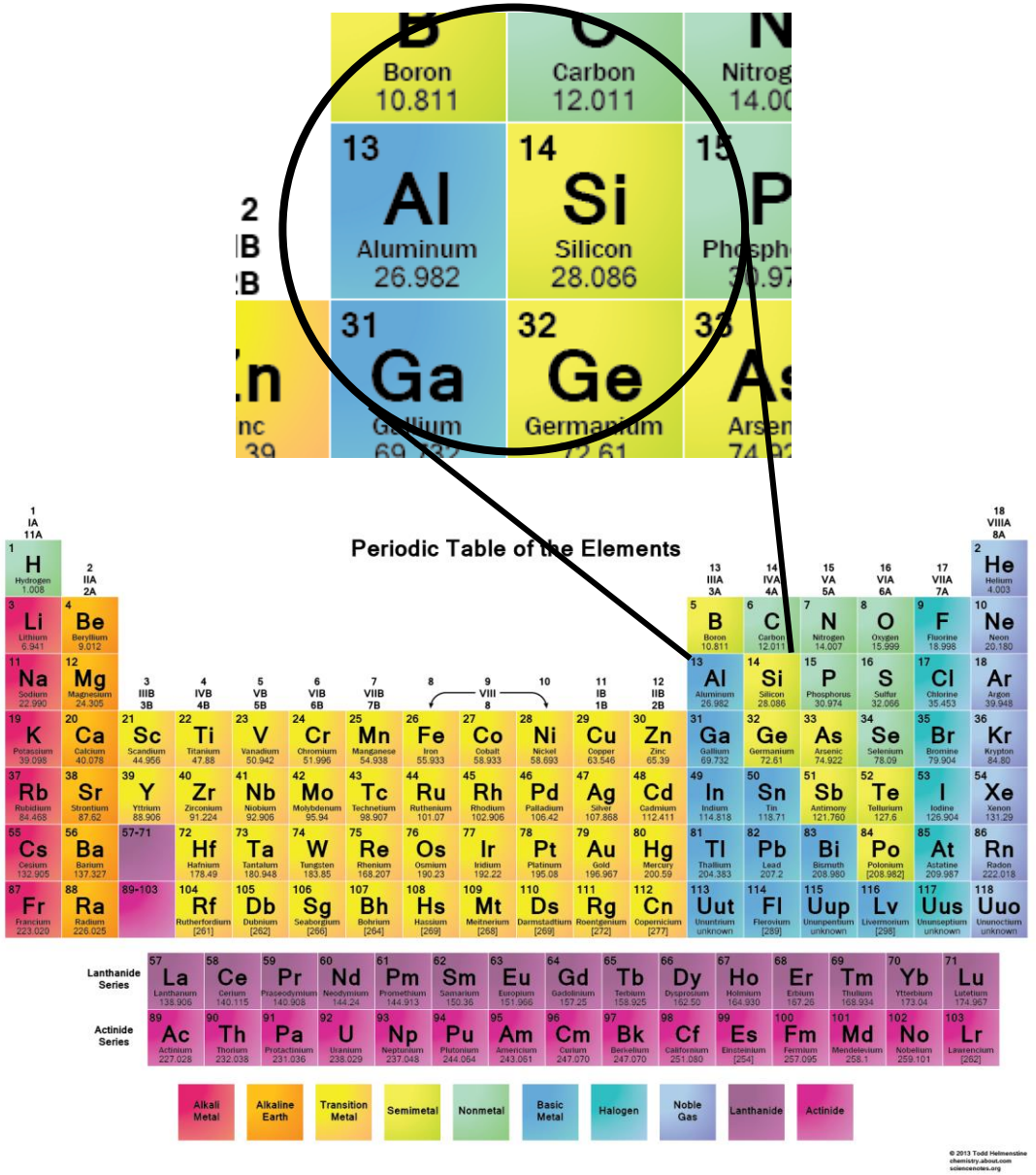
YEAR OF PRODUCTION	2022	2025	2028	2031	2034	2037
	G48M24	G45M20	G42M16	G40M16 T2	G38M16 T4	G38M16 T6
Logic industry "Node Range" Labeling	"3nm"	"2nm"	"1.5nm"	"1.0nm eq"	"0.7nm eq"	"0.5nm eq"
Fine-pitch 3D integration scheme	Stacking	Stacking	Stacking	3DVLSI	3DVLSI	3DVLSI
Logic device structure options	finFET LGAA	LGAA	LGAA CFET-SRAM	LGAA-3D CFET-SRAM	LGAA-3D CFET-SRAM	LGAA-3D CFET-SRAM
Platform device for logic	finFET	LGAA	LGAA CFET-SRAM	LGAA-3D CFET-SRAM-3D	LGAA-3D CFET-SRAM-3D	LGAA-3D CFET-SRAM-3D
						
LOGIC DEVICE GROUND RULES						
Mx pitch (nm)	32	24	20	16	16	16
M1 pitch (nm)	32	23	21	20	19	19
M0 pitch (nm)	24	20	16	16	16	16
Gate pitch (nm)	48	45	42	40	38	38
Lg: Gate Length - HP (nm)	16	14	12	12	12	12
Lg: Gate Length - HD (nm)	18	14	12	12	12	12
Channel overlap ratio - two-sided	0.20	0.20	0.20	0.20	0.20	0.20
Spacer width (nm)	6	6	5	5	4	4
Spacer k value	3.5	3.3	3.0	3.0	2.7	2.7
Contact CD (nm) - finFET, LGAA	20	19	20	18	18	18
Device architecture key ground rules						
Device lateral pitch (nm)	24	26	24	24	23	23
Device height (nm)	48	52	48	64	60	56
FinFET Fin width (nm)	5.0					
Footprint drive efficiency - finFET	4.21					
Lateral GAA vertical pitch (nm)		18.0	16.0	16.0	15.0	14.0
Lateral GAA (nanosheet) thickness (nm)		6.0	6.0	6.0	5.0	4.0
Number of vertically stacked nanosheets on one device		3	3	4	4	4
LGAA width (nm) - HP		30	30	20	15	15
LGAA width (nm) - HD		15	10	10	6	6
LGAA width (nm) - SRAM		7	6	6	6	6
Footprint drive efficiency - lateral GAA - HP		4.41	4.50	5.47	5.00	4.75
Device effective width (nm) - HP	101.0	216.0	216.0	208.0	160.0	152.0
Device effective width (nm) - HD	101.0	126.0	96.0	128.0	88.0	80.0
PN seperation width (nm)	45	40	20	15	15	10

2022IRDS_ES.pdf

Conductivity

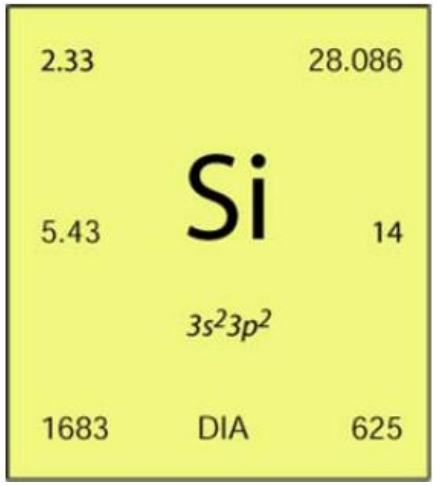
Al: $\sigma = 3.5 \times 10^{7}$ 1/Ω·m

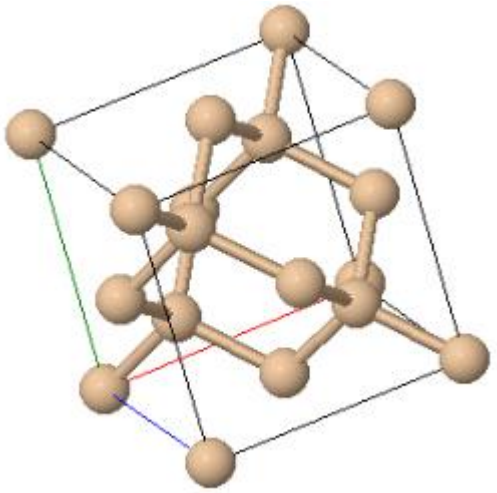
Si: $\sigma = 4.3 \times 10^{-4}$ 1/Ω·m



Silicon

- important semiconducting material
- 2nd most common element on earths crust (rocks, sand, glass, concrete)
- often doped with other elements
- oxide SiO_2 is a good insulator



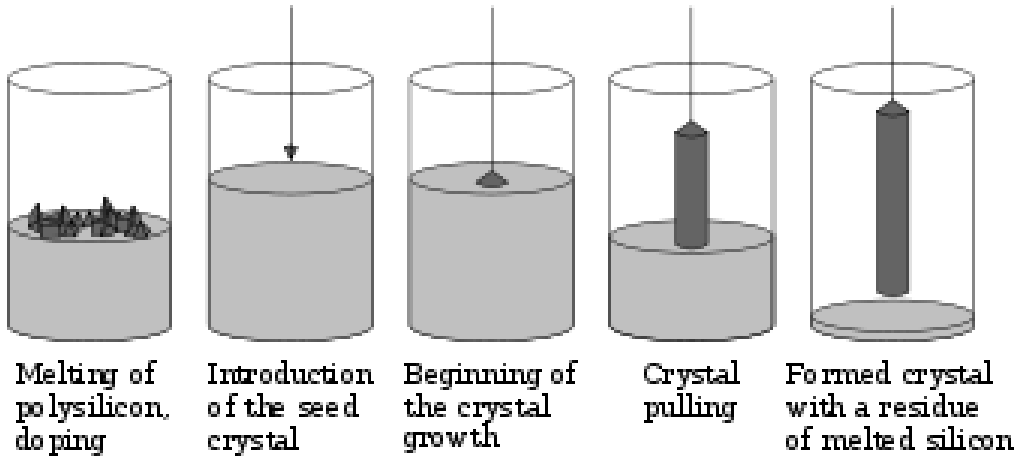


silicon crystal = diamond crystal structure

Silicon

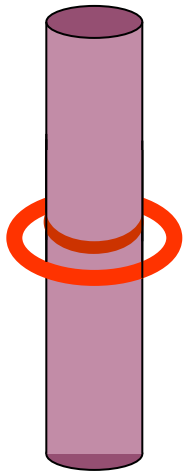
Large (2 m) single crystals are grown

Czochralski process

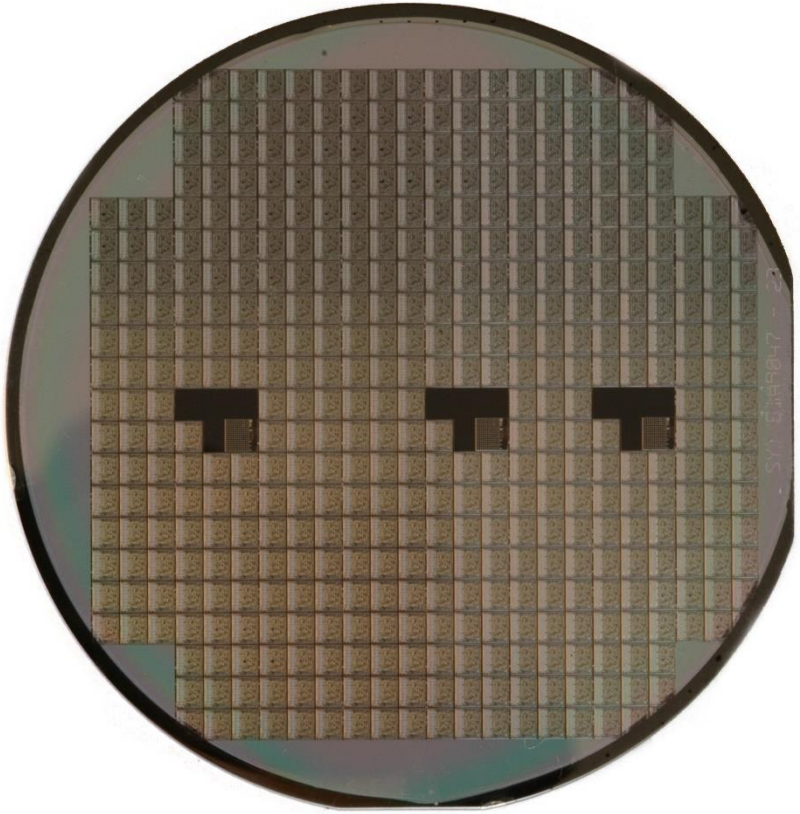


http://en.wikipedia.org/wiki/Czochralski_process

Float zone

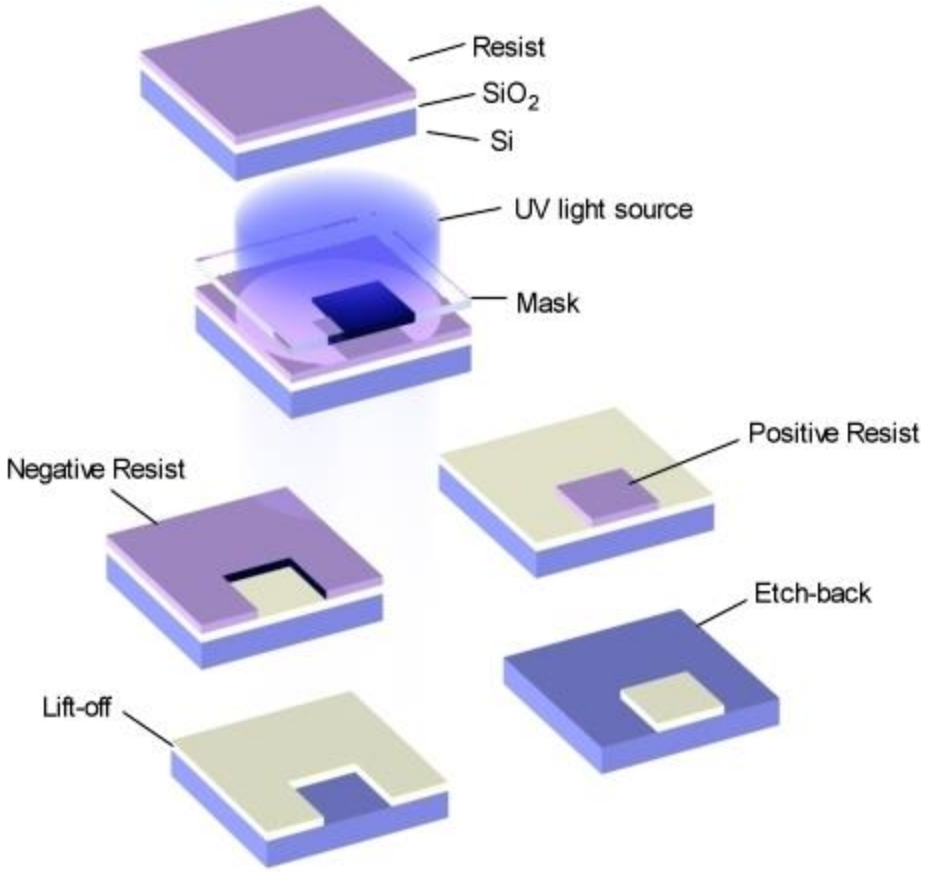


Silicon wafers



50 mm - 0.5 mm thick

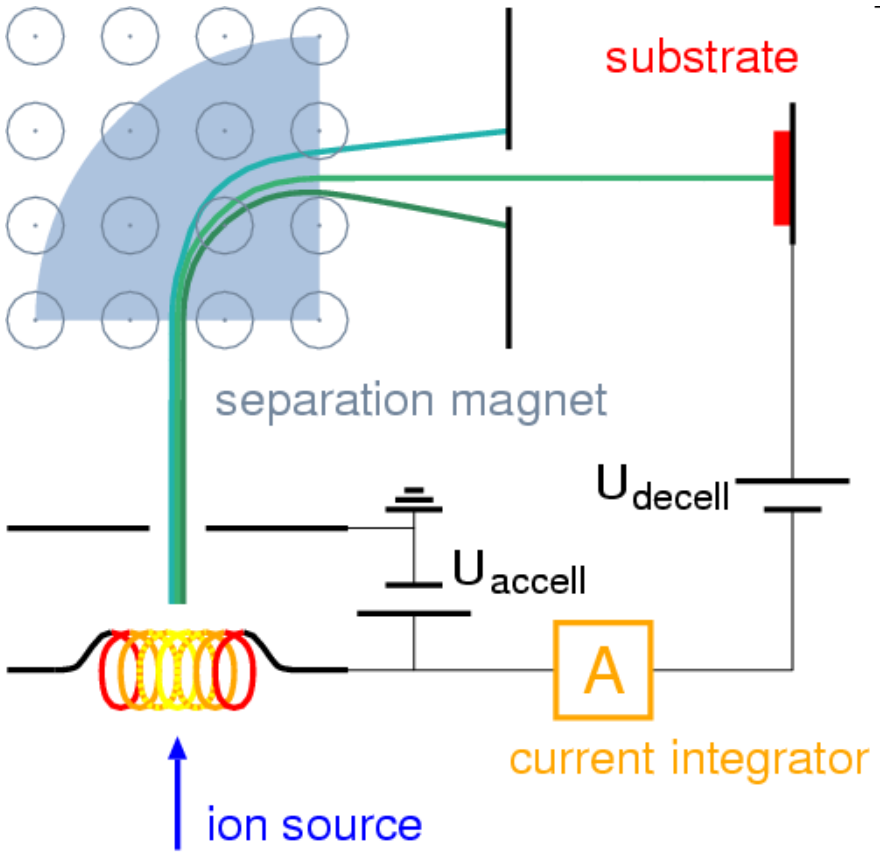
Photolithography



http://britneyspears.ac/physics/fabrication/photolithography.htm

http://cleanroom.byu.edu/lithography.parts/Lithography.html

Ion implantation



Implant at 7º to avoid channeling

On the chip

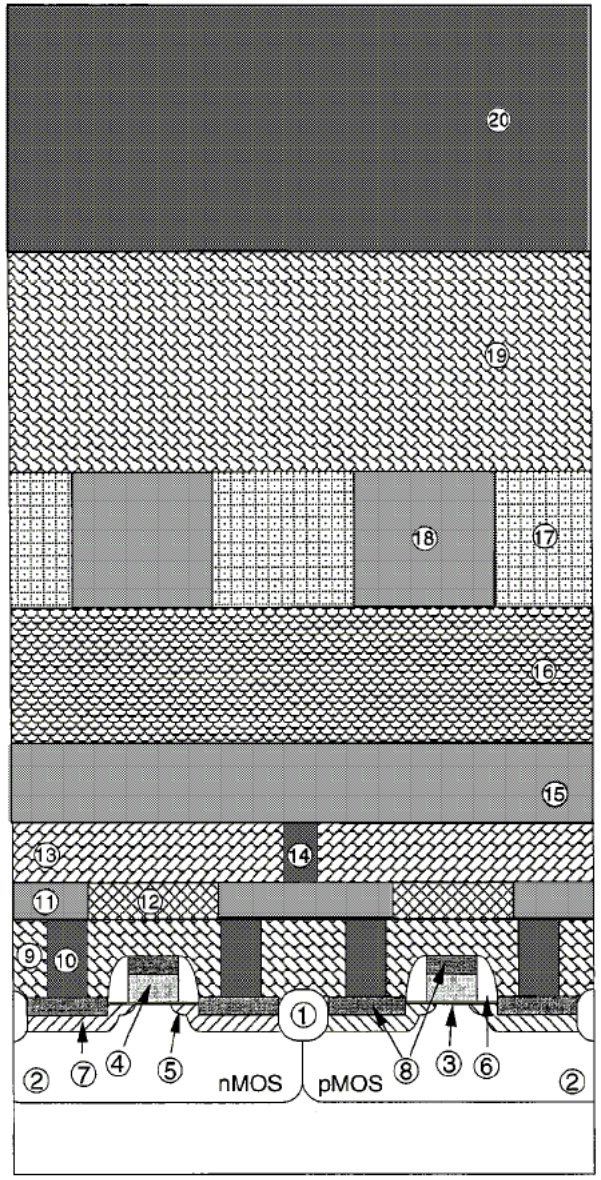
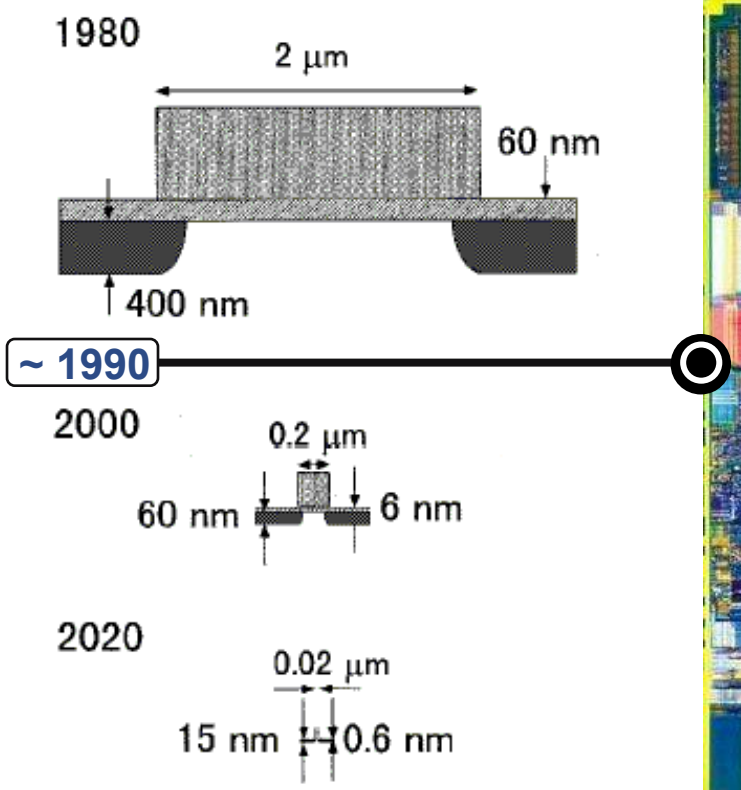
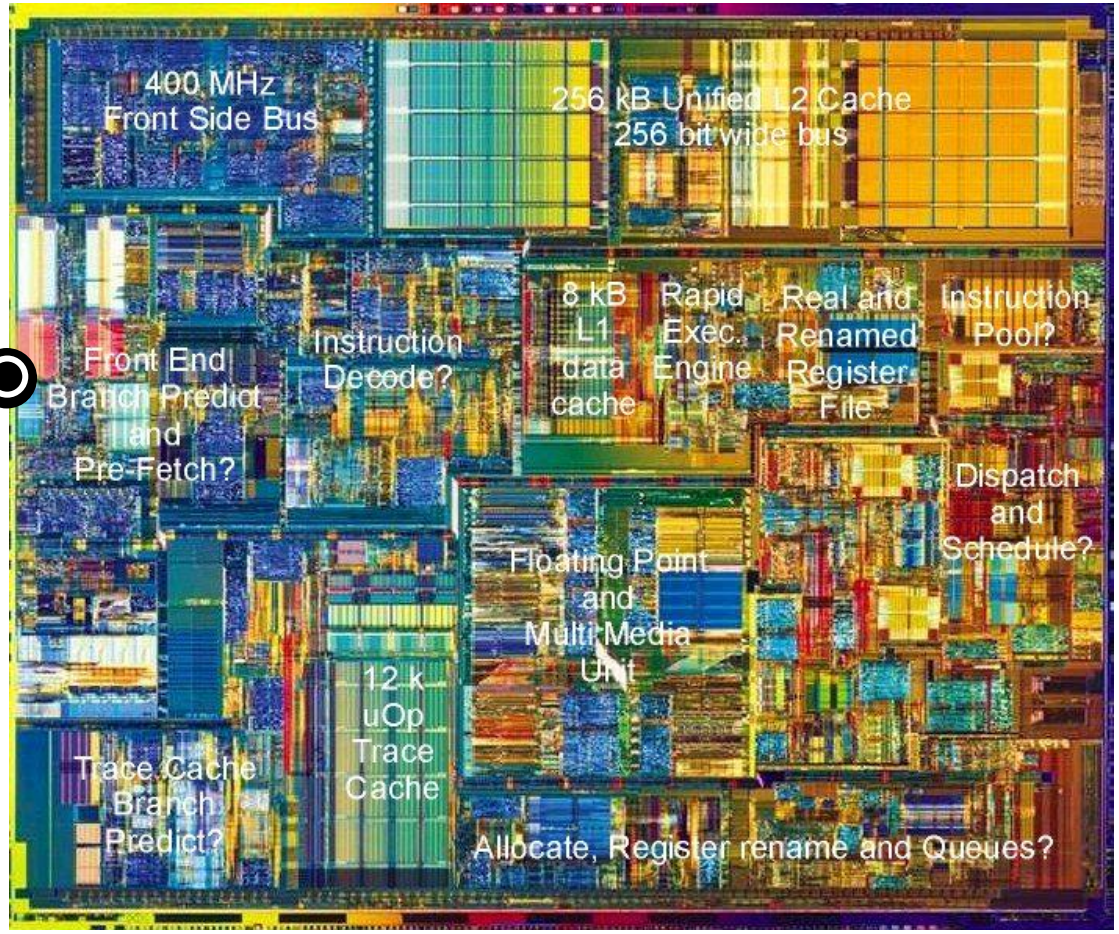


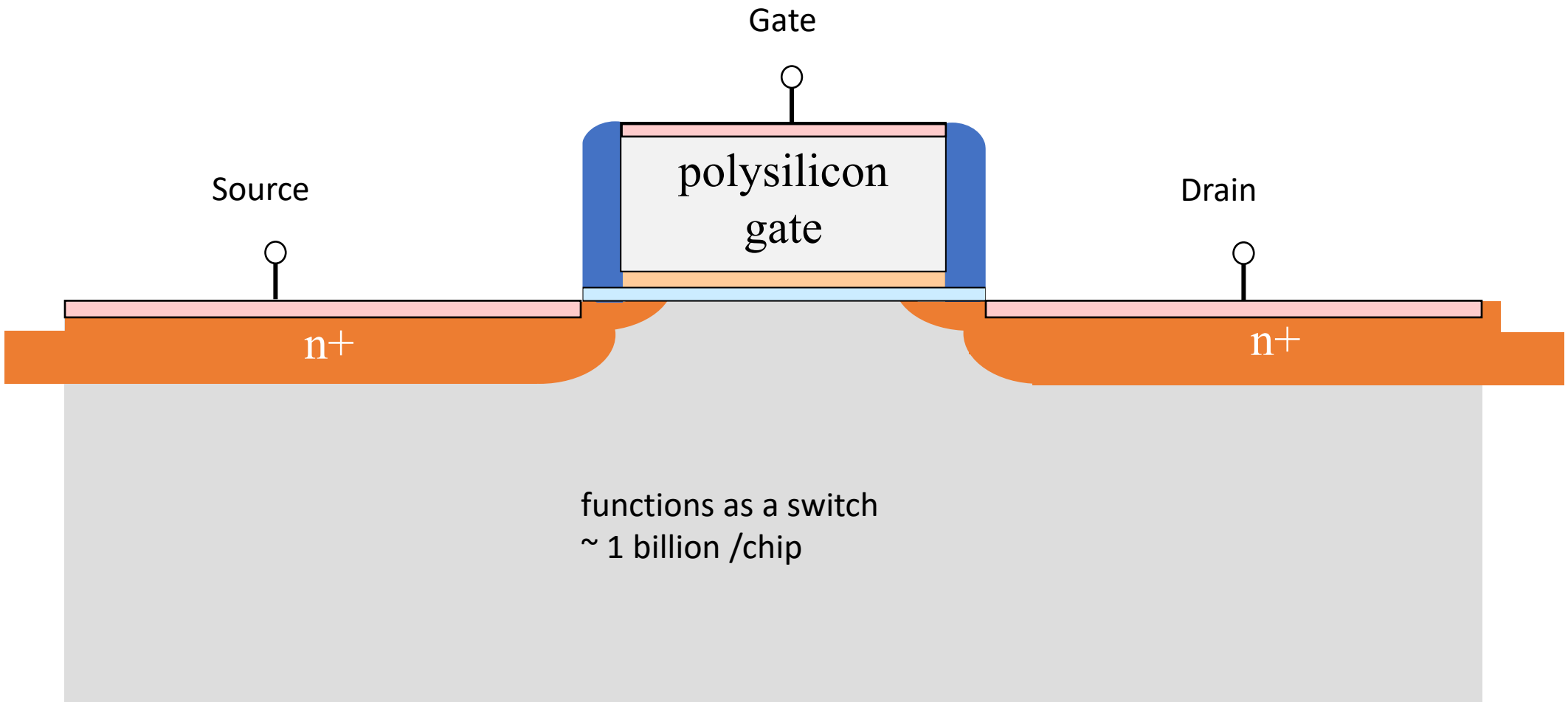
Fig. 2 Schematic cross section of present CMOS FETs with multilayered wiring.





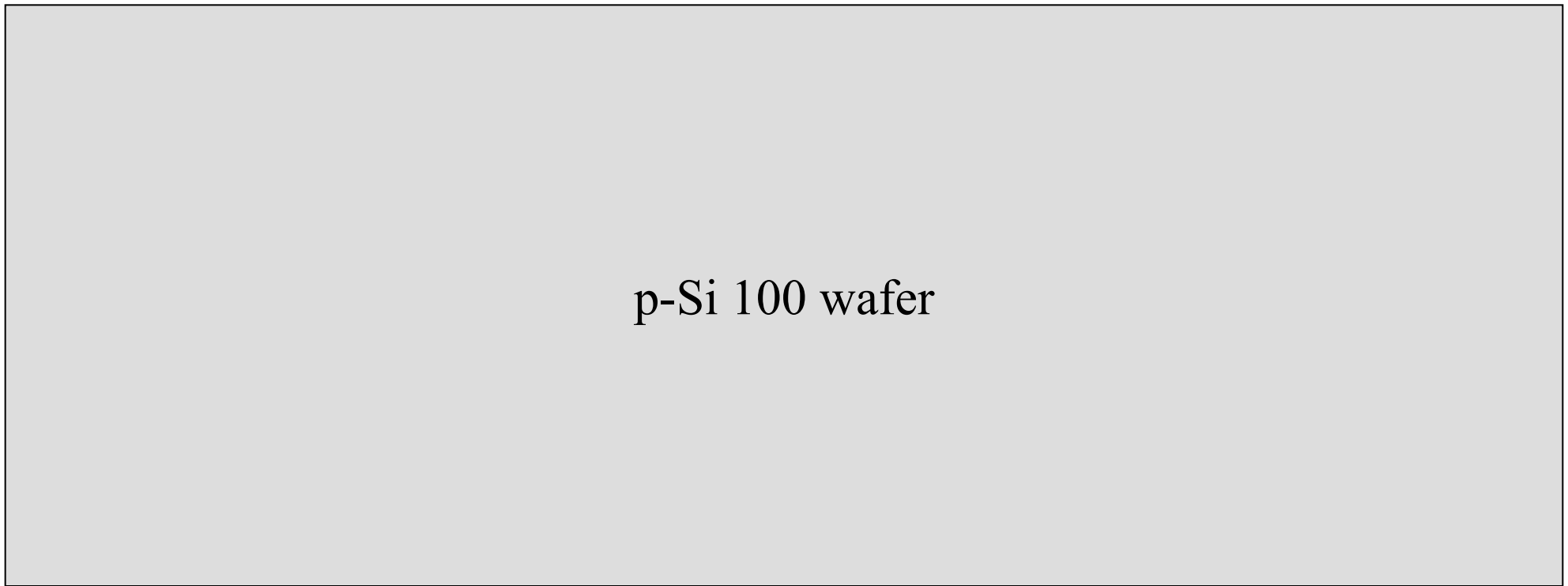
MOSFET

Metal Oxide Semiconductor Field Effect Transistor

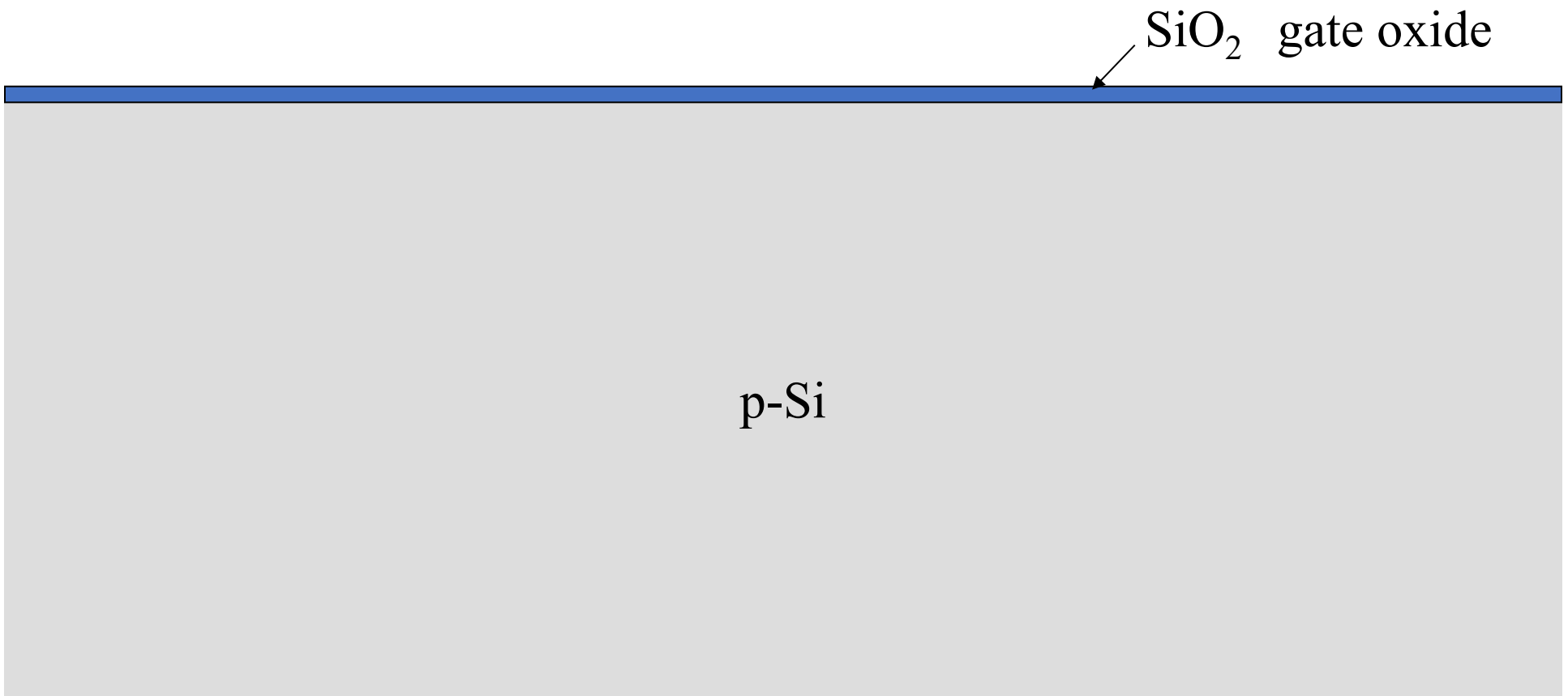


functions as a switch
~ 1 billion /chip

Self-aligned fabrication

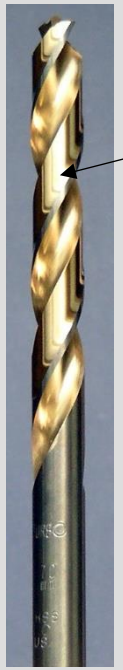


Dry oxidation



photoresist

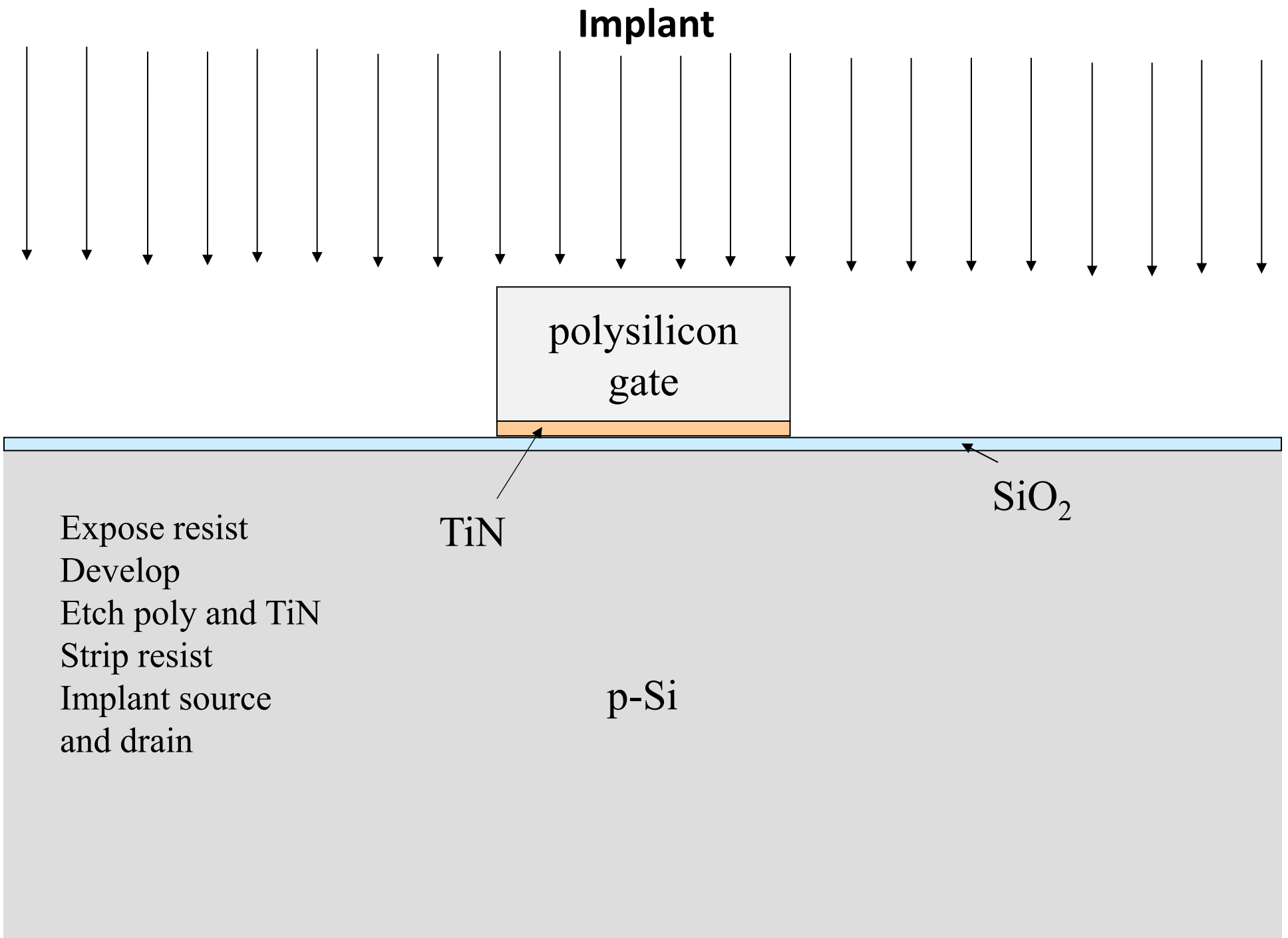
polysilicon CVD: SiH_4 @ 580 to 650 °C



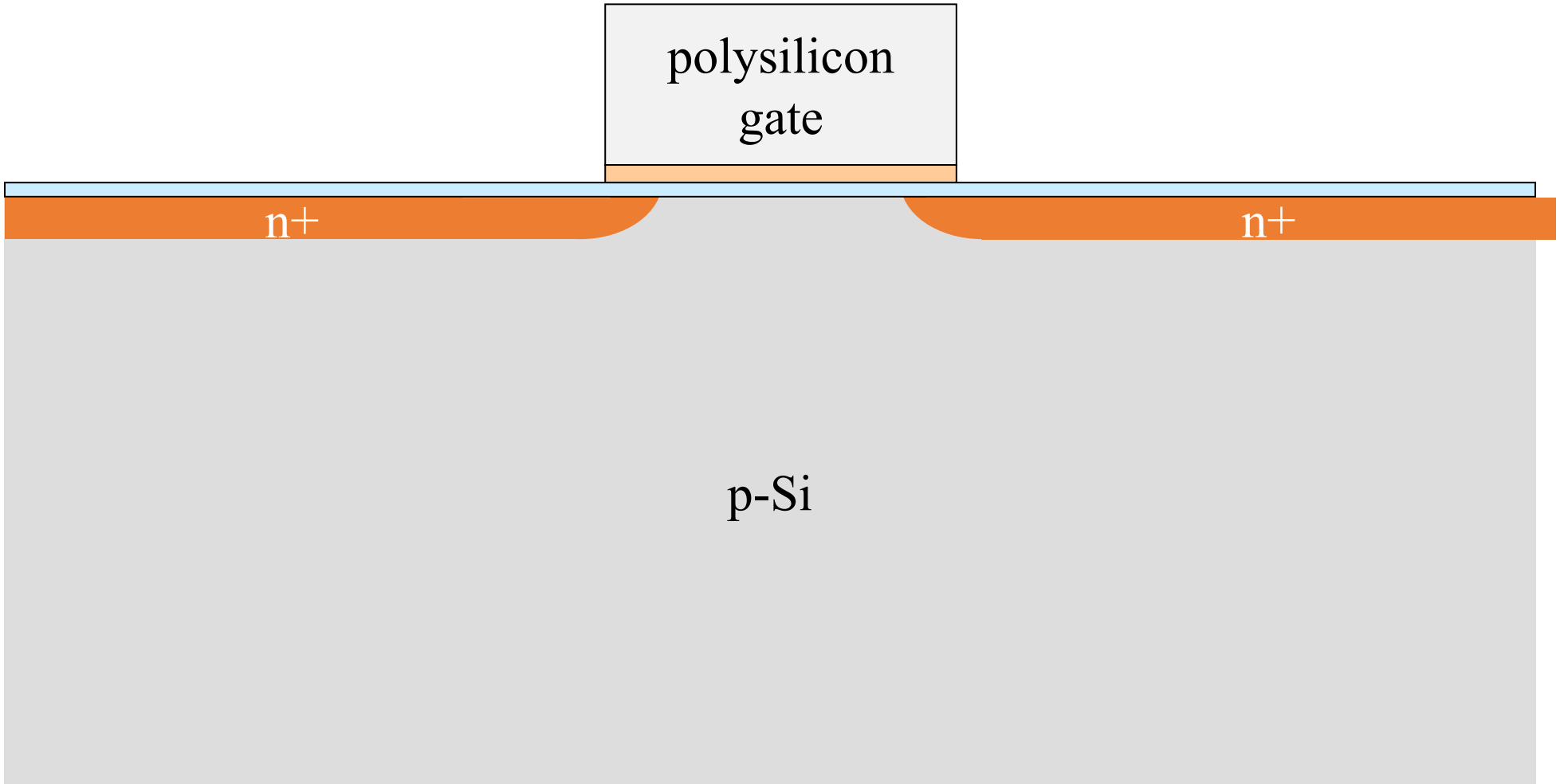
TiN (CVD)
30–70 μΩ·cm Conductive diffusion barrier

SiO_2

p-Si

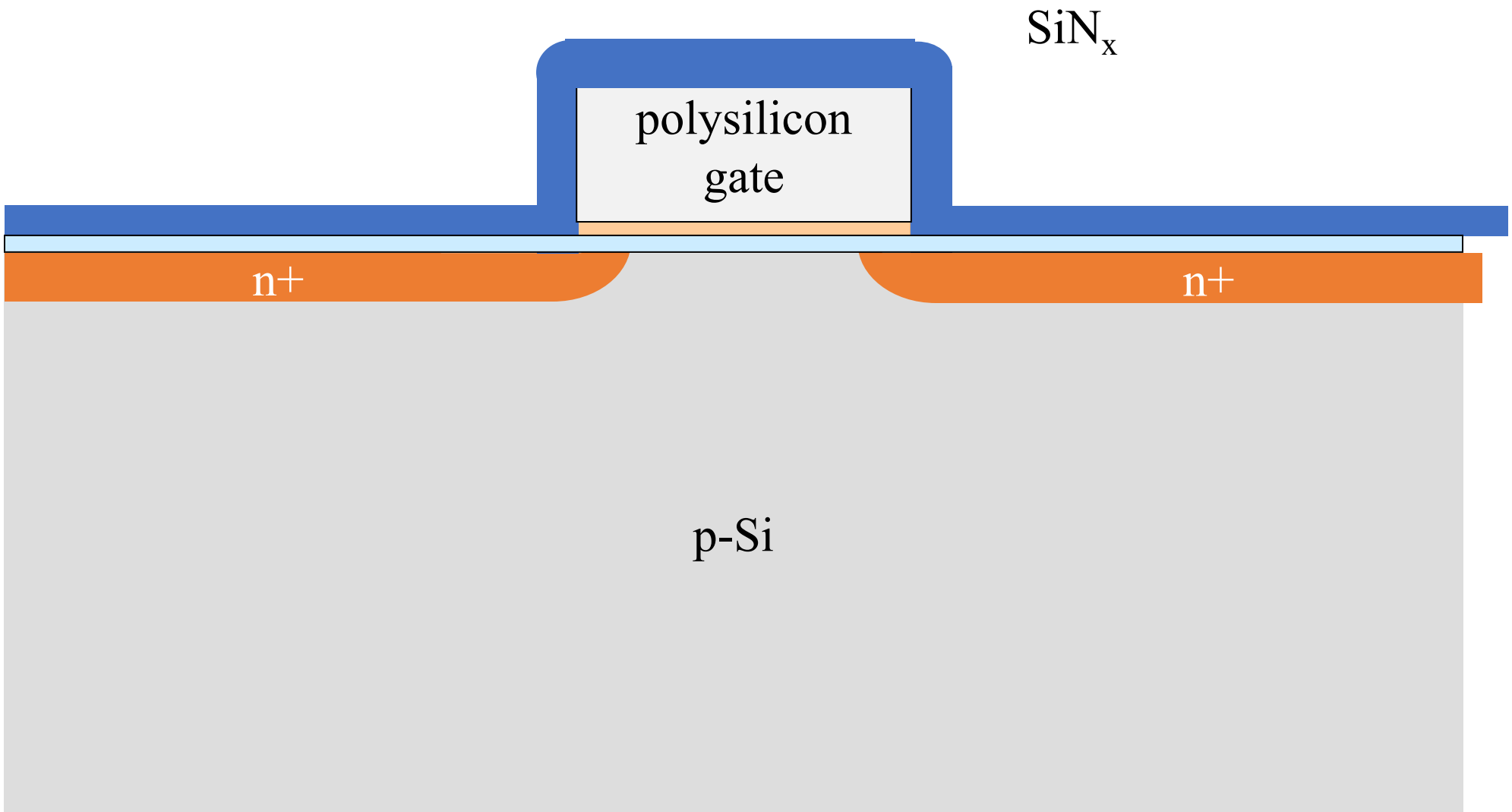

Implant
polysilicon
gate
TiN
SiO_2
Expose resist
Develop
Etch poly and TiN
Strip resist
Implant source
and drain
p-Si

Self-aligned fabrication



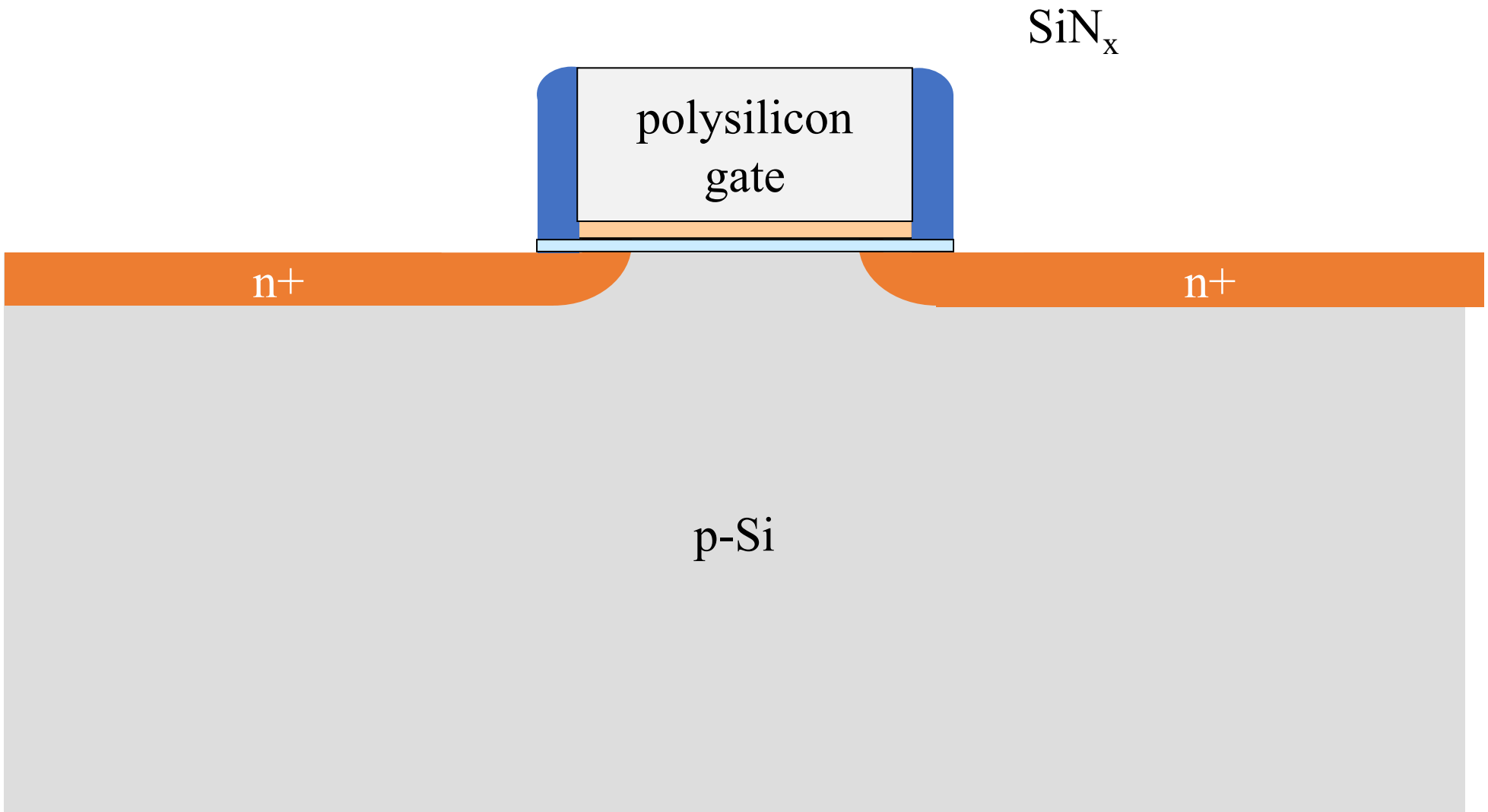
Spacer

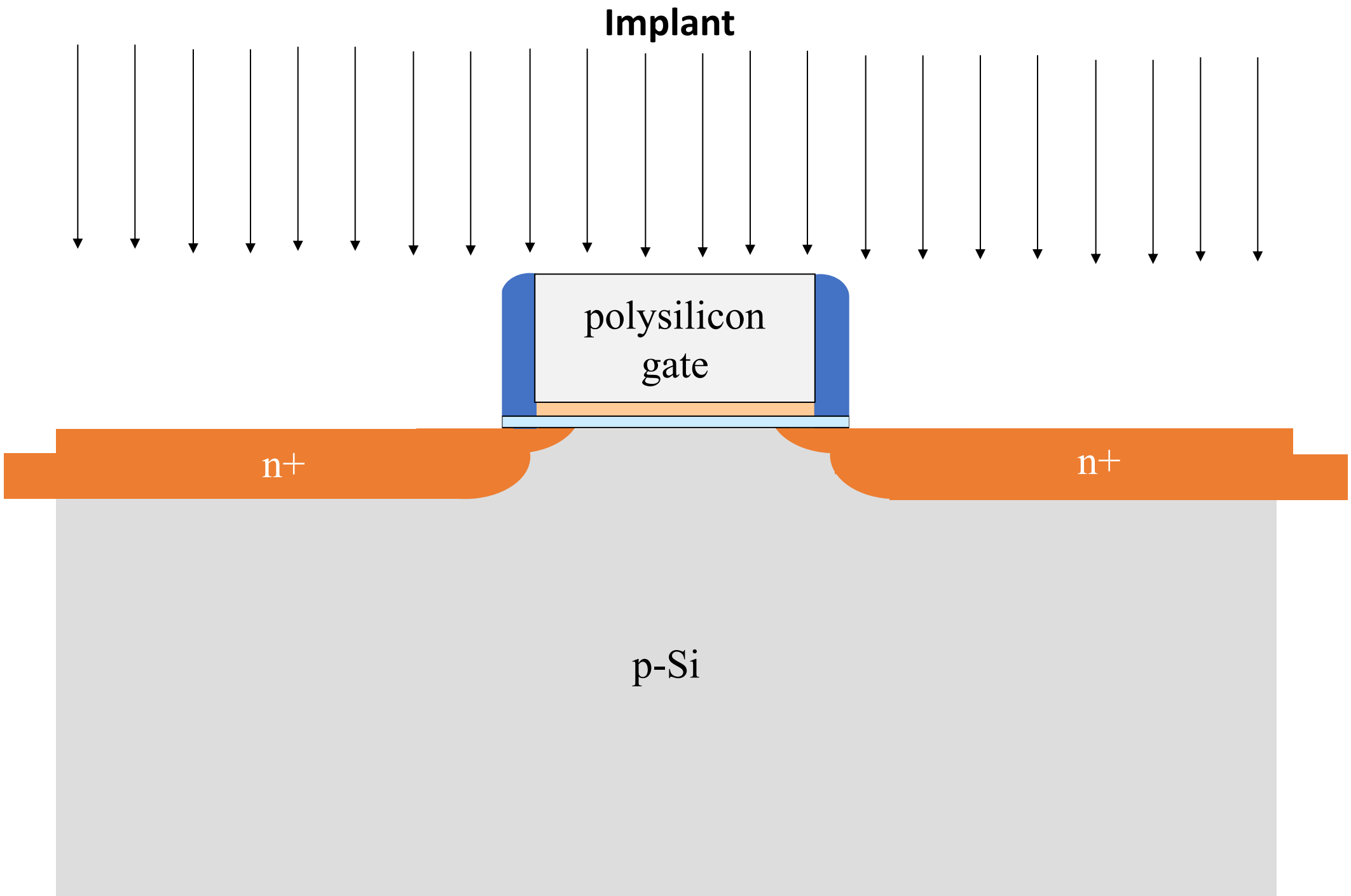
PECVD SiN_x



Spacer

Etch back to leave
only sidewalls




Implant
polysilicon
gate
n+
n+
p-Si

Salicide (Self-aligned silicide)

Transition metal (Ti, Co,W) is deposited (CVD). During a high temperature step is reacts to a silicide ($TiSi_2$). Not silicide is formed on nitride or oxide.