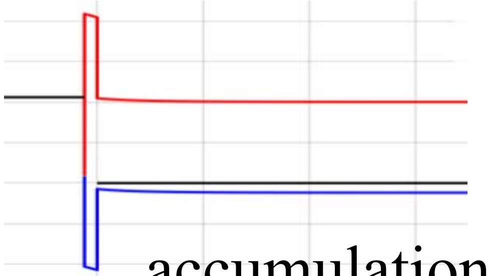
11. MOSFETs

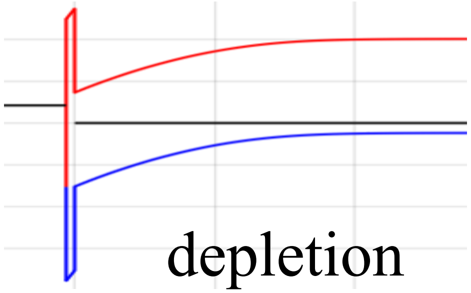
Dec. 12, 2018

Gradual channel approximation

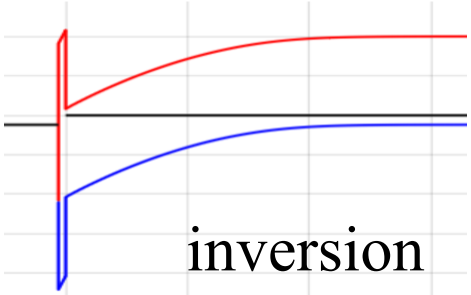


accumulation

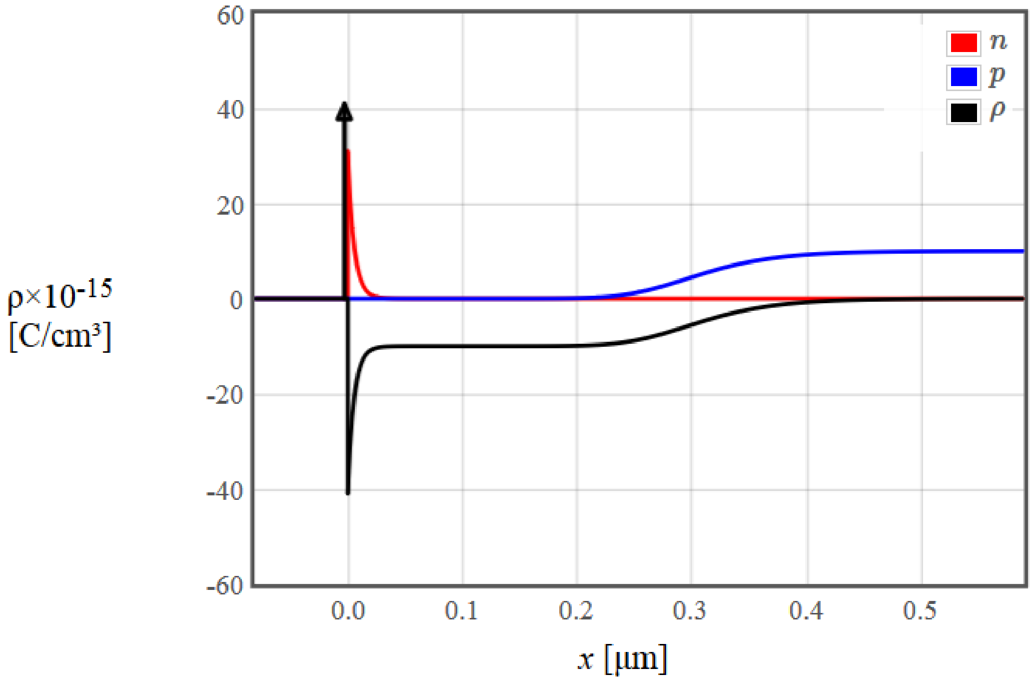
$$Q_{\text{mobile}} = \begin{cases} 0, & \text{for } V_G - V_B < V_T \\ -C_{\text{ox}}(V_G - V_B - V_T) & \text{for } V_G - V_B > V_T \end{cases}$$



depletion



inversion



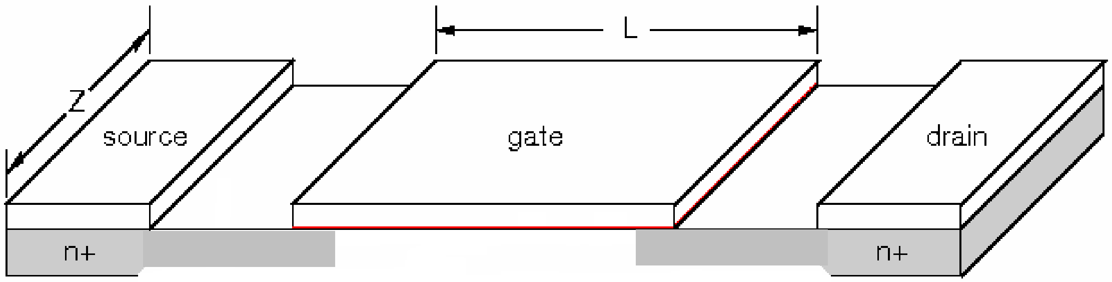
http://lampx.tugraz.at/~hadley/psd/L10/gradualchannelapprox.php

Gradual channel approximation

Ohm's law →

$$j = -nev_d = ne\mu_n E_y$$

$$I = Ztj = Ztne\mu_n E_y = Ze\mu_n n_s E_y$$



$n_s = nt$ is the sheet charge at the interface.

$$n_s(y) = -\frac{Q}{e} = \frac{C_{ox}\left(V_G - V_{ch}(y) - V_T\right)}{e}$$

Gradual channel approximation

$$n_s(y) = -\frac{Q(y)}{e} = \frac{C_{ox}(V_G - V_{ch}(y) - V_T)}{e}$$

$$I = Ztj = Ztnev_d = Zen_s\mu_n E_y$$

$$I_D = -Z\mu_n C_{ox}(V_G - V_{ch}(y) - V_T)\frac{dV_{ch}}{dy}$$

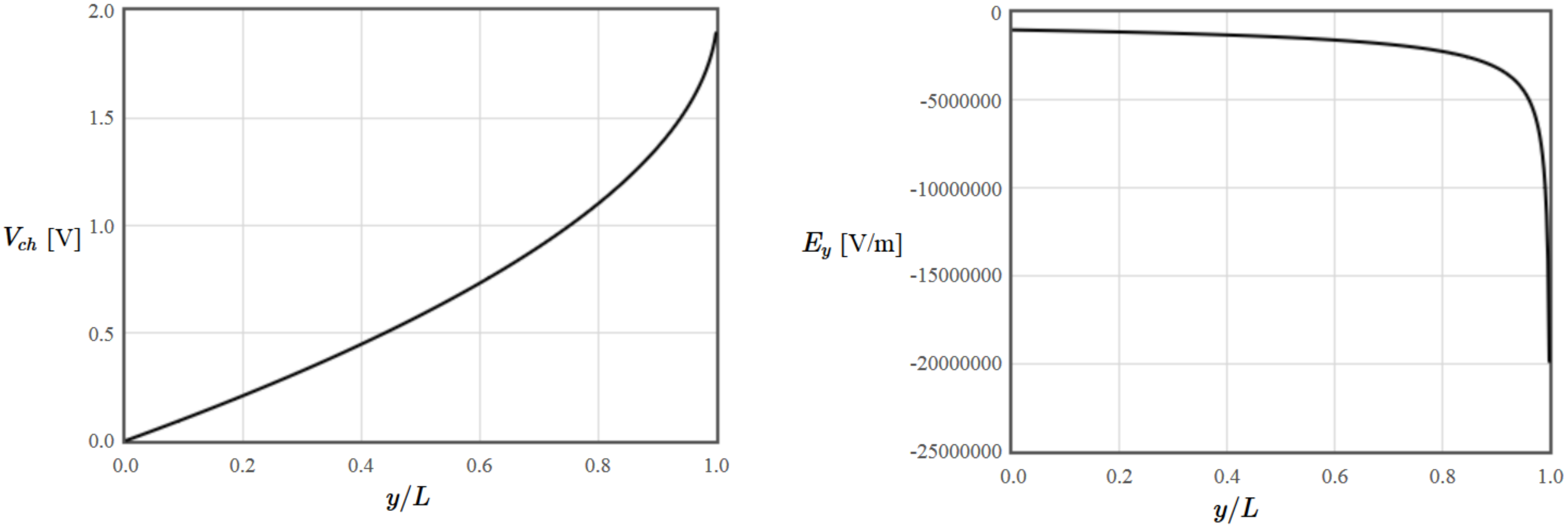
differential equation for V_{ch}

http://lampx.tugraz.at/~hadley/psd/L10/gradualchannelapprox.php

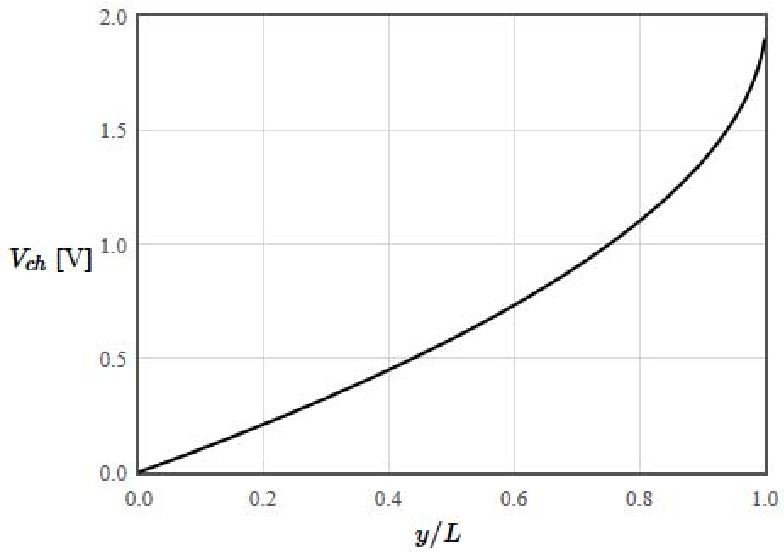
Gradual channel approximation

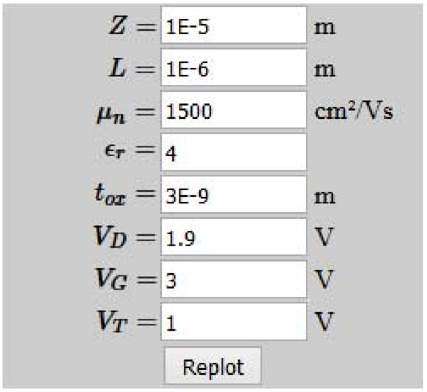
$$V_{ch}(y) = V_G - V_T - \sqrt{(V_G - V_T)^2 - \frac{2I_D y}{Z\mu_n C_{ox}}}$$

$$E_y = -\frac{dV_{ch}}{dy} = -\frac{I_D}{Z\mu_n C_{ox}\sqrt{(V_G - V_T)^2 - \frac{2I_D y}{Z\mu_n C_{ox}}}}$$



MOSFET Gradual Channel Approximation





$Z =$ 1E-5 m

$L =$ 1E-6 m

$\mu_n =$ 1500 cm²/Vs

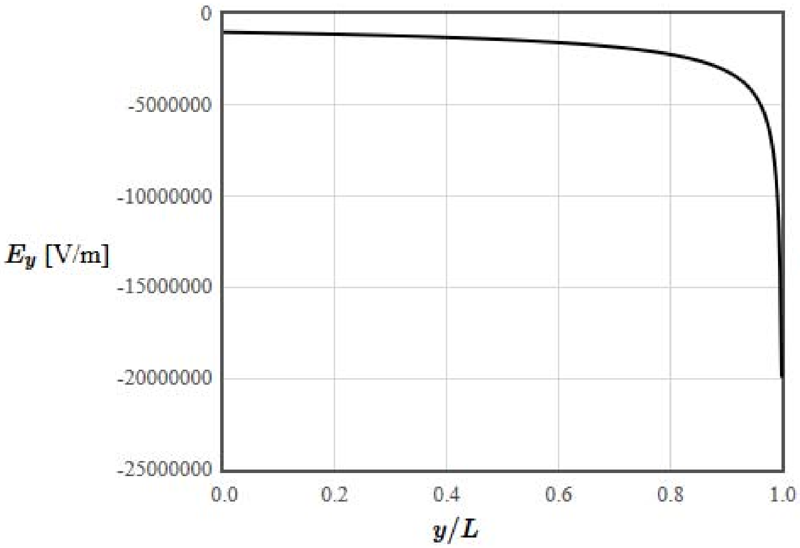
$\epsilon_r =$ 4

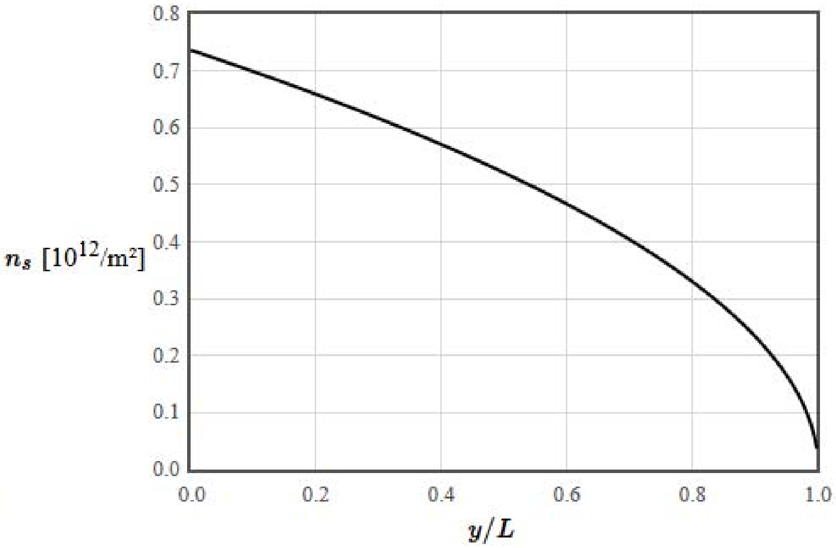
$t_{ox} =$ 3E-9 m

$V_D =$ 1.9 V

$V_G =$ 3 V

$V_T =$ 1 V





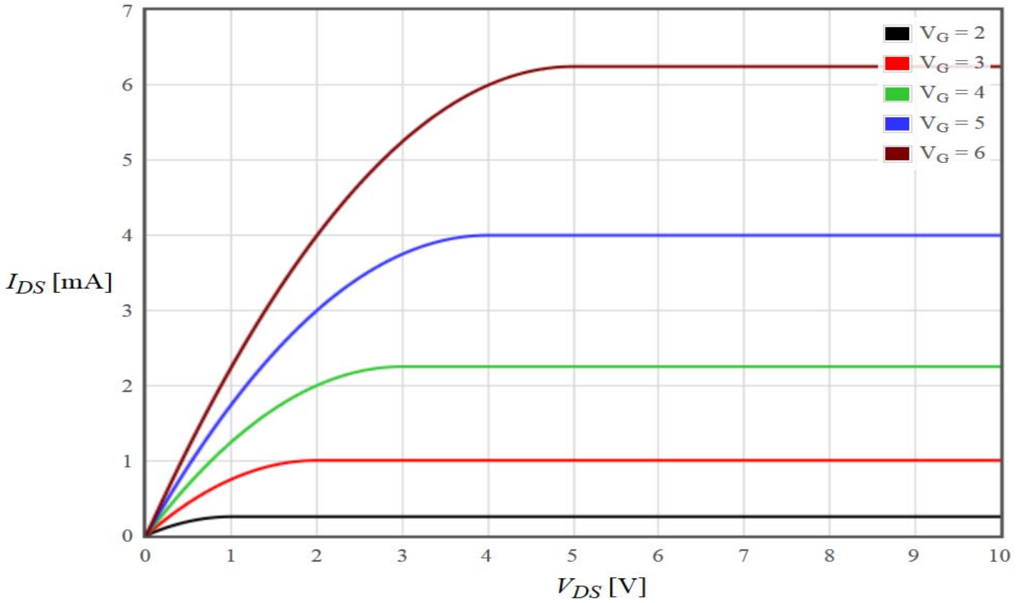
http://lampx.tugraz.at/~hadley/psd/L10/gradualchannelapprox.php

Gradual channel approximation

$$\int_0^L I_D\,\mathrm{d}y = \int_0^{V_D} Z\mu_n C_{ox}(V_G - V_B(y) - V_T)\,\mathrm{d}V$$

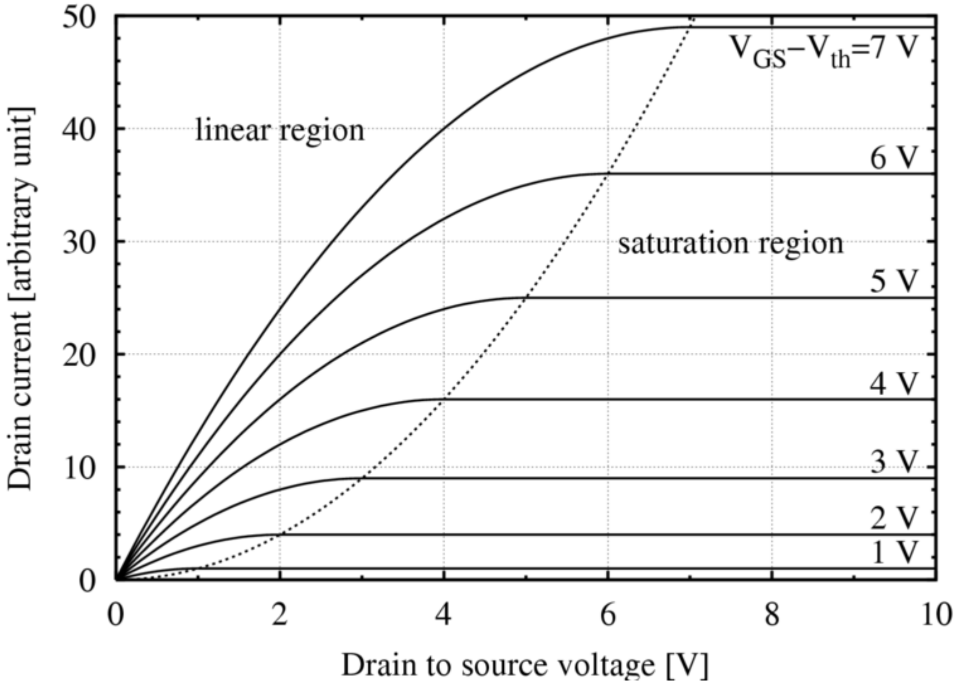
$$\boxed{I_D = \frac{Z}{L}\mu_n C_{ox}\left[(V_G - V_T)V_D - \frac{V_D^2}{2}\right]}$$

Valid in the linear regime (until pinch-off occurs at the drain).



MOSFET-saturation voltage

$$I = \frac{Z}{L}\mu_n C_{ox}\left[\left(V_G - V_T\right)V_D - \frac{V_D^2}{2}\right]$$



At pinch-off, $dI_{ds}/dV_{ds} = 0$

$$\frac{dI}{dV_D} = \frac{Z}{L}\mu_n C_{ox}\left[\left(V_G - V_T\right) - V_D\right] = 0$$

$$V_{sat} = \left(V_G - V_T\right)$$

A MOSFET in saturation is a voltage controlled current source.

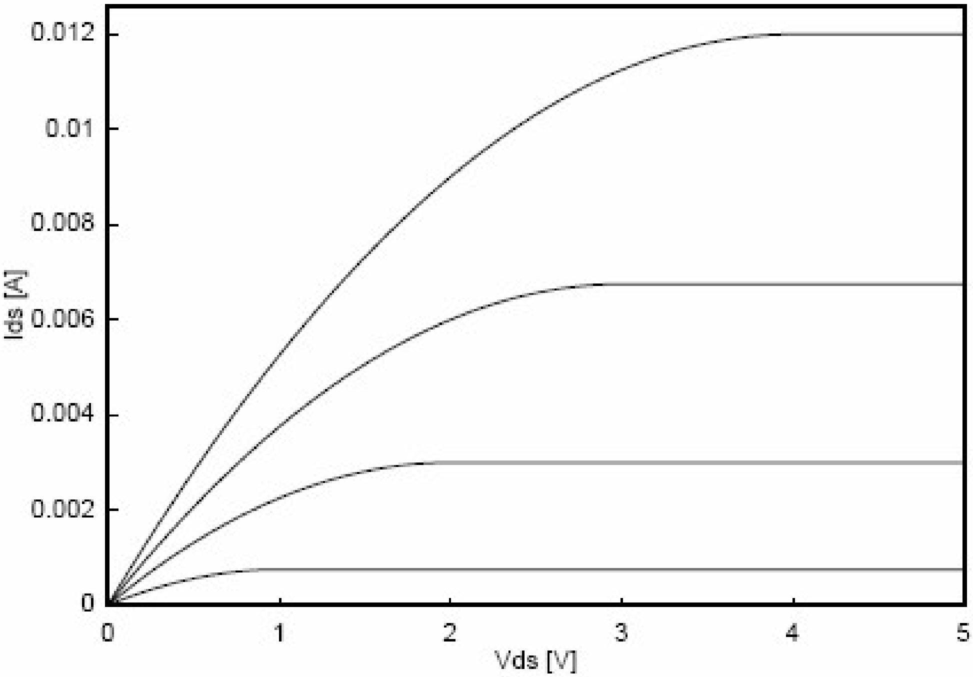
MOSFET - saturation current

Use the saturation voltage at pinch-off to determine the saturation current

$$V_{sat} = \left(V_G - V_T\right)$$

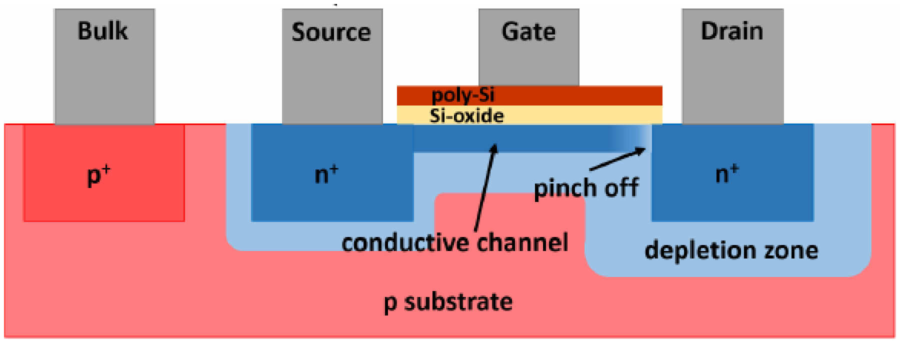
$$I = \frac{Z}{L}\mu_n C_{ox}\left[\left(V_G - V_T\right)V_D - \frac{V_D^2}{2}\right]$$

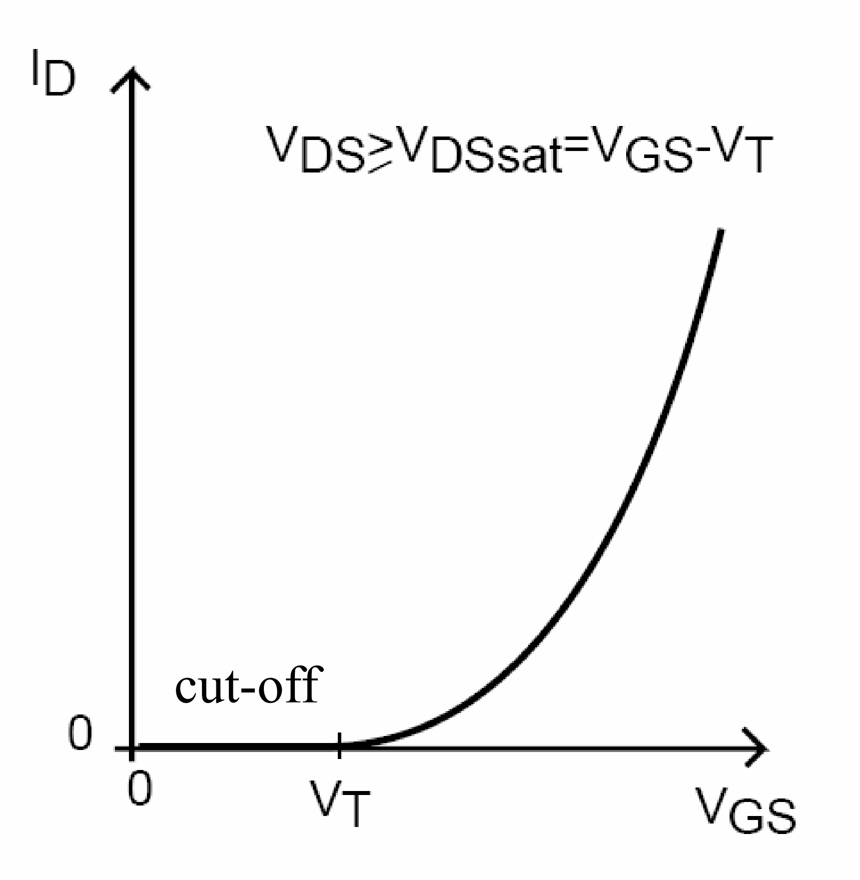
$$I_{sat} = \frac{Z}{2L}\mu_n C_{ox}\left(V_G - V_T\right)^2$$

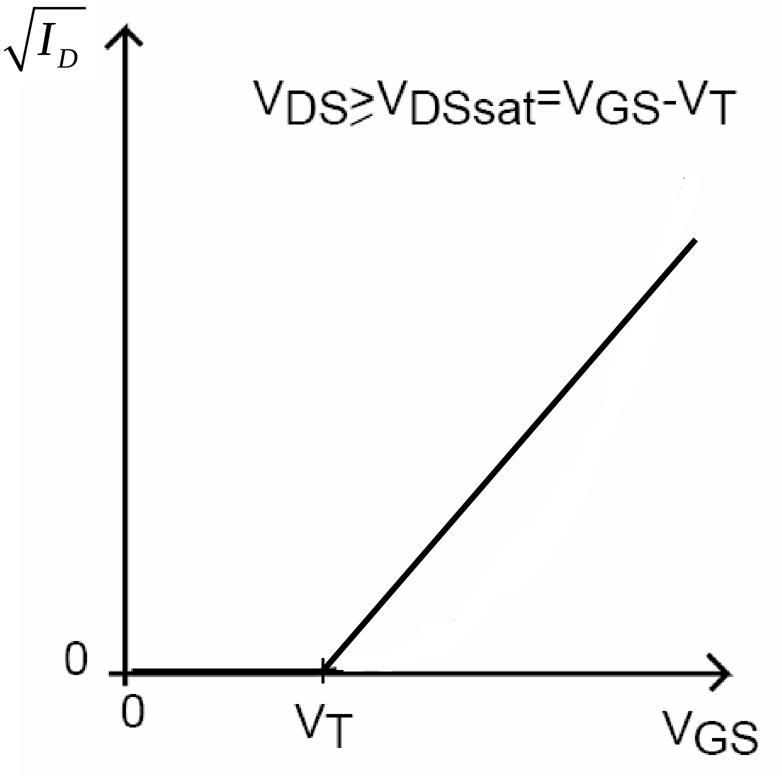


MOSFET (saturation regime)

$$I_{sat} = \frac{Z}{2L}\mu_n C_{ox}\left(V_{GS} - V_T\right)^2$$







MOSFET (linear regime)

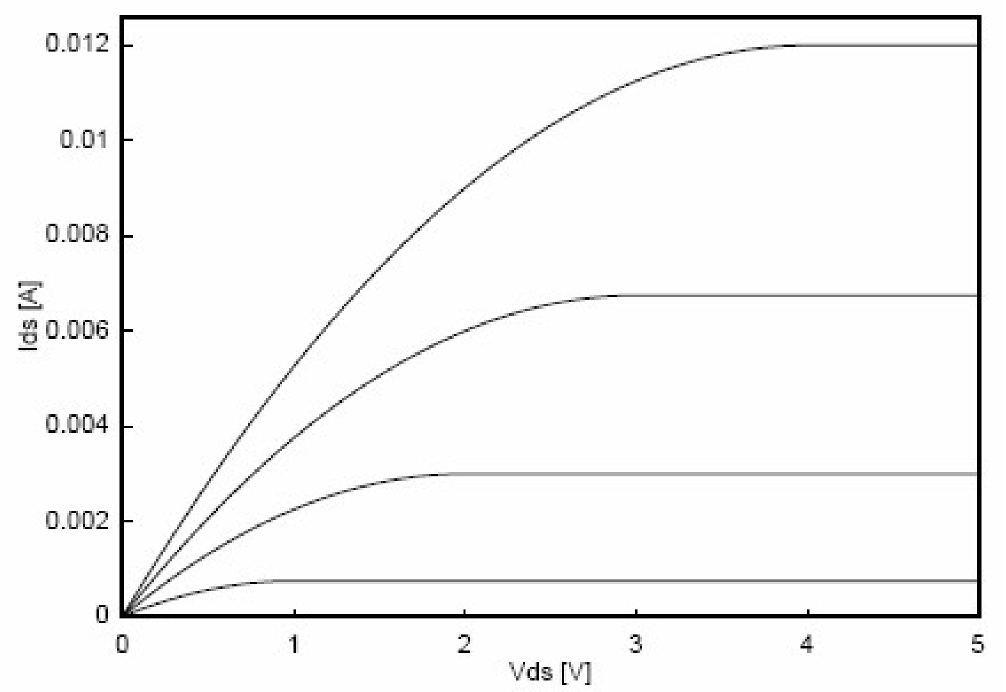
Channel conductance in the linear regime. For small V_D

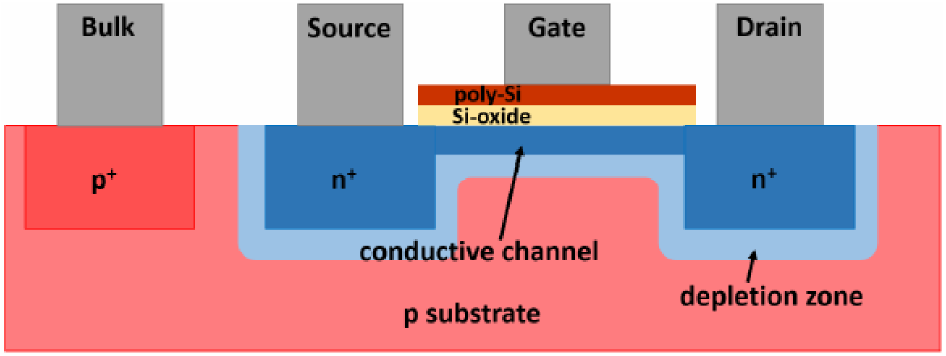
$$I \approx \frac{Z}{L}\mu_n C_{ox}\left[(V_G - V_T)V_D\right]$$

$$g_D = \frac{dI_D}{dV_D} = \frac{Z}{L}\mu_n C_{ox}(V_G - V_T)$$

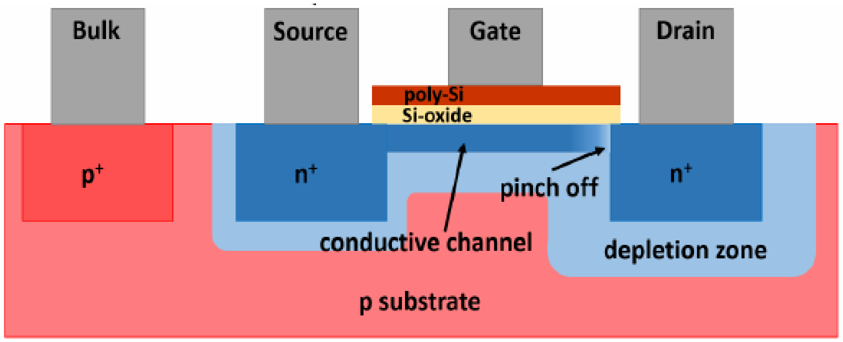
Transconductance

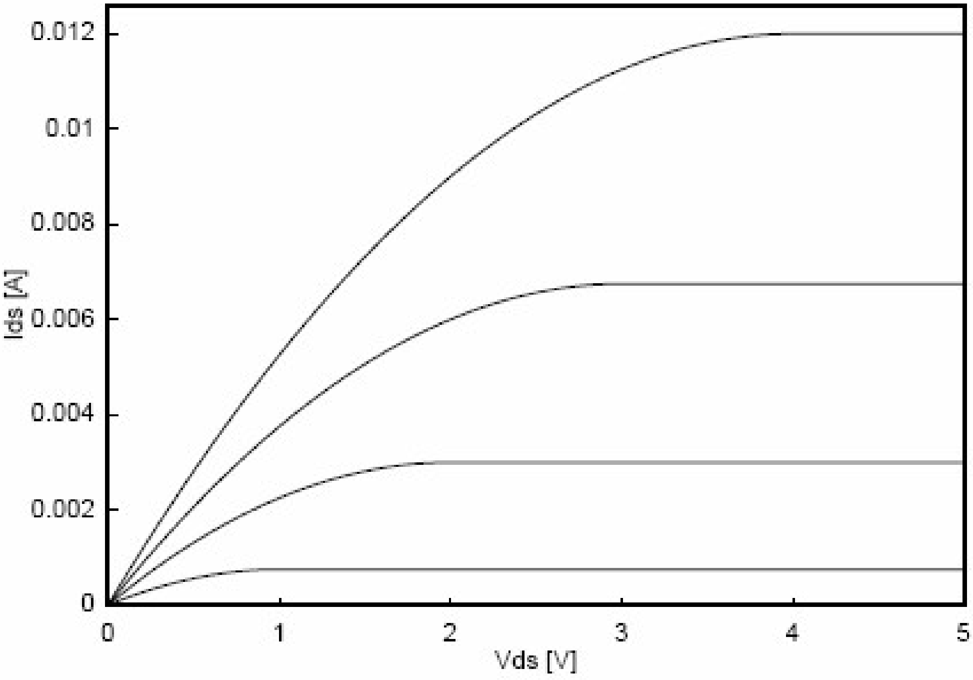
$$g_m = \frac{dI_D}{dV_G} = \frac{Z}{L}\mu_n C_{ox} V_D$$





MOSFET (saturation regime)





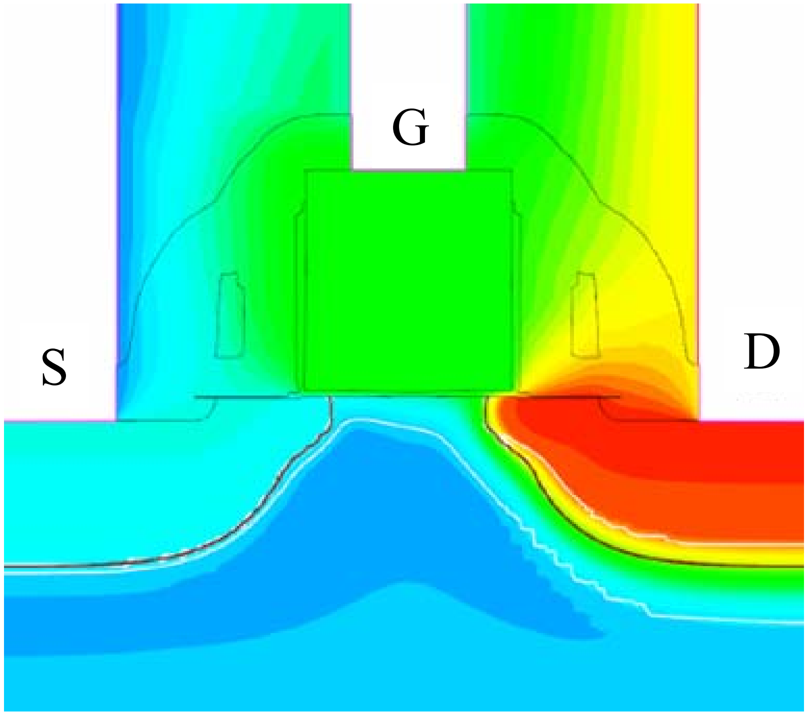
$$I_{sat} = \frac{Z}{2L}\mu_n C_{ox}\left(V_G - V_T\right)^2$$

Transconductance

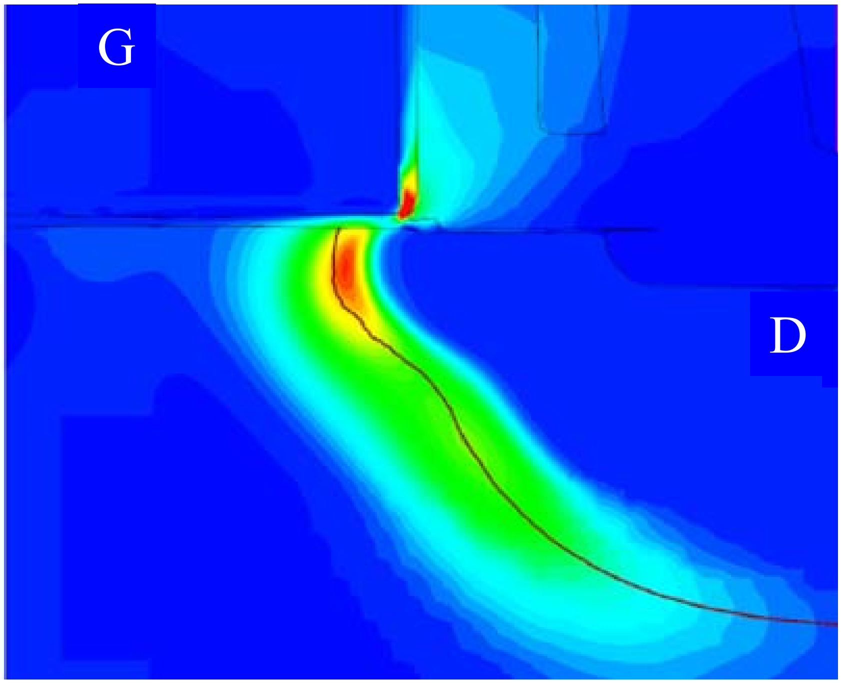
$$g_m = \frac{dI_D}{dV_G} = \frac{Z}{L}\mu_n C_{ox}\left(V_G - V_T\right)$$

A MOSFET in the saturation regime acts like a voltage controlled current source.

Saturation



Potential

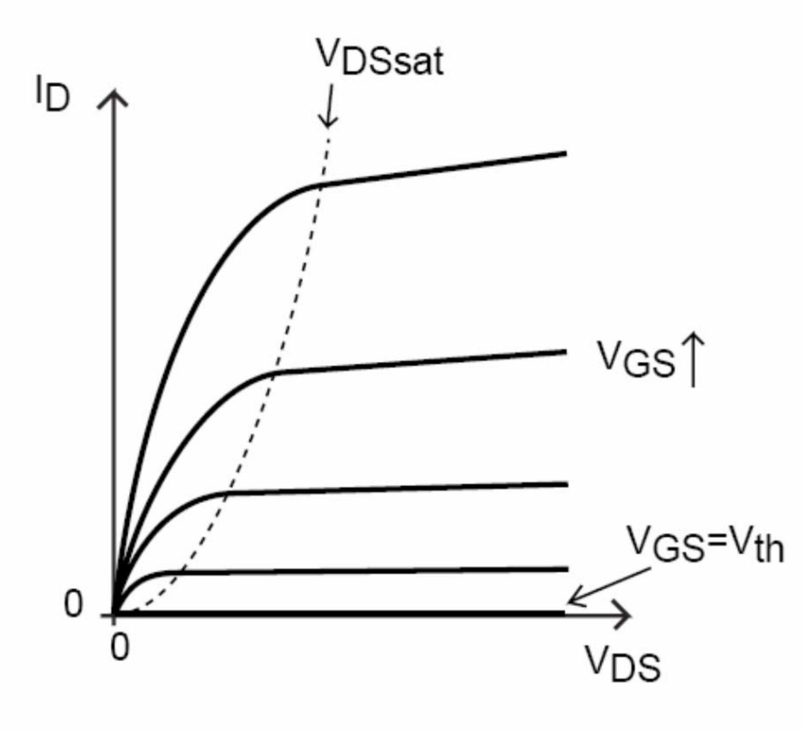


Electric field strength

Alexander Schiffmann, Master Thesis (2016)

MOSFET (saturation regime)

$$I_{sat} = \frac{Z}{2L}\mu_n C_{ox}\left(V_G - V_T\right)^2\left(1-\lambda\left(V_D - V_{sat}\right)\right)$$



Experimentally: channel length modulation $\lambda \propto \frac{1}{L}$

High frequencies

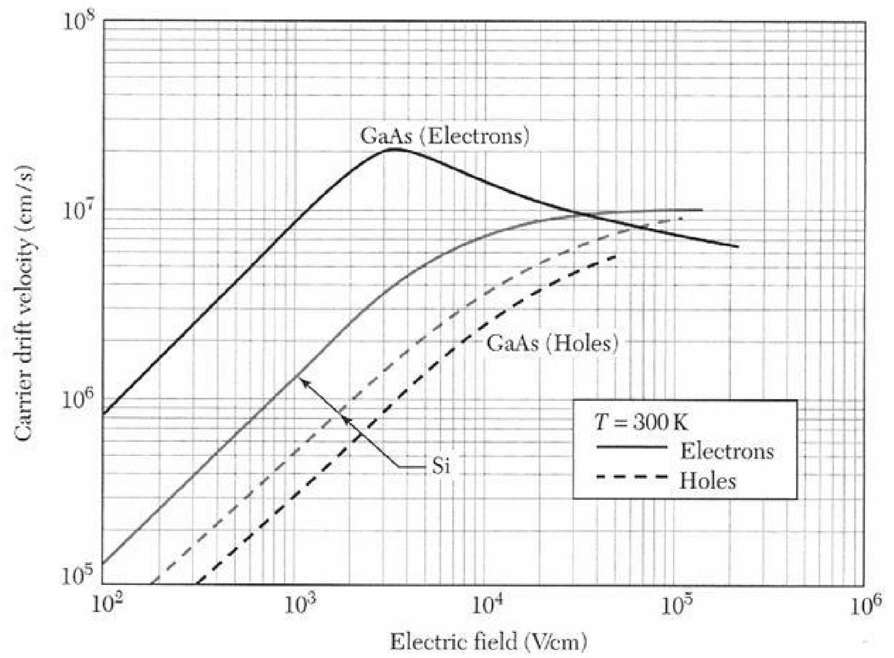
$$\tilde{i}_{in} = 2\pi f C_G \tilde{v}_G \qquad \tilde{i}_{out} = g_m \tilde{v}_G$$

$$\tilde{i}_{in} < \tilde{i}_{out}$$

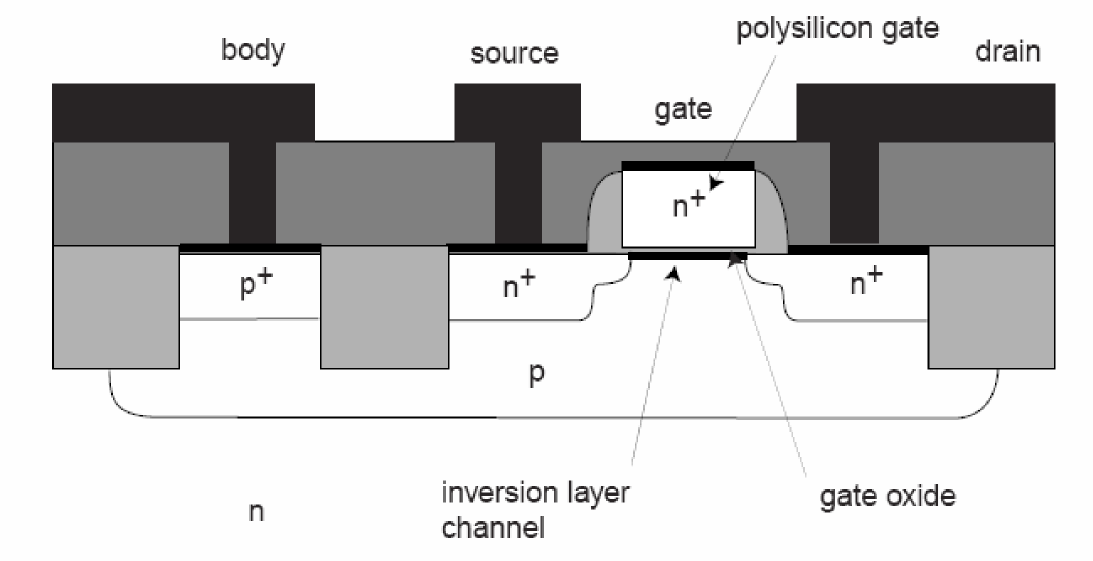
$$f < \frac{g_m}{2\pi C_G} \propto \frac{1}{s^2} = f_T$$

For large *E*, Ohm's law ($j = ne\mu E$) is not valid. The electron velocity saturates. For velocity saturation:

$$f_T \approx \frac{v_s}{L}$$



Constant E-field Scaling



Gate length L, transistor width Z, oxide thickness t_{ox} are scaled down.

V_{ds}, V_{gs}, and V_T are reduced to keep the electric field constant.

Power density remains constant.

$$L \sim 45\ t_{ox}$$

1975 - 1990: "Days of happy scaling"

Constant E-field scaling

$$I_{sat} = \frac{Z}{2L}\mu_n \frac{\varepsilon_{ox}}{t_{ox}}\left(V_G - V_T\right)^2$$

$$L \Rightarrow sL, \qquad Z \Rightarrow sZ, \qquad t_{ox} \Rightarrow st_{ox}, \qquad V_{th} \Rightarrow sV_{th}$$

$$I_{sat} \Rightarrow sI_{sat} \qquad \longleftarrow$$ I_{sat} gets smaller

$$g_m = \frac{dI_D}{dV_G} = \frac{Z}{L}\mu_n \frac{\varepsilon_{ox}}{t_{ox}}\left(V_G - V_T\right) \qquad \longleftarrow$$ Transconductance stays the same.

Power per transistor decreases like L^2. Power per unit area remains constant.

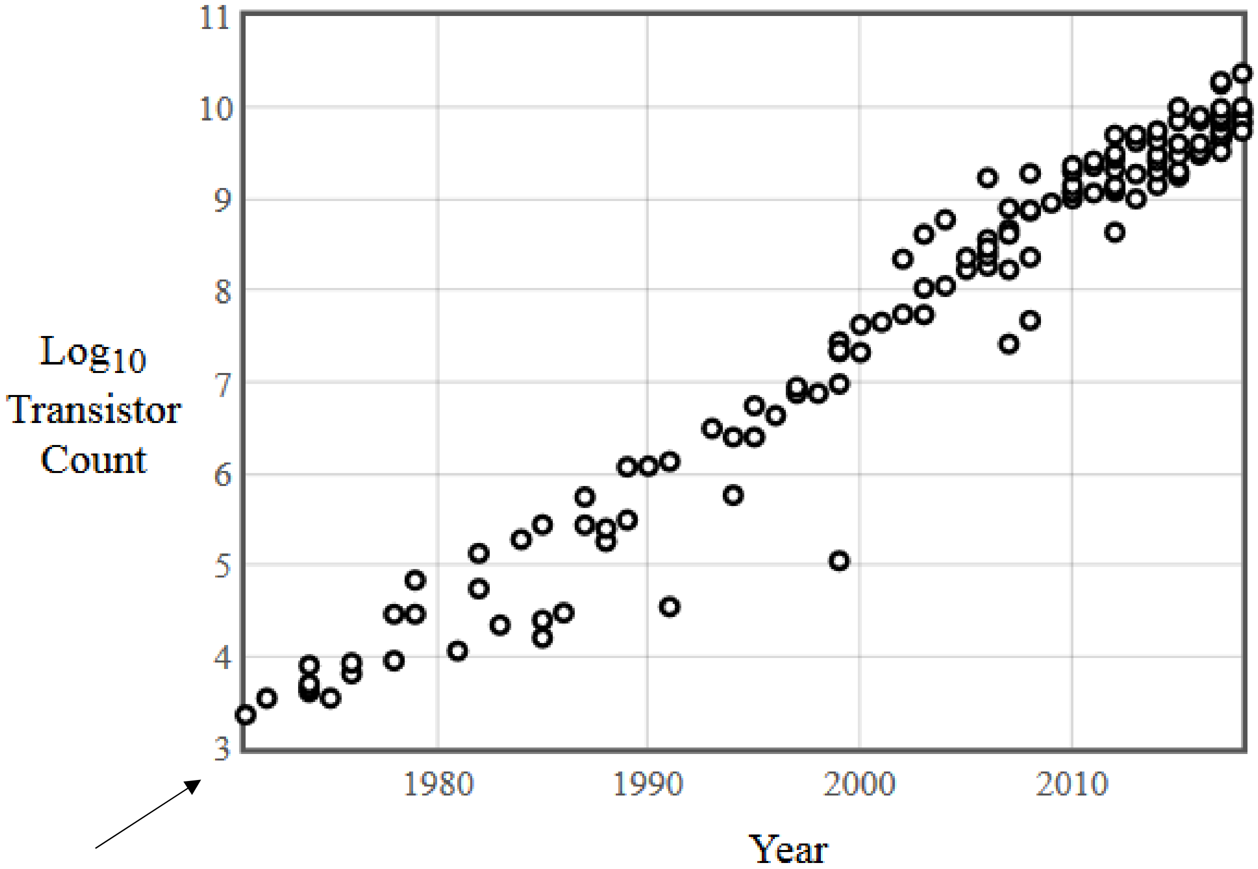
The heat dissipation problem

Microprocessors are hot ~ 100 C
Hotter operation will cause dopants to diffuse

When more transistors are put on a chip they must dissipate less power.

Power per transistor decreases like L^2.

Transistor Count 2018

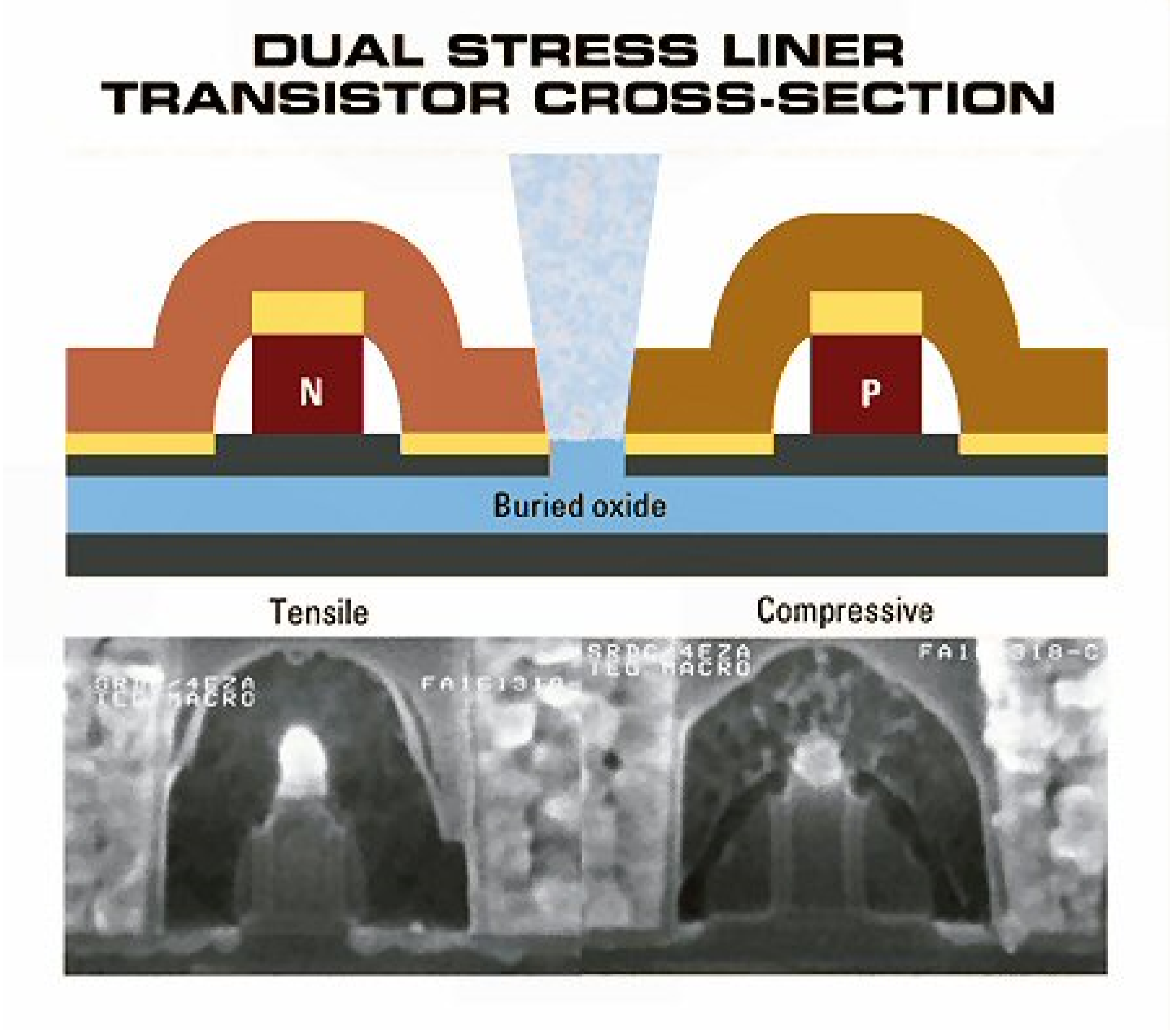


Jan 1 1970

Transistor count doubles about every 2 years

https://en.wikipedia.org/wiki/Transistor_count

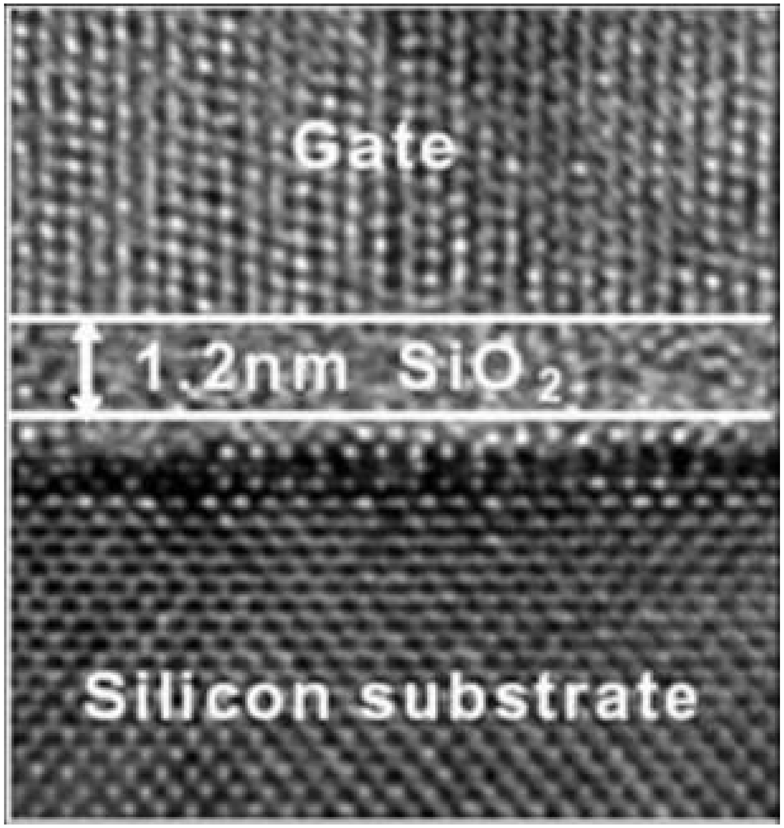
Dual stress liners



Tensile silicon nitride film over the NMOS and a compressive silicon nitride film over the PMOS improves the mobility.

http://www.xbitlabs.com/articles/cpu/display/athlon64-venice_2.html

Gate dielectric

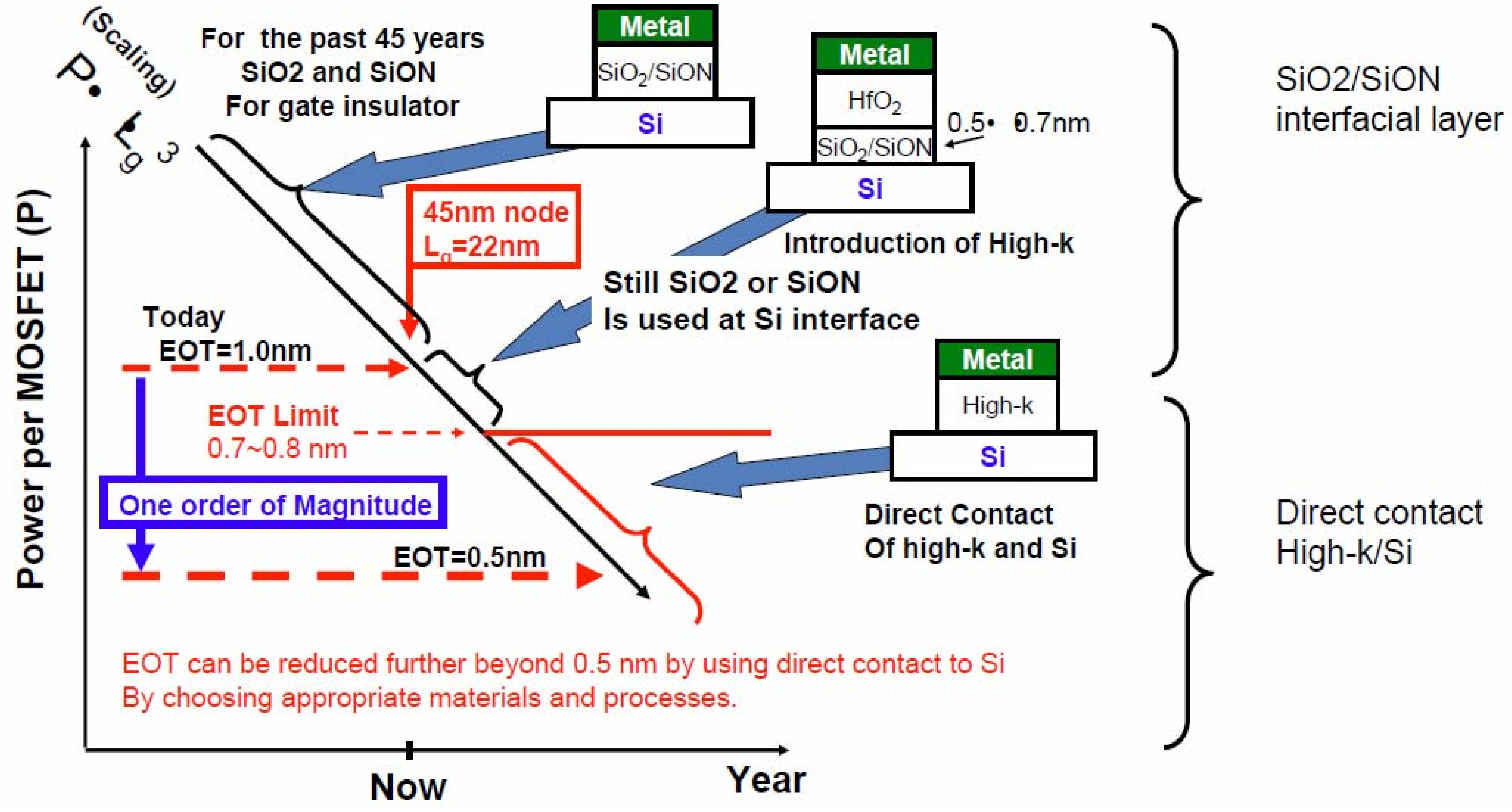


Thinner than 1 nm: electrons tunnel

Large dielectric constant desirable
$\varepsilon_r(SiO_2) \sim 4$

$\varepsilon_r(Si_3N_4) \sim 7$

Direct contact technology of high-k to Si



For the past 45 years
SiO2 and SiON
For gate insulator

Introduction of High-k

Still SiO2 or SiON
Is used at Si interface

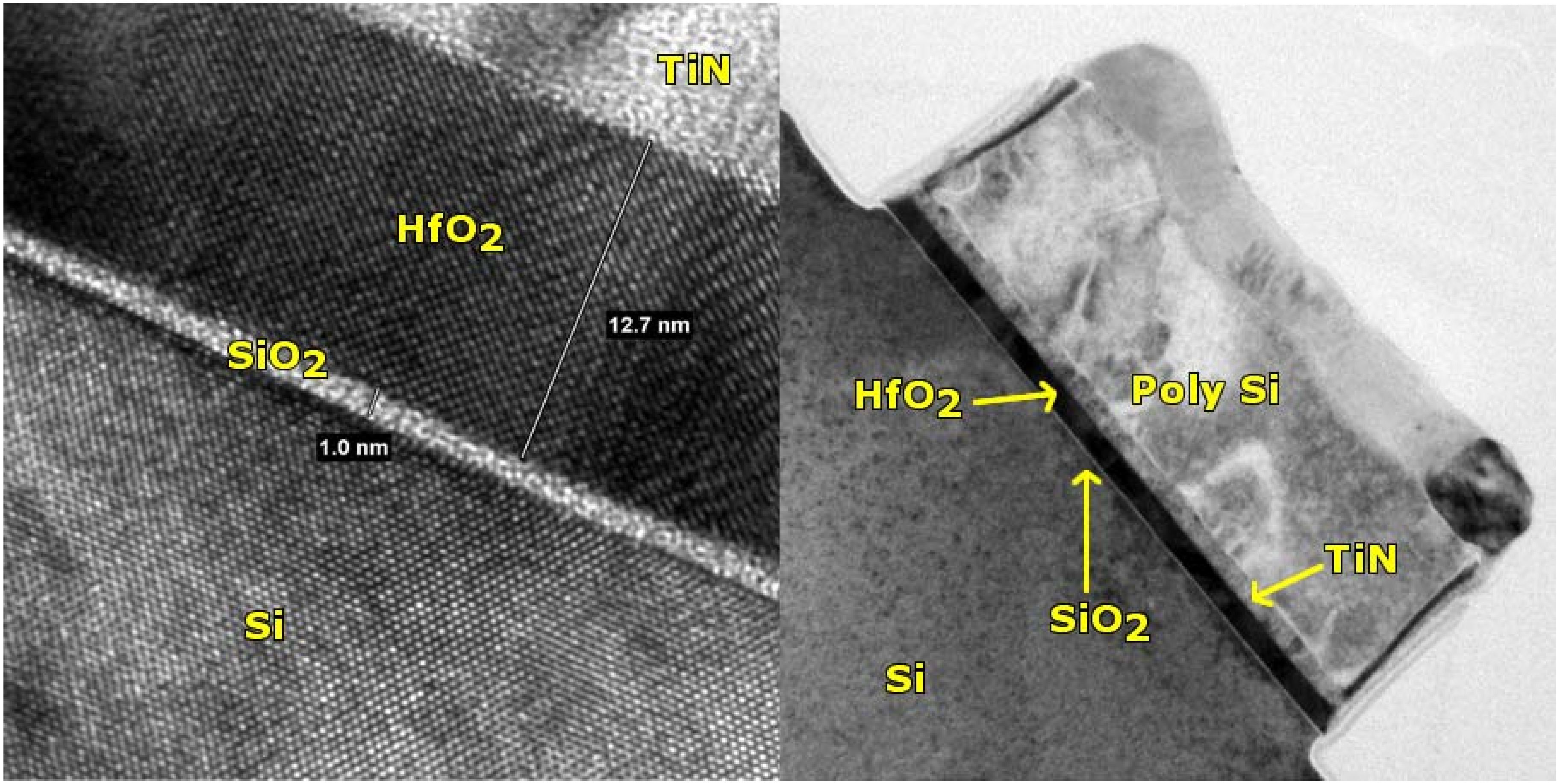
Direct Contact
Of high-k and Si

SiO2/SiON
interfacial layer

Direct contact
High-k/Si

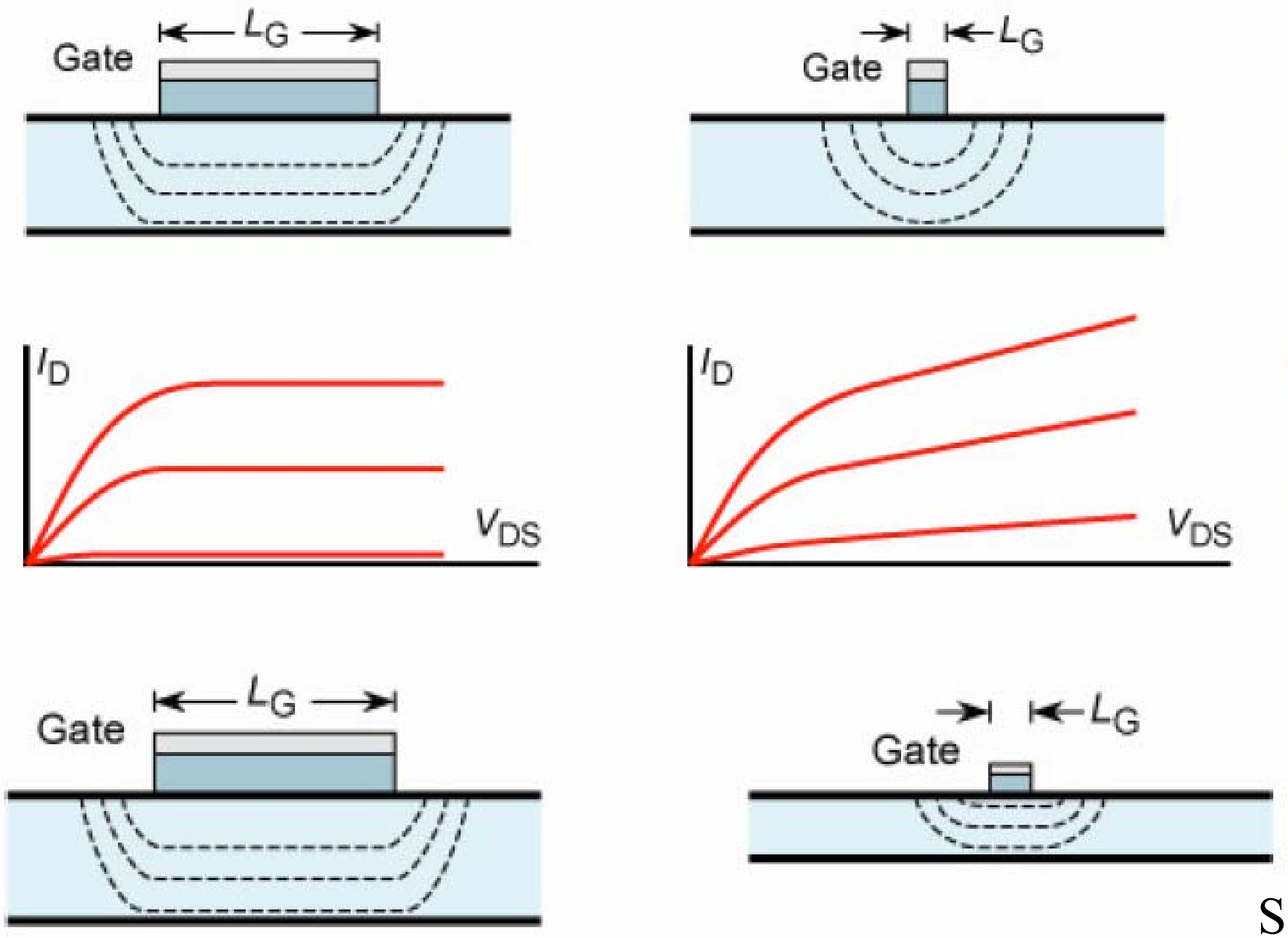
EOT can be reduced further beyond 0.5 nm by using direct contact to Si
By choosing appropriate materials and processes.

High-k dielectrics



http://nano.boisestate.edu/research-areas/gate-oxide-studies/

Short channel effects



Short-channel effects:

Threshold-voltage shift

Lack of pinch-off

Increased leakage current

Increase of output conductance

SOI: silicon on insulator

CMOS SOI

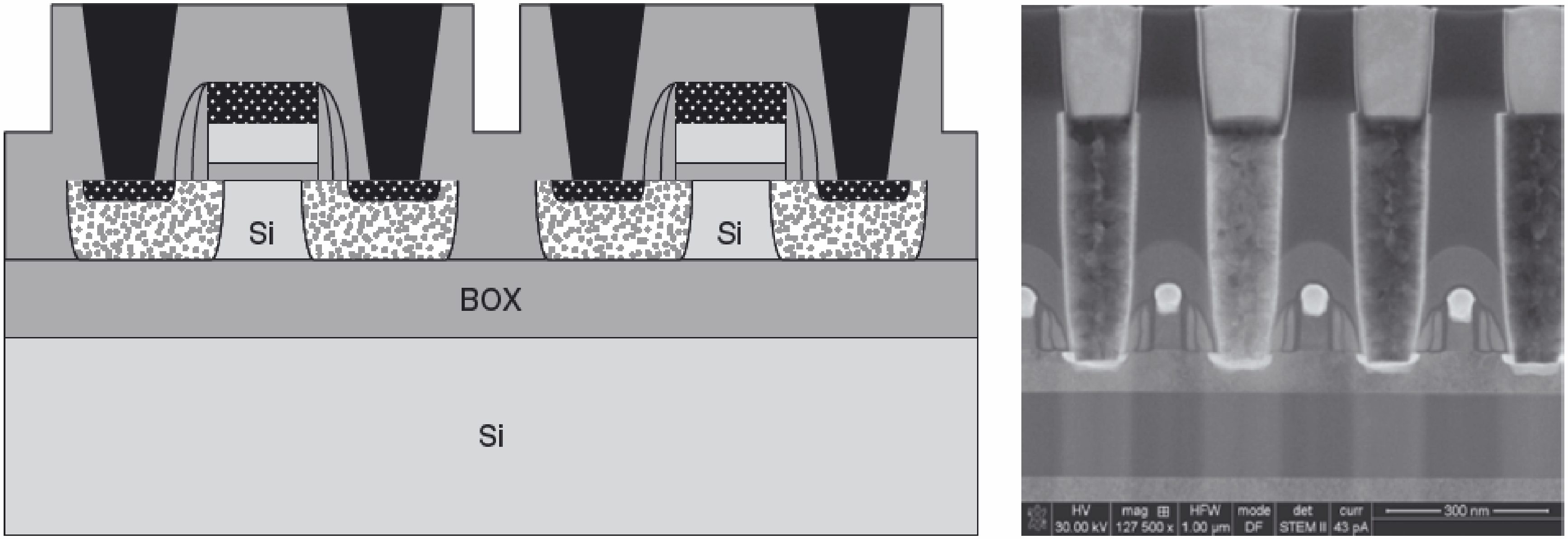
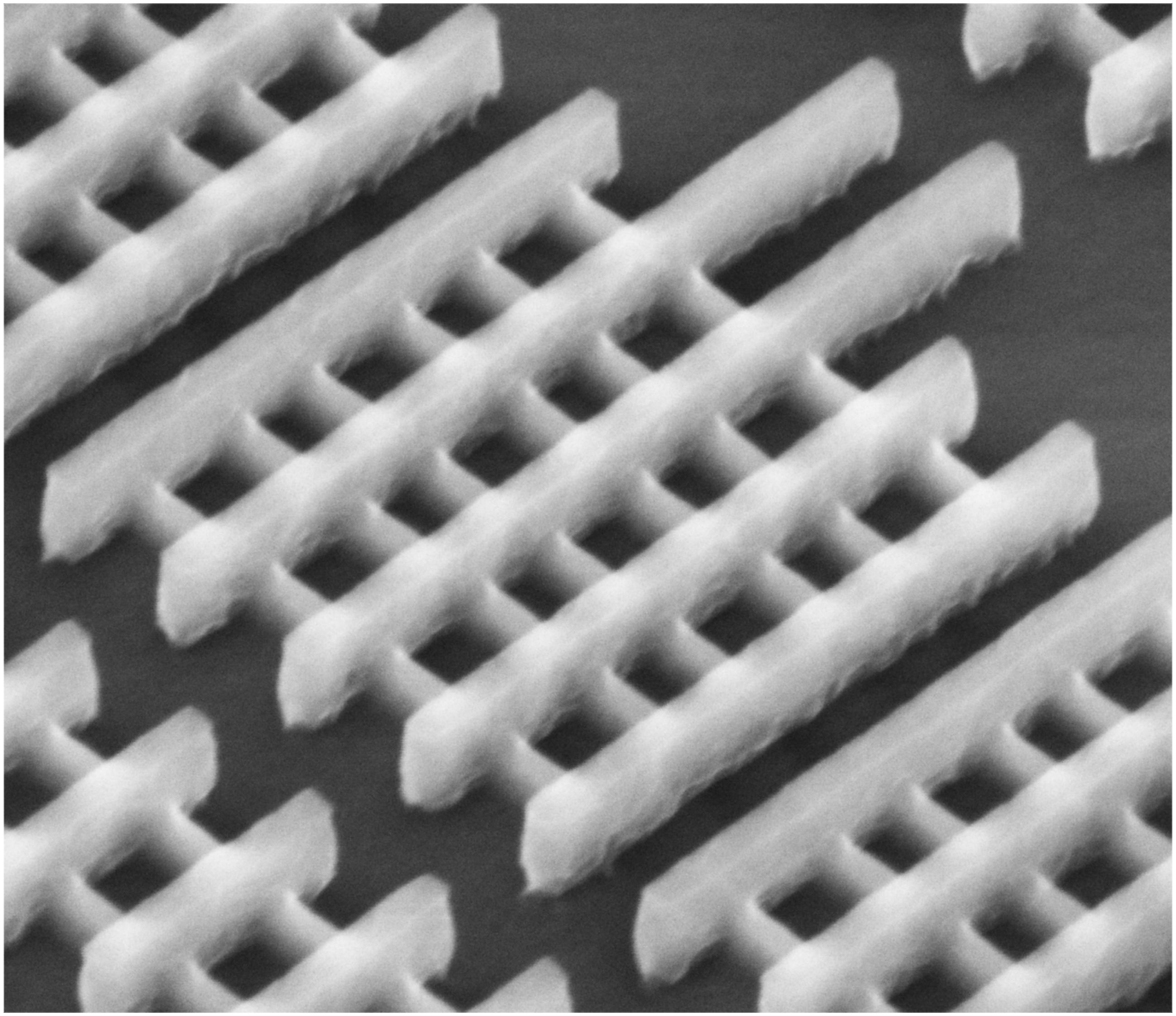


Figure 26.16 SOI MOSFET with first-level metal, schematic and TEM. Courtesy Brandon Van Leer, FEI Company4

Fransila

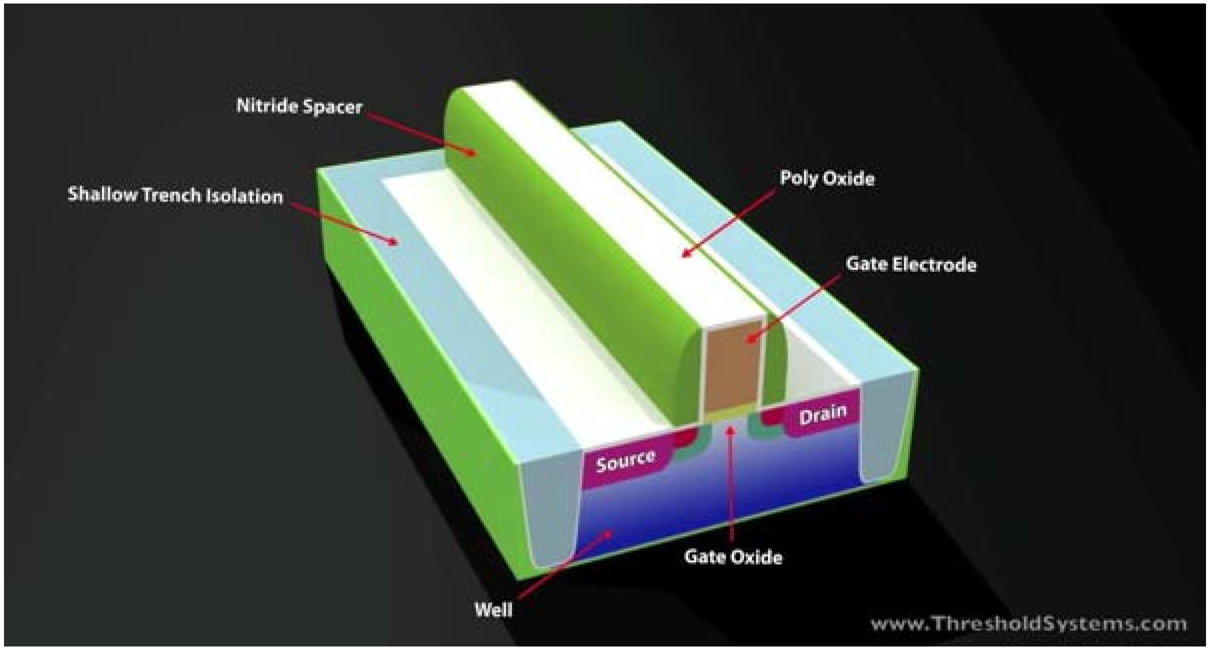
Intel® Pentium® 4	90 nm
Intel® Pentium® D	65 nm
Intel® Core™2 Duo	45 nm
Intel® Atom™ Z6xx Series	45 nm
Intel® Core™2 Celeron	45 nm
Intel® Core™ i7-900	32 nm
Intel® Xeon® 5600 Series	32 nm
Intel® Ivy bridge tri-gate	22 nm
Intel® Haswell FinFET	16 nm

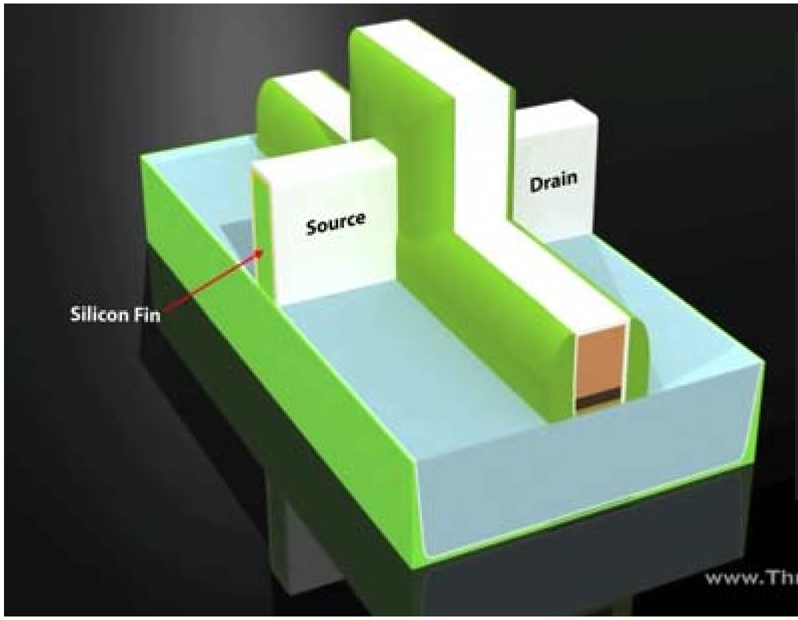
Intel 22nm 3D tri-gate transistor

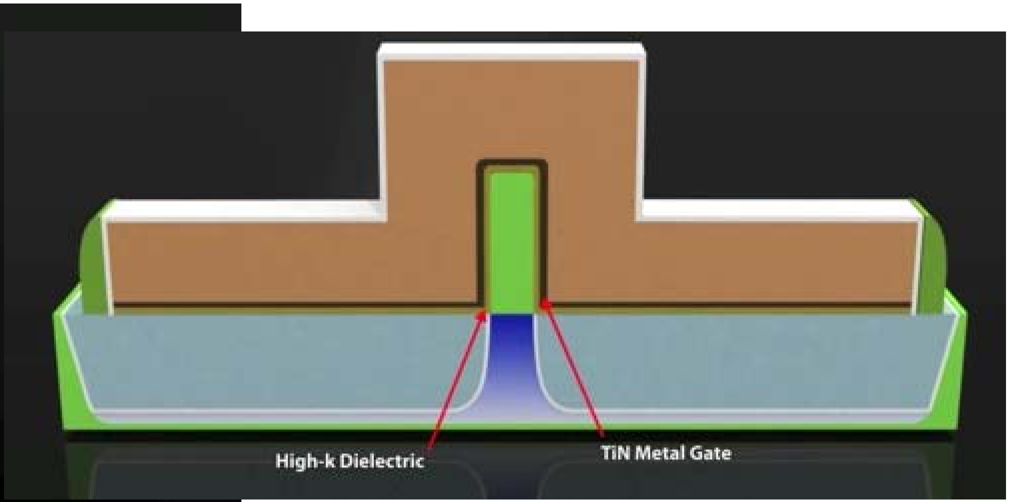


http://download.intel.com/newsroom/kits/22nm/gallery/images/Intel-22nm_Transistor.jpg

FinFET



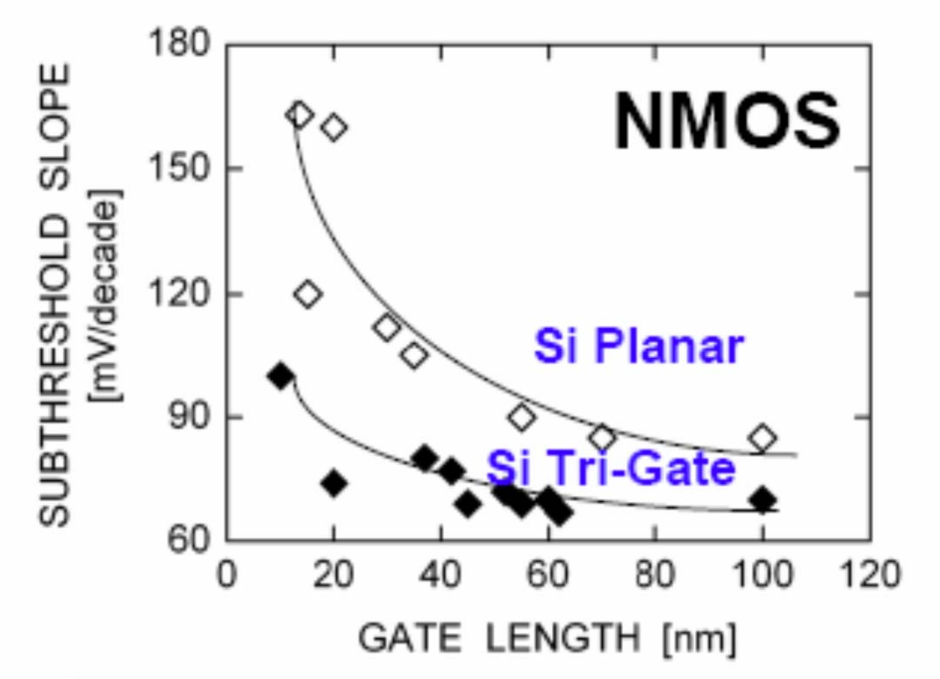


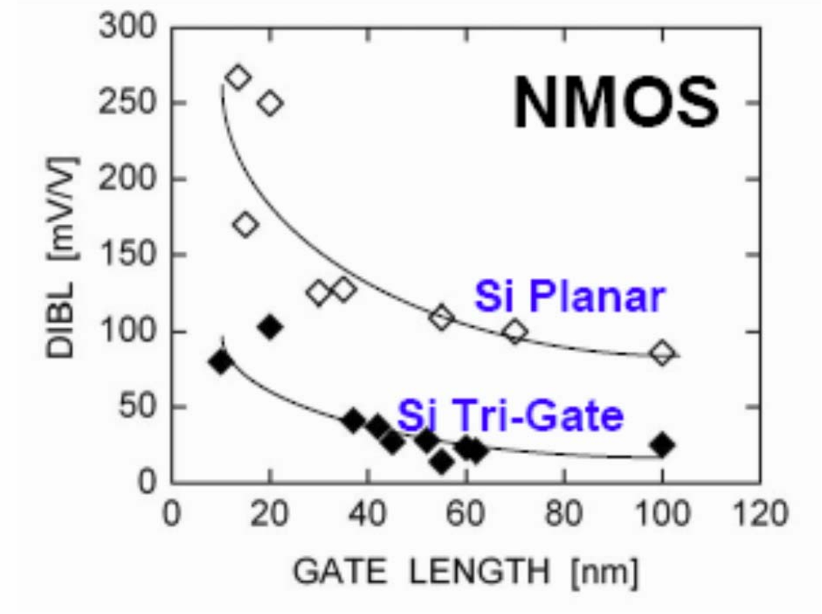


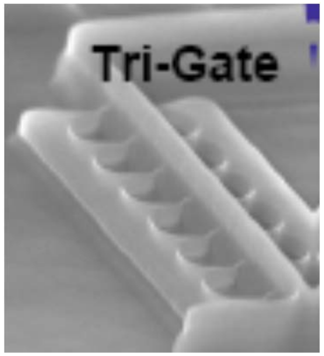
https://www.youtube.com/watch?v=Jctk0DI7YP8

FinFET, Tri-gate

Drain induced barrier lowering



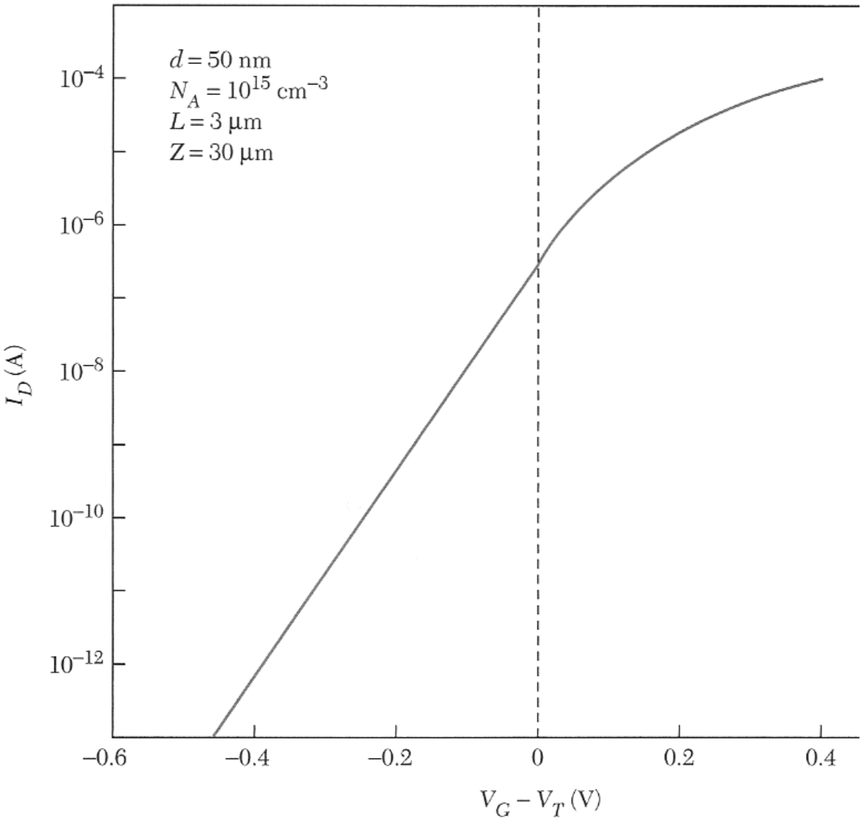




Robert Chau, Intel

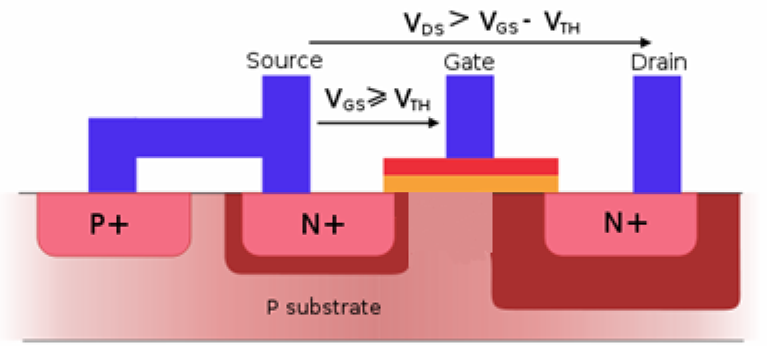
Subthreshold current

For $V_G < V_T$ the transistor should switch off but there is a diffusion current. The current is not really off until ~ 0.5 V below the threshold voltage.



Weak inversion

$$I_D \propto \exp\left(\frac{e(V_G - V_T)}{k_B T}\right)$$



Subthreshold swing: 70-100 mV/decade