12. Memories / Bipolar transistors

Jan. 9, 2019

Exams

January 31
March 8
May 17
June 19
October ...

Exam

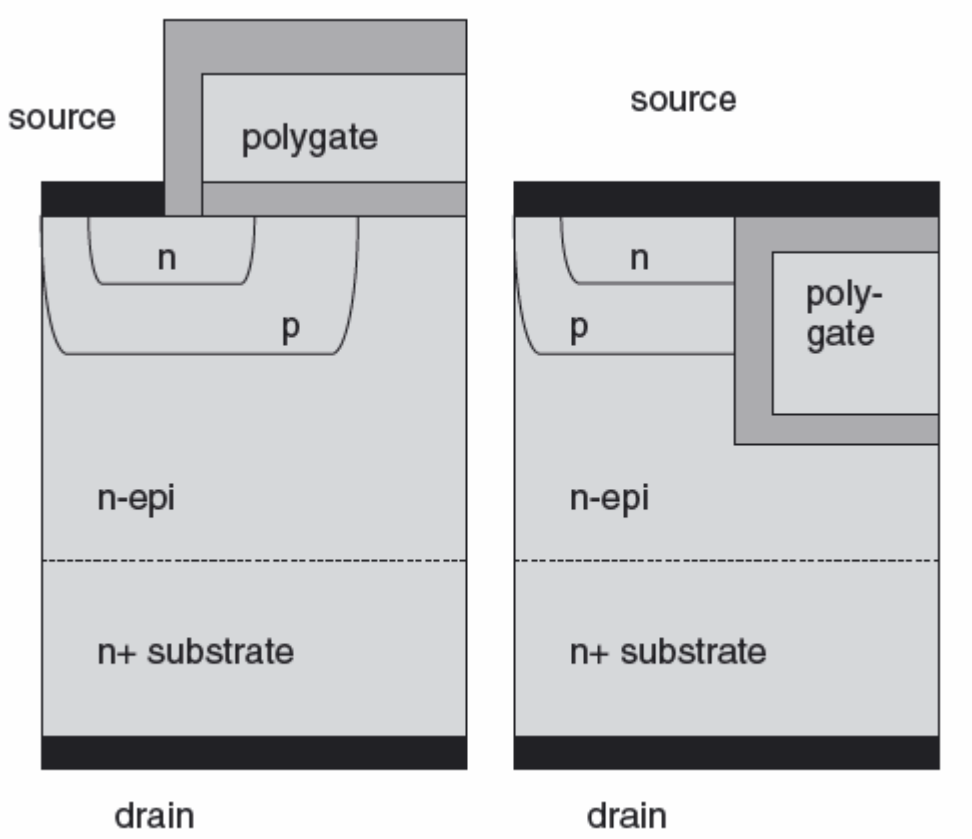
Calculator is ok. One A4 of handwritten notes.

Explain some concept:
(tunnel contact, indirect band gap, thermionic emission, inversion, threshold voltage, ...)

Perform a calculation:
(concentration of minority carriers, integrate charge density to find electric field, ...)

Explain how a device works:
(JFET, MESFET, MOSFET, laser diode, bipolar transistor, LED, Schottky diode, Heterojunction bipolar transistor, ...)

U-MOSFET and D-MOSFET

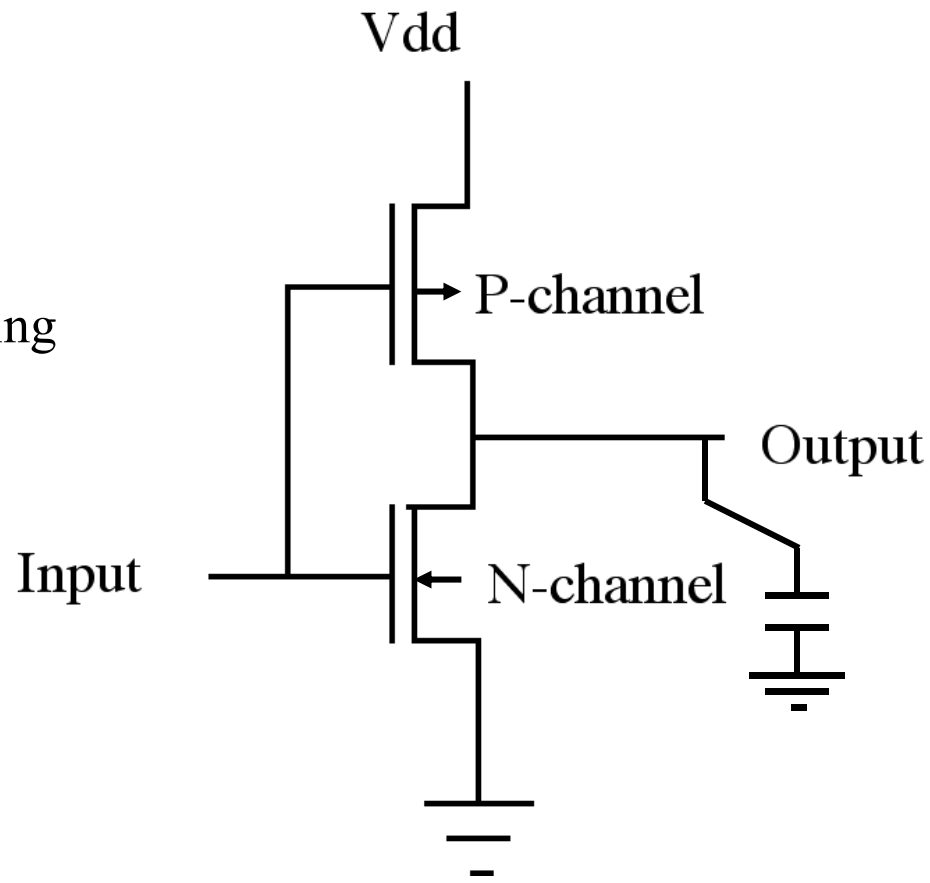


Fransila

Power transistors

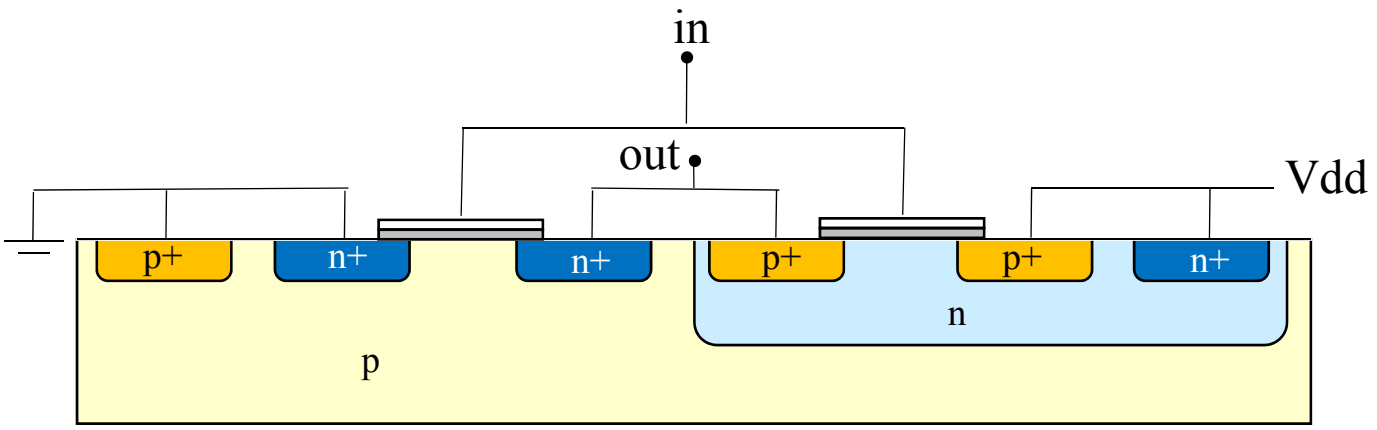
CMOS inverter

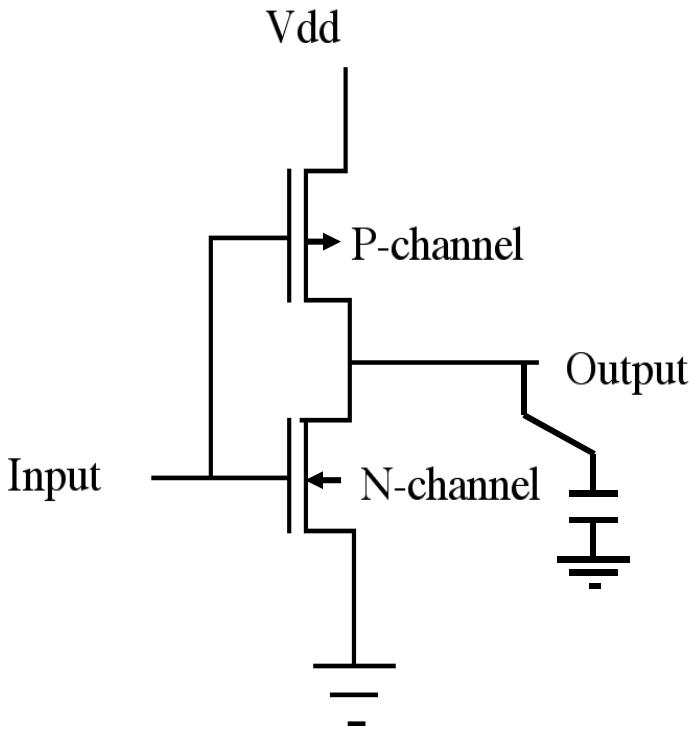
Dissipates little power
except when it is switching

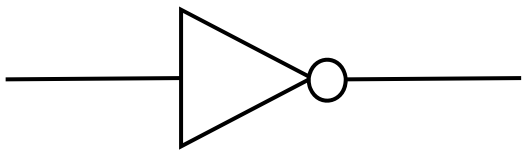


$$E = QV_{dd} = CV_{dd}^2$$

CMOS inverter

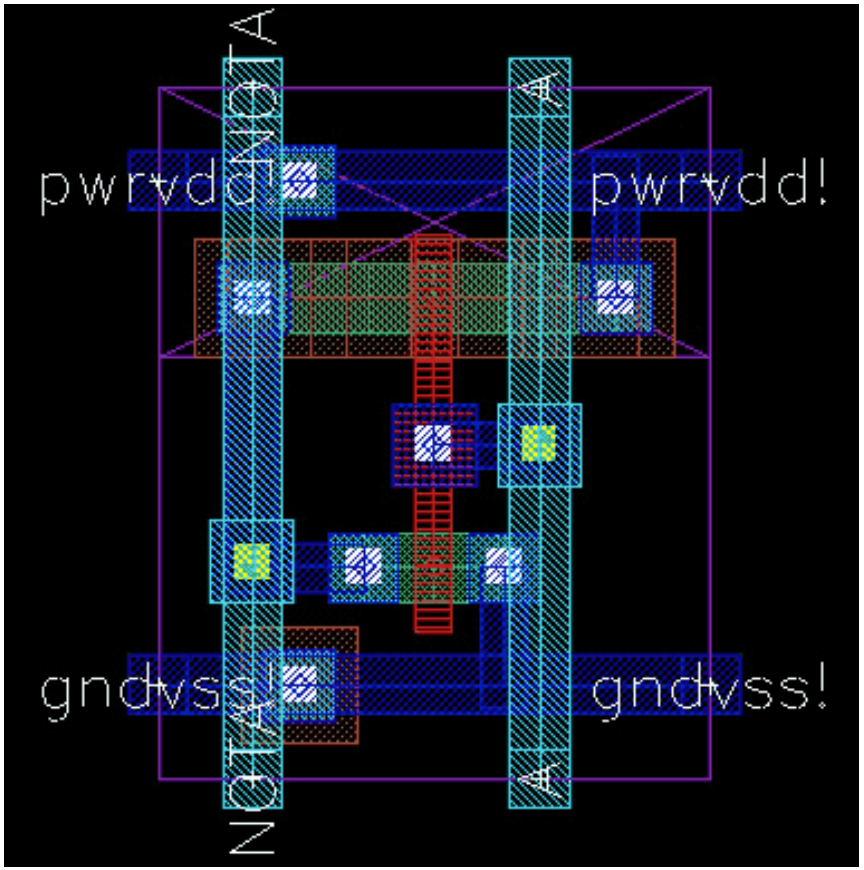


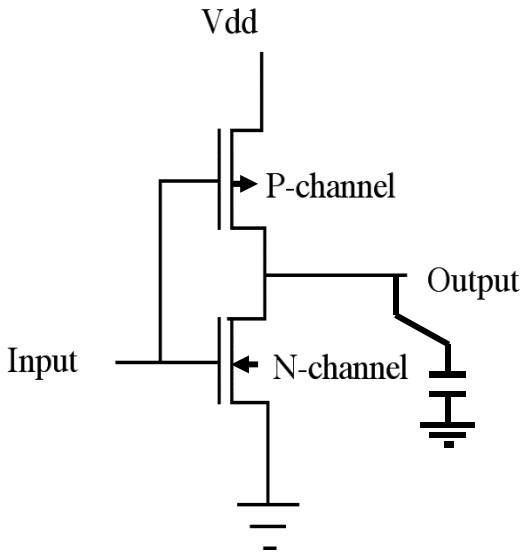


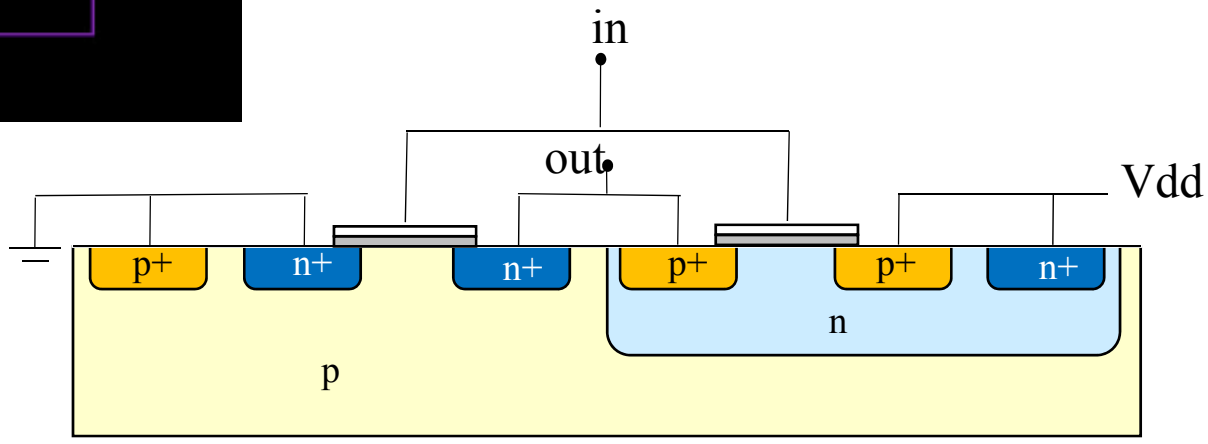


inverter

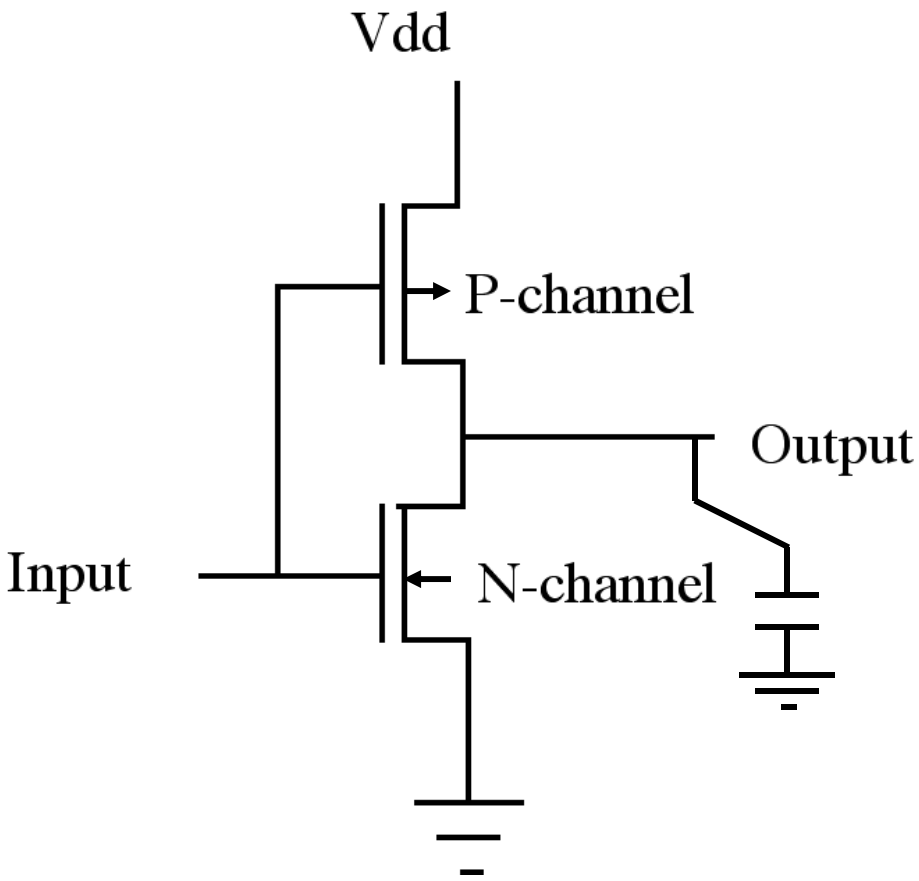
CMOS inverter



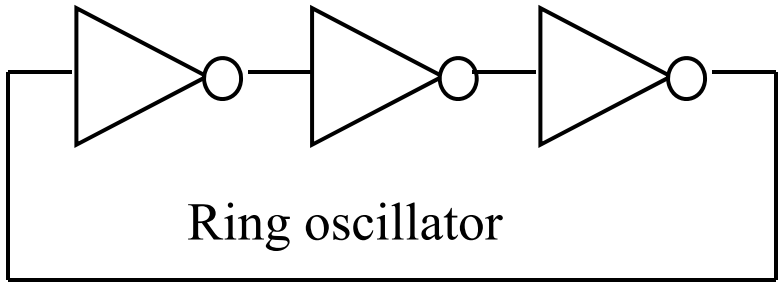




Gate delay

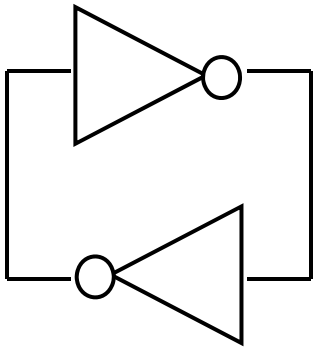


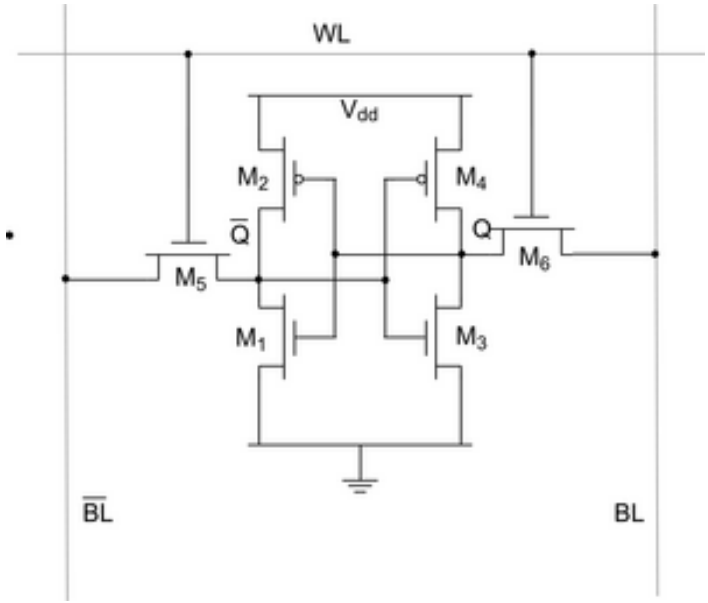
Gate delay is limited by $C_{gate}V_{dd}/I$.



SRAM

Static random access memory

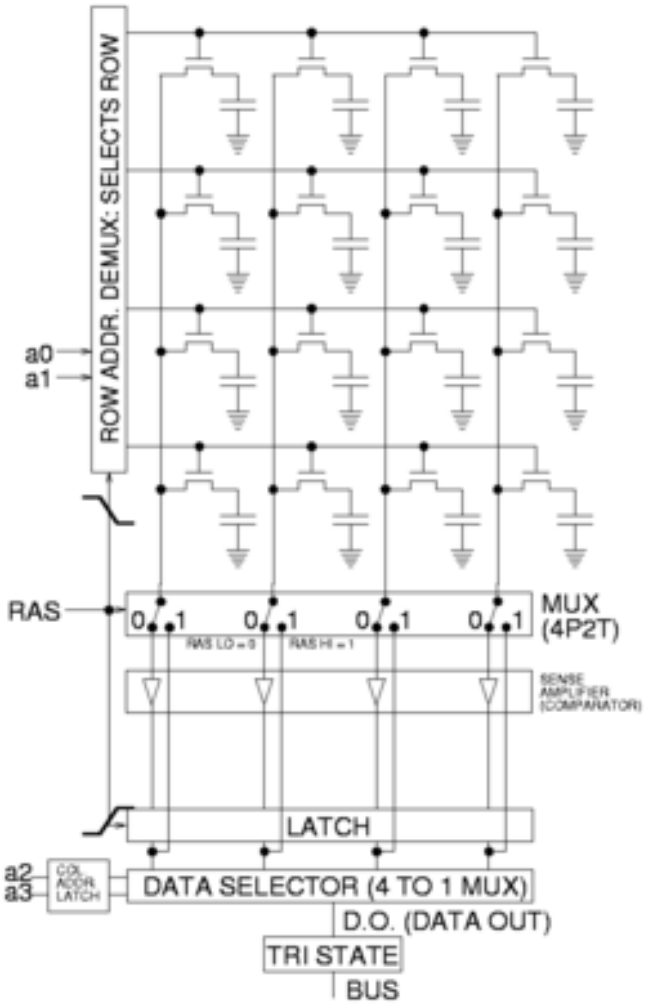




No refresh circuitry needed.

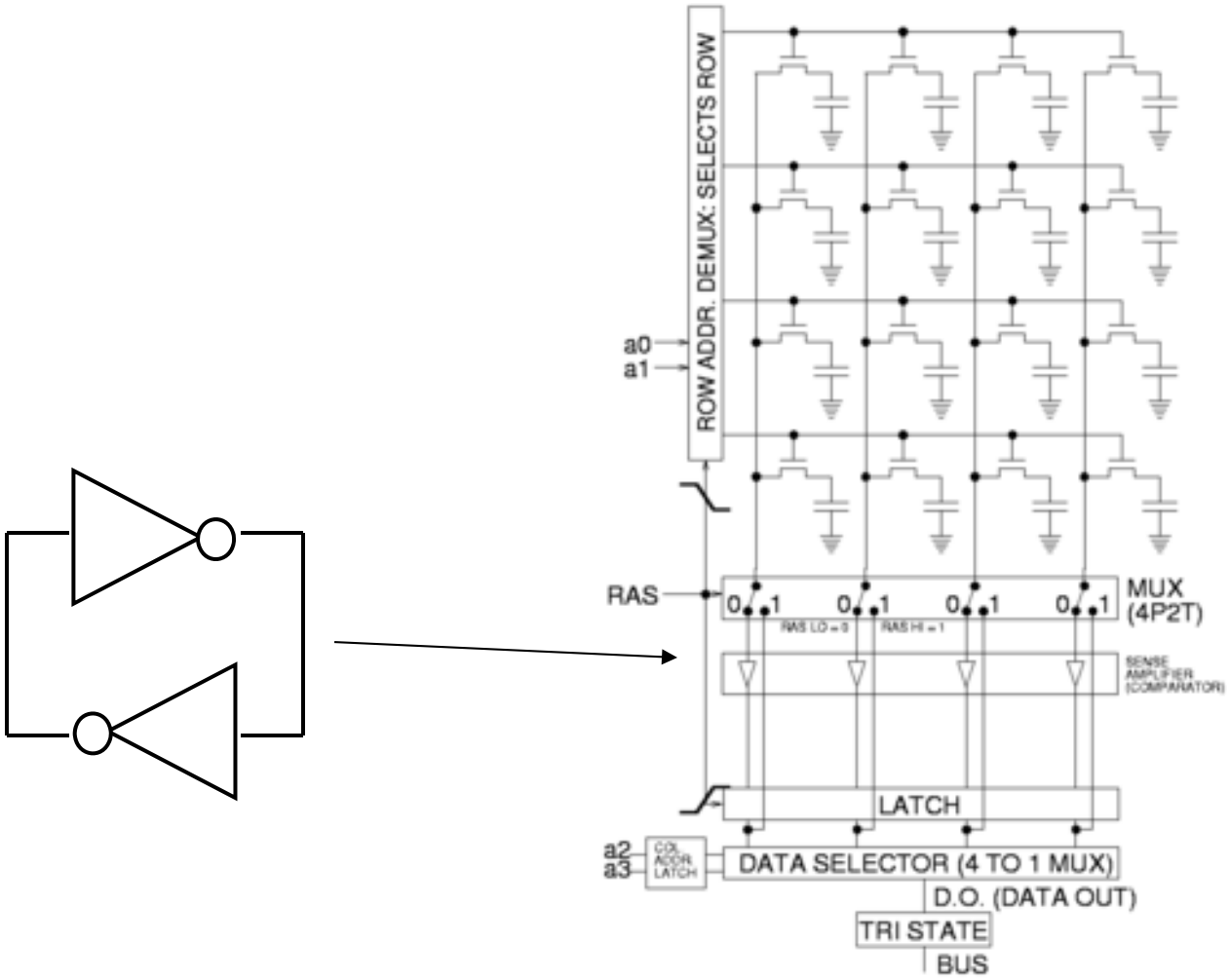
DRAM

Dynamic random access memory

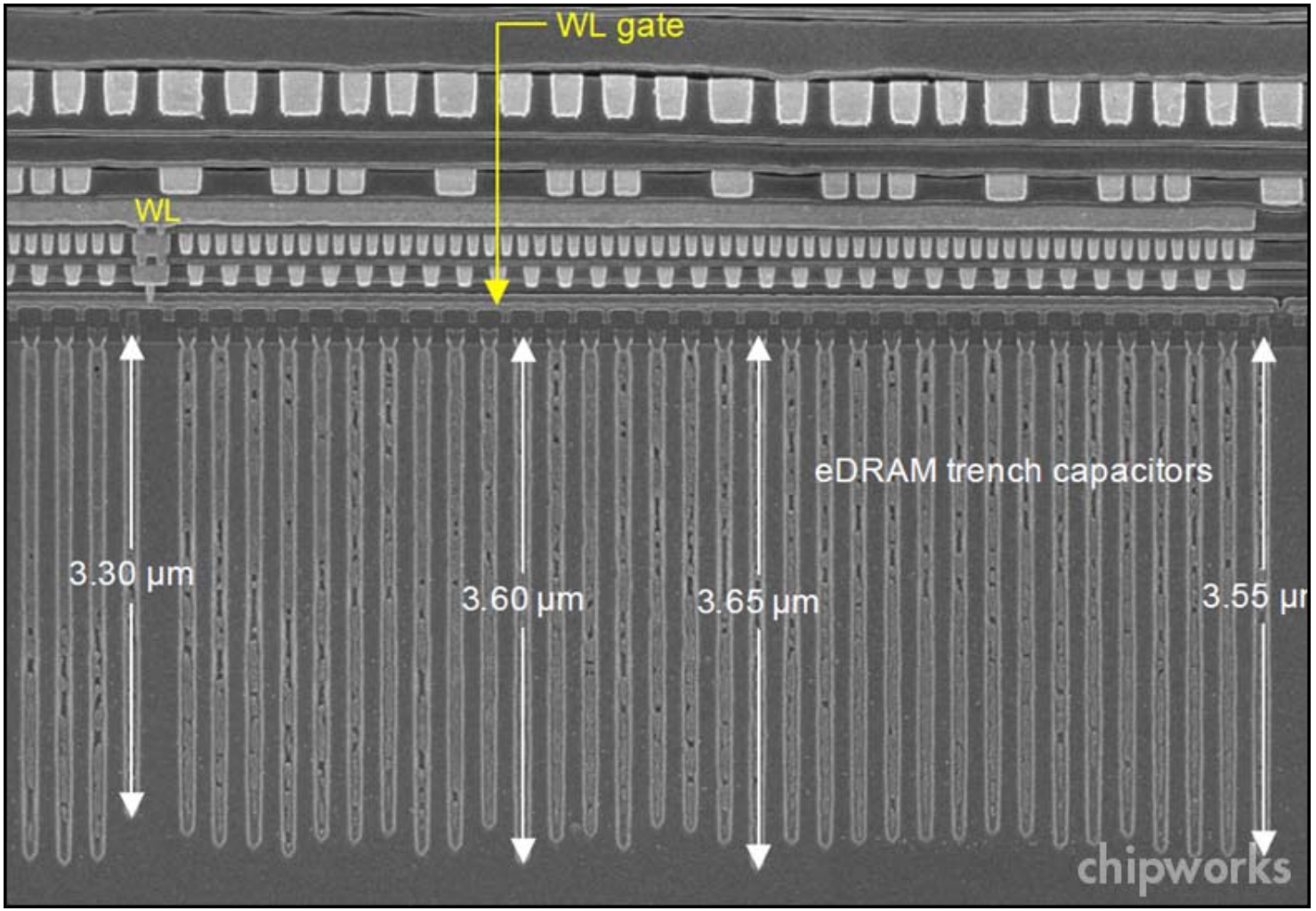


DRAM

Read and refresh DRAM with a SRAM cell



DRAM

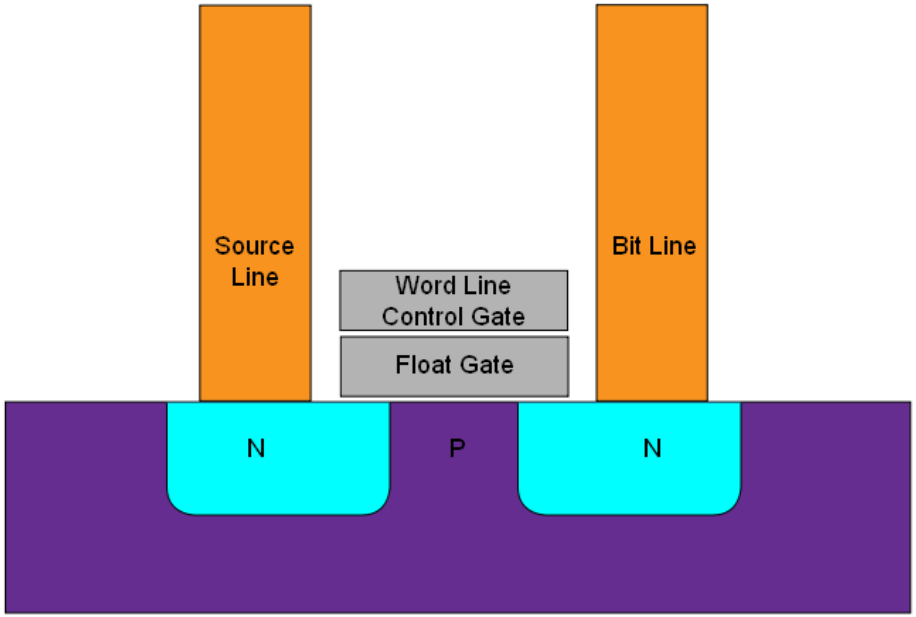


75:1

Silicon oxynitride SiO_xN_y dielectric

http://electroiq.com/chipworks_real_chips_blog/

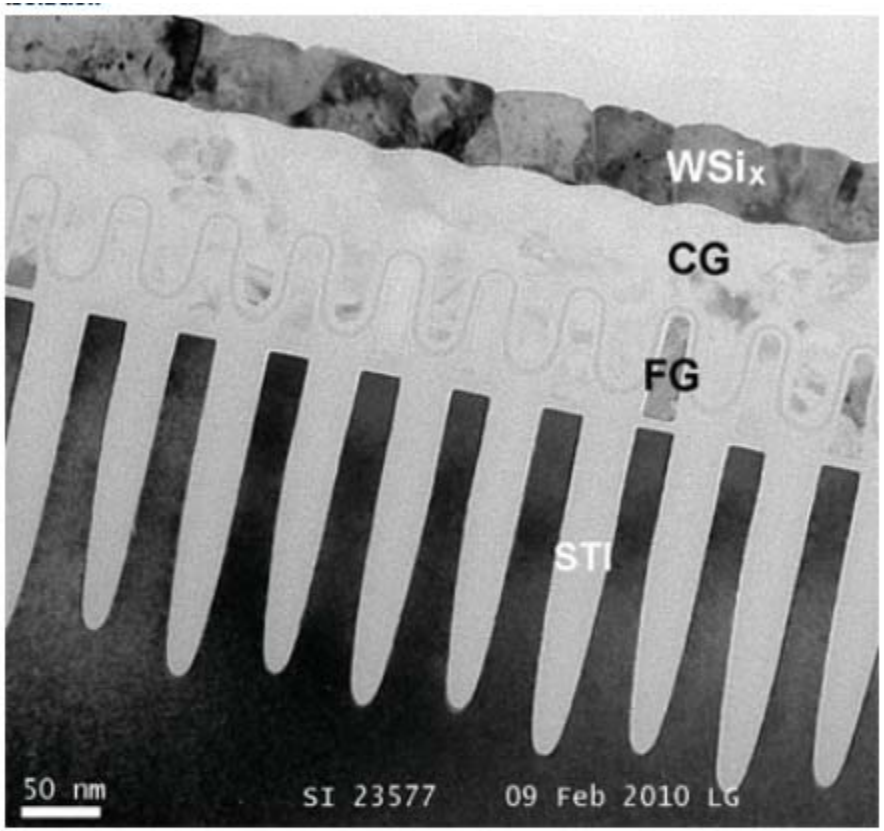
Flash memory



Charge is stored on a floating gate

nonvolatile

Intel Micron Flash Technologies (IMFT)
Shallow Trench Isolation (STI)
Control Gate (CG)
Floating Gate (FG)
Self-Aligned Doubled Patterning (SADP)



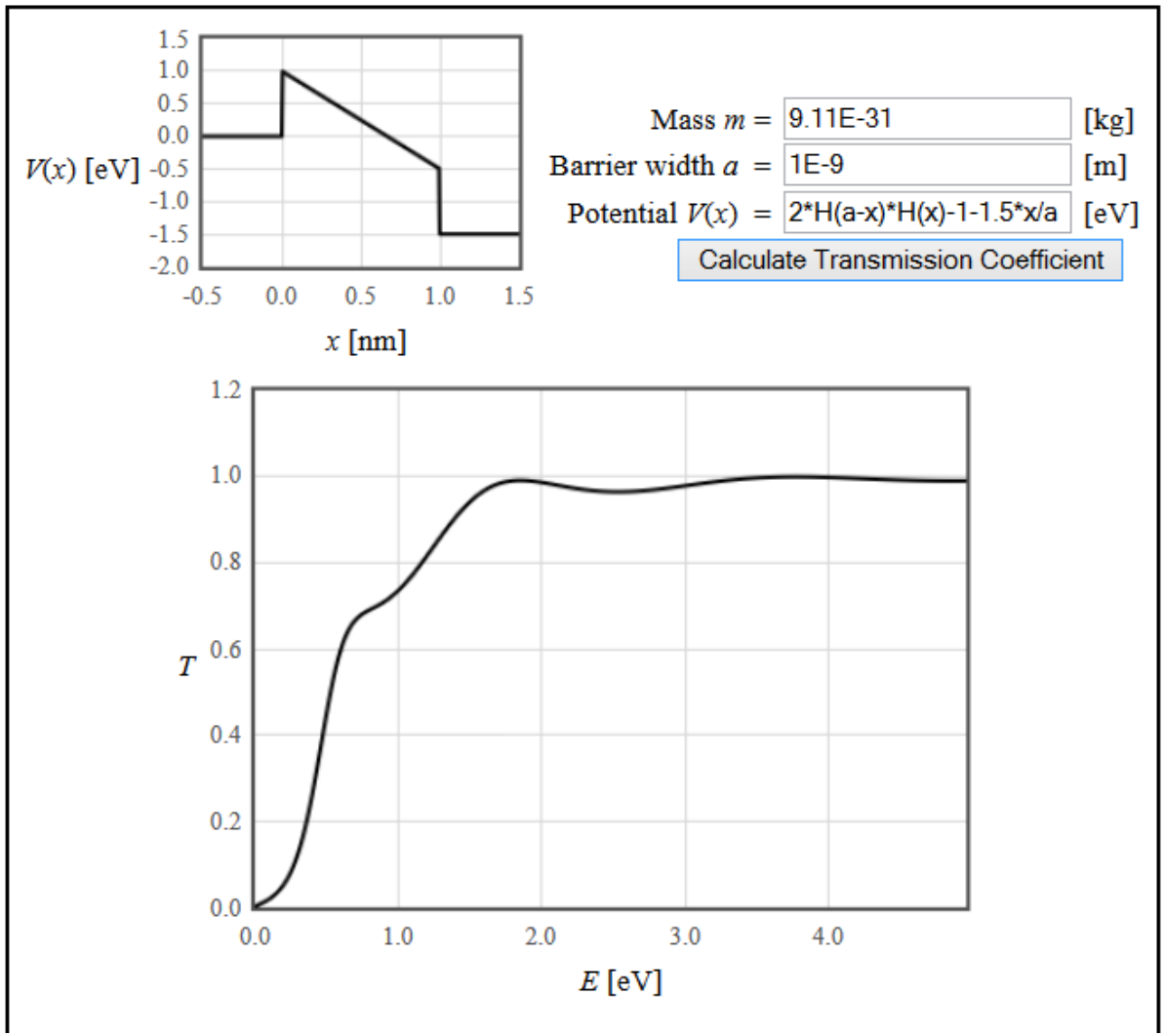
Topographical SEM image of the IMFT 25-nm flash memory array at gate level: array trench depth is shallower to allow a denser flash array

The extent of immersion-lithography tool usage cannot be known, but our end-of-the-wordline analysis and STI pattern analysis of the IMFT device has shown some interesting spacing patterns that could give useful insight into the lithography and SADP processes. Technically, immersion lithography is the mainstream technology for NAND flash integration for sub-50 nm and is used along with SADP to shrink line widths and avoid overlay issues. Strongly enhanced DP (two exposures + spacer approach) could extend immersion to 21 nm and beyond. Since the extreme ultraviolet lithography (EUVL) tool is not going to be ready till 2012, immersion would continue to fill the gap up to 2x-nm node and beyond.

http://www.dongyitech.com/en/newsdetail.asp?newsid=128

Tunneling through an arbitrarily shaped potential barrier

In quantum mechanics, there is some probability that a particle of mass m will tunnel through a potential barrier even if the energy of the particle is less than the energy of the barrier. During a direct tunneling process, the energy of the electron remains contant. The form below calculates the transmission coefficient for tunneling. The shape of the tunnel barrier can be arbitrarily defined in the interval between $x = 0$ and $x = a$. The potential is assumed to be constant to the left of the tunnel barrier at the value $V(x=0)$ and constant to the right of the barrier at the value $V(x=a)$.

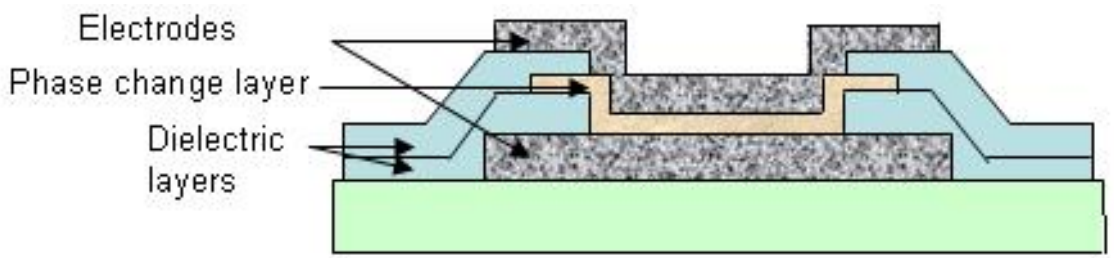


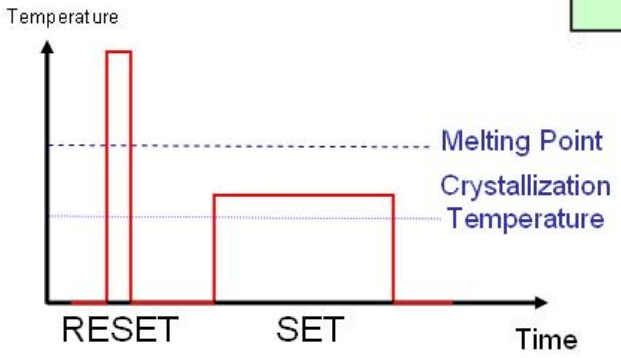
http://lamp.tu-graz.ac.at/~hadley/ss1/appendix/tunnel/tunneltrans.php

Phase change memory

Phase-change memory (PRAM) uses chalcogenide materials. These can be switched between a low resistance crystalline state and a high resistance amorphous state.

GeSbTe is melted by a laser in rewritable DVDs and by a current in PRAM.

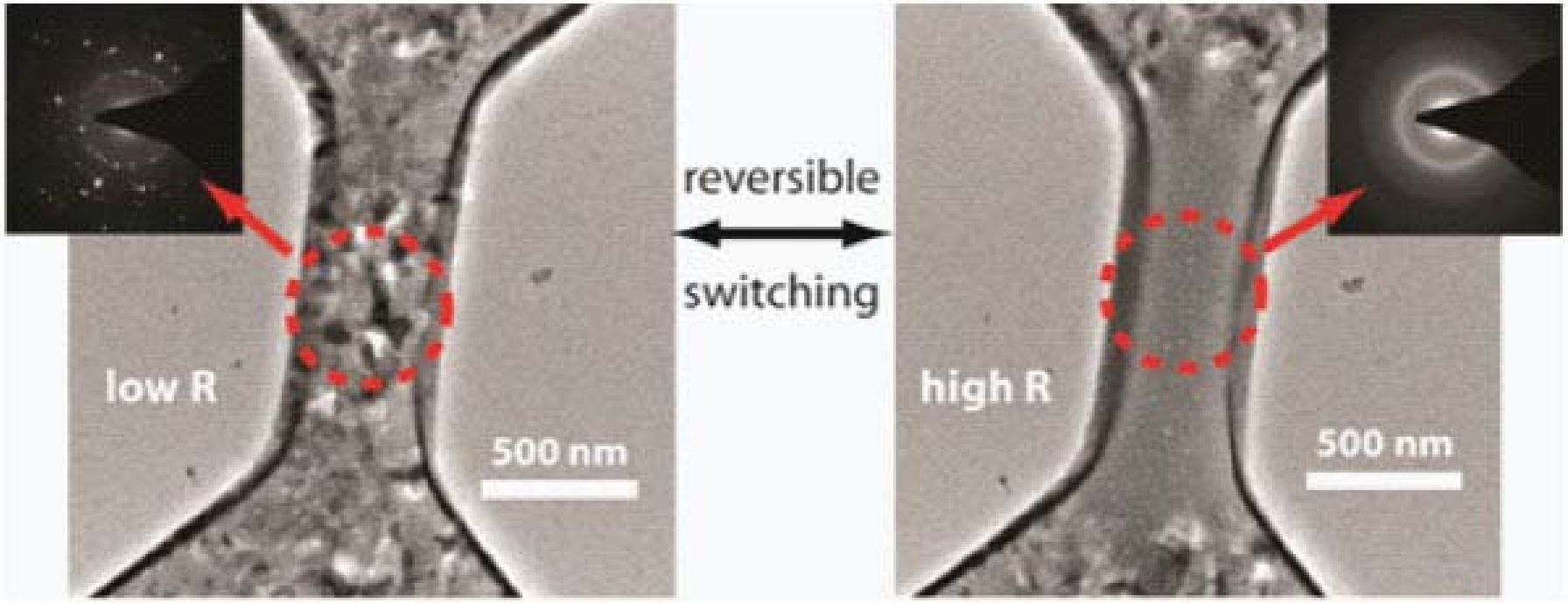




nonvolatile

Phase change material

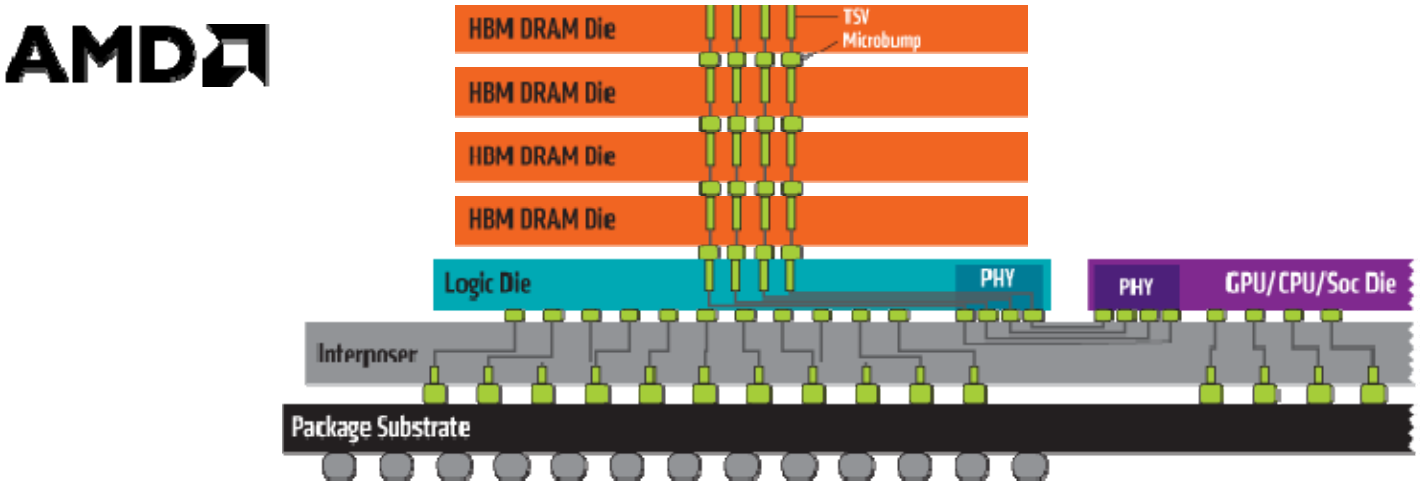
Electron diffraction in a TEM of a GeSbTe alloy.

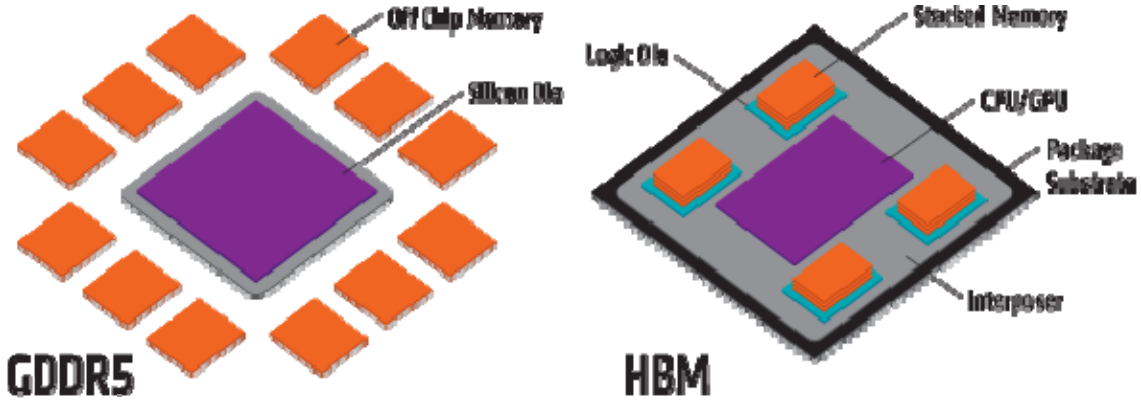


http://web.stanford.edu/group/cui_group/research.htm

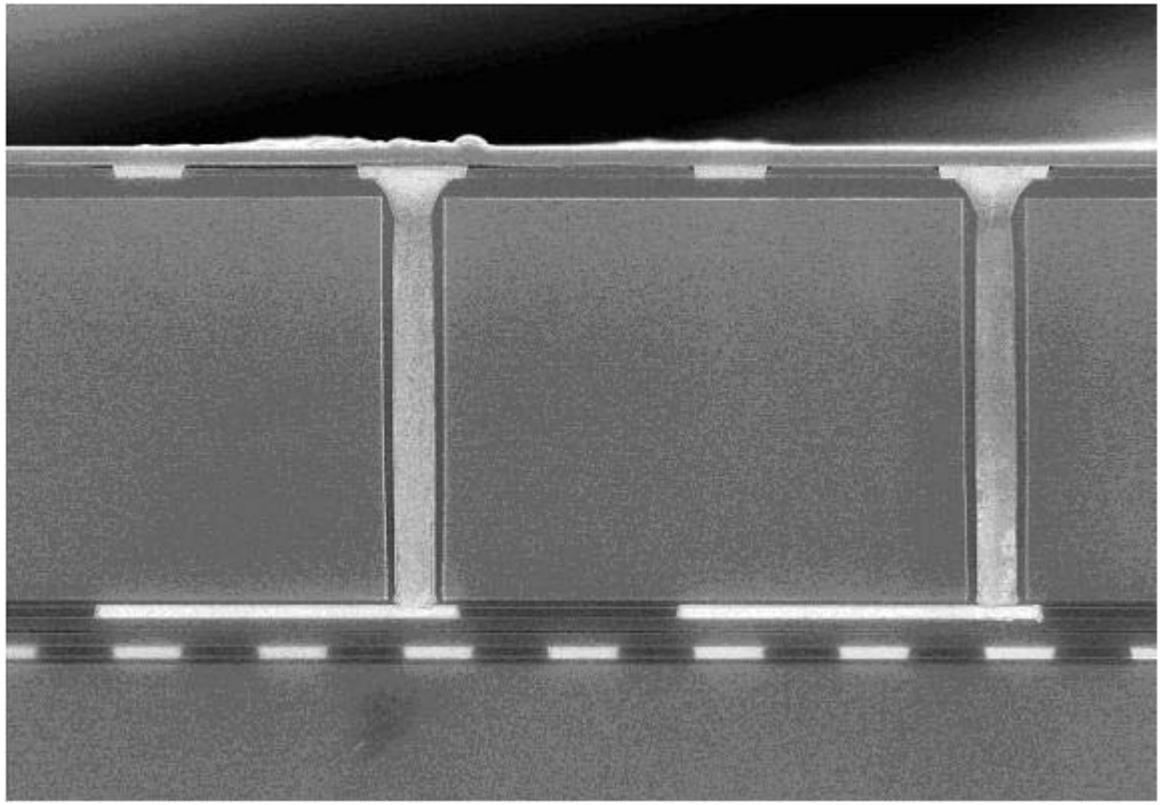
High Bandwidth Memory

AMD to launch its HBM graphics cards on 16 June 2015.





Through-Silicon Via (TSV)



A vertical electrical connection (via) passing completely through a silicon wafer.

Used in 3D integration.

http://javier.esilicon.com/2011/01/30/thru-silicon-vias-current-state-of-the-technology/

Bosch process

Repeat 2 processes over and over

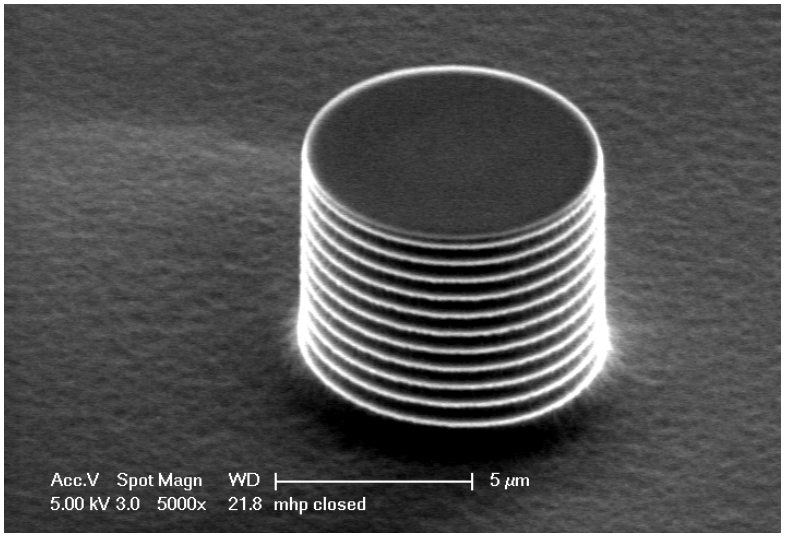
1. Etch Si with SF_6 (nearly isotropic)

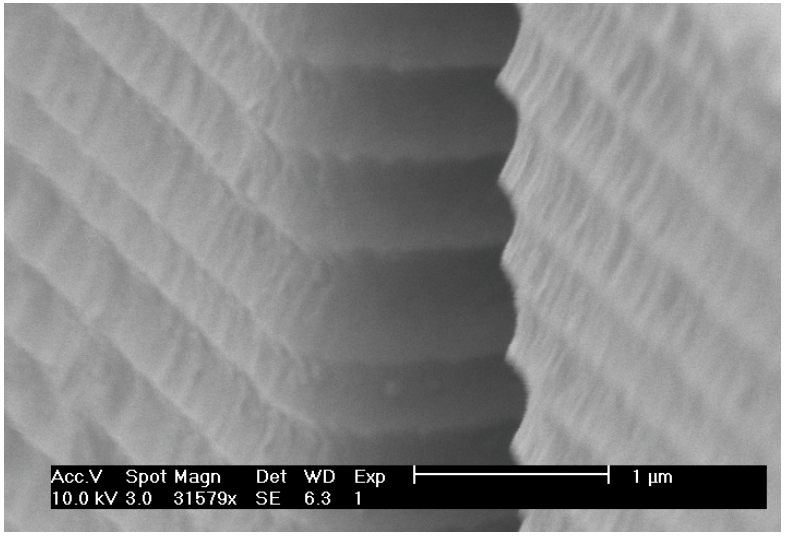
2. Deposit passivation layer C_4F_8

Directional etching at the bottom breaks through the passivation layer.

Short cycles: smooth walls

Long cycles: fast etching



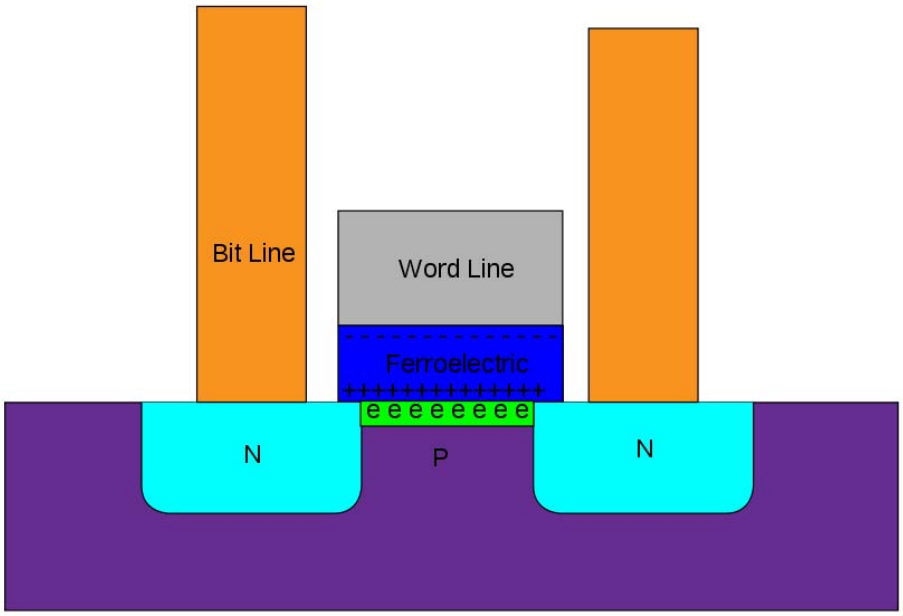


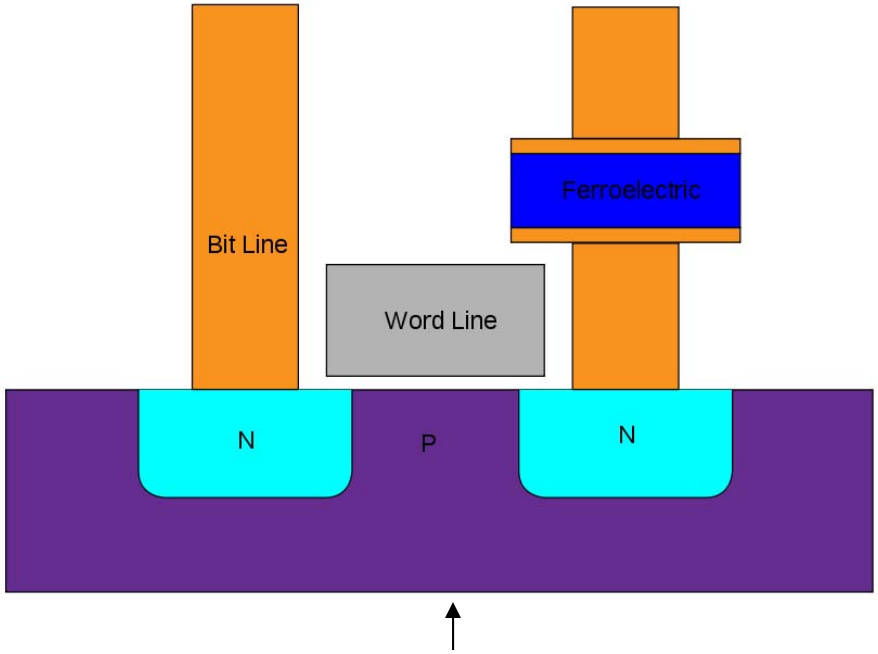
http://en.wikipedia.org/wiki/Deep_reactive-ion_etching

Ferroelectric RAM

FeRAM uses a Ferroelectric material like PZT to store information.

Sometimes used in smart cards.

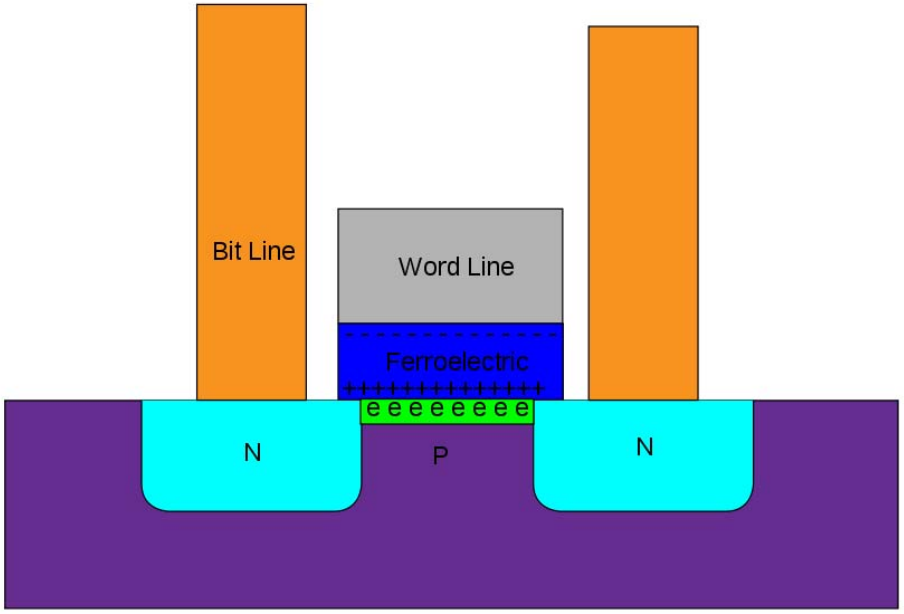


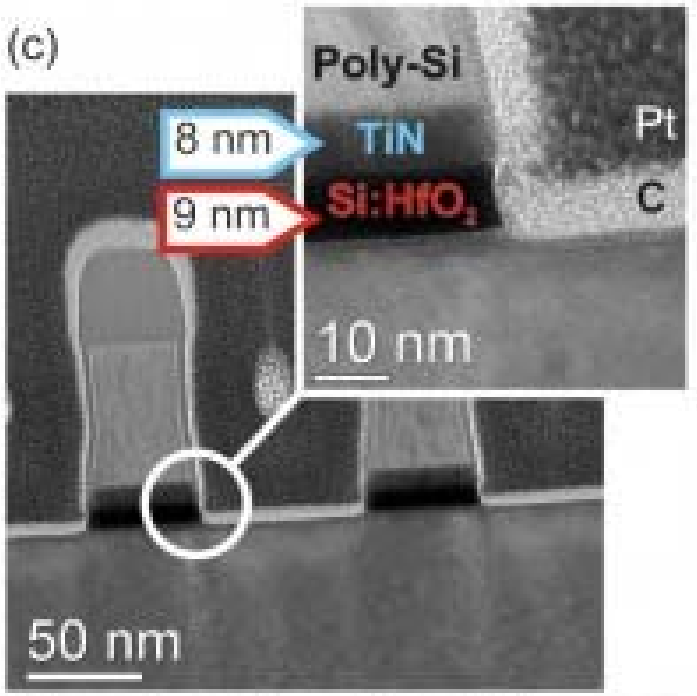


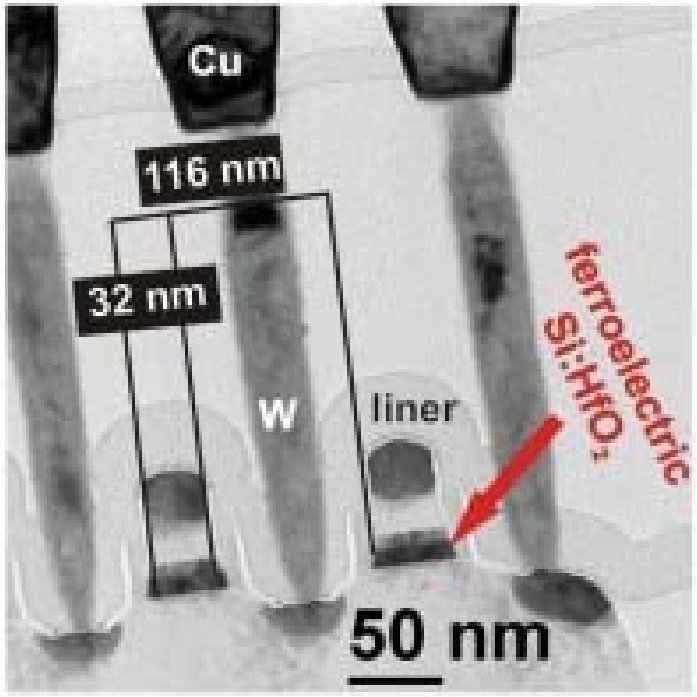
nonvolatile

To read, try to write a 0,
if a current flows, it was a 1.

Ferroelectric RAM



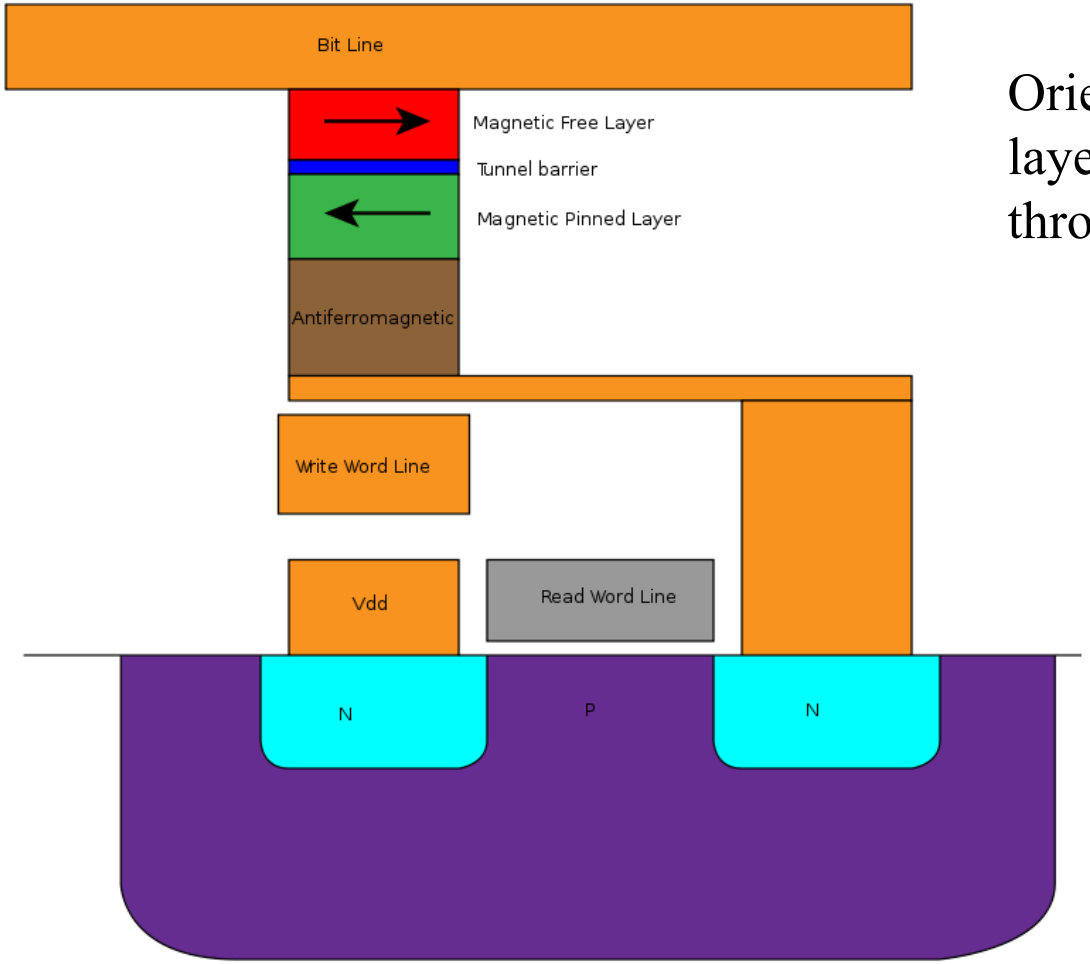




http://baldengineering.blogspot.co.at/2013_12_01_archive.html

Magnetic memory

In MRAM the resistance depends on whether the magnetic layers are parallel or antiparallel.

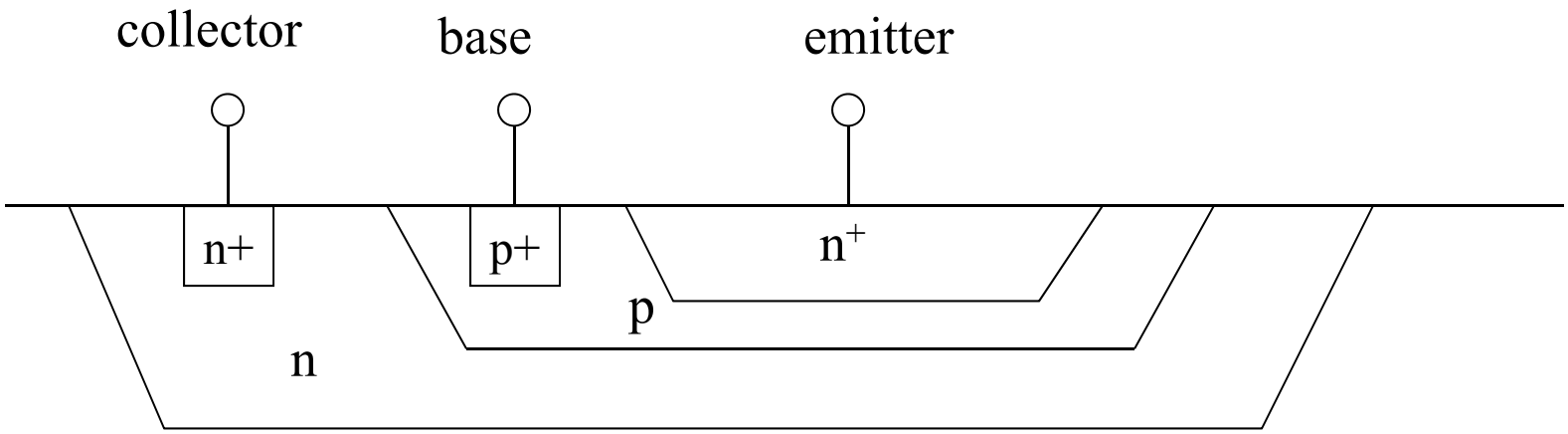


Orientaion of the magnetic free layer is set by sending a current through the bit and word lines.

nonvolatile

bipolar transistors

npn transistor

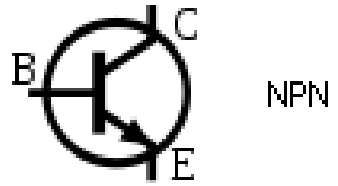


lightly doped p substrate

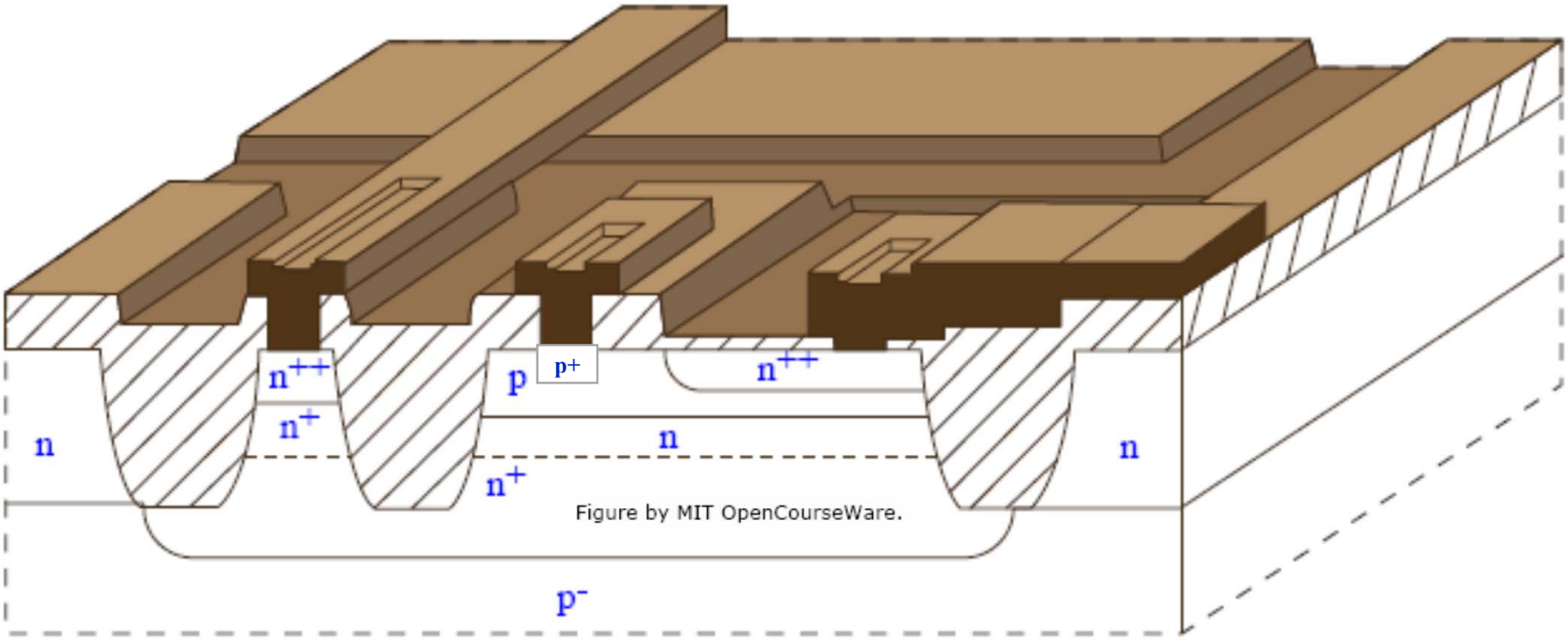
Used in front-end high-frequency receivers (mobile telephones).

bipolar transistors

PNP

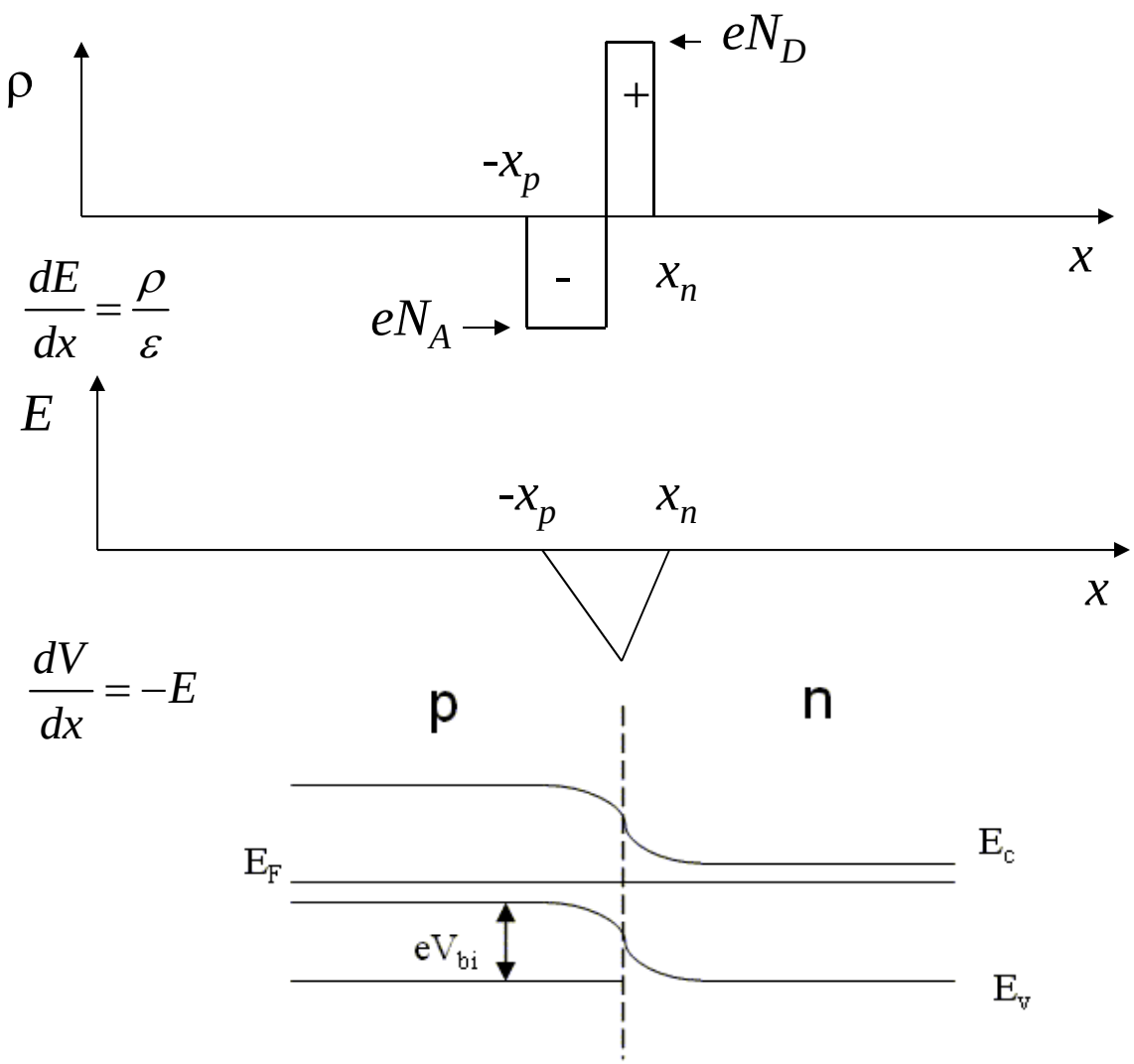


NPN



Oxide isolated integrated BJT - a modern process

abrupt junction



$$eV_{bi} = k_B T \ln\left(\frac{N_D N_A}{n_i^2}\right)$$

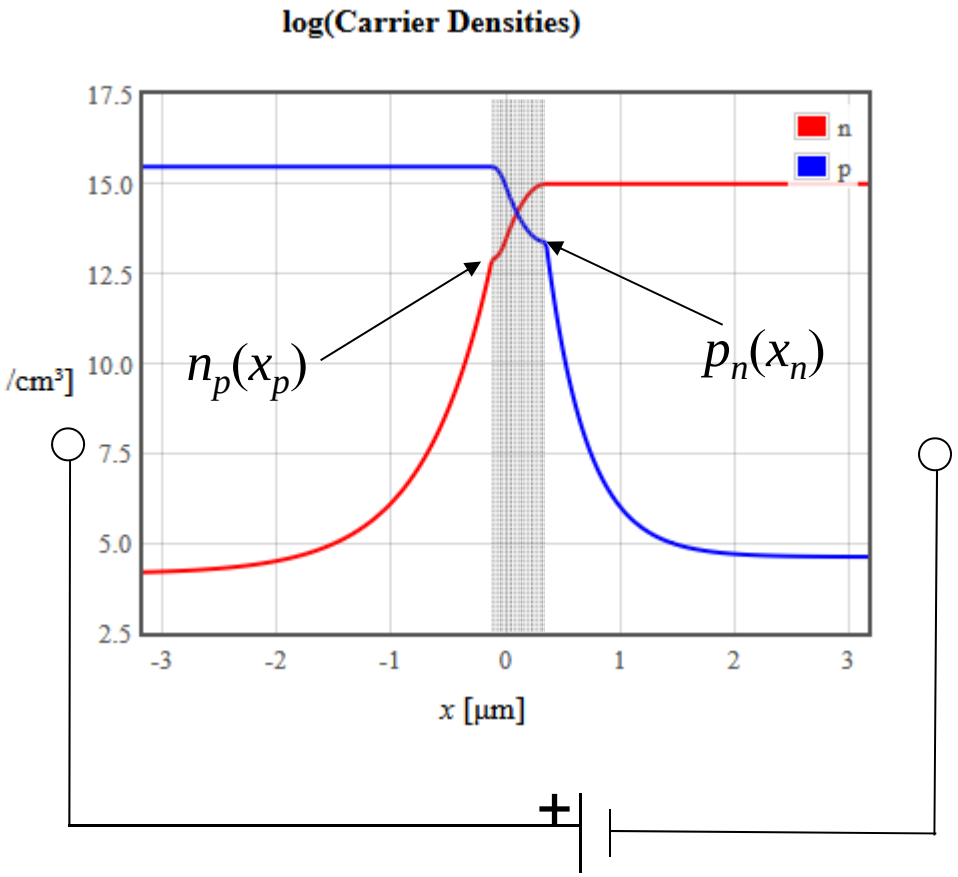
$$E = -\frac{eN_A}{\varepsilon}\left(x + x_p\right) \qquad -x_p > x > 0$$

$$E = \frac{eN_D}{\varepsilon}\left(x - x_n\right) \qquad 0 > x > x_n$$

$$V = \frac{eN_A}{\varepsilon}\left(\frac{x^2}{2} + xx_p\right) \qquad -x_p > x > 0$$

$$V = \frac{-eN_D}{\varepsilon}\left(\frac{x^2}{2} - xx_n\right) \qquad 0 > x > x_n$$

Forward bias, V > 0



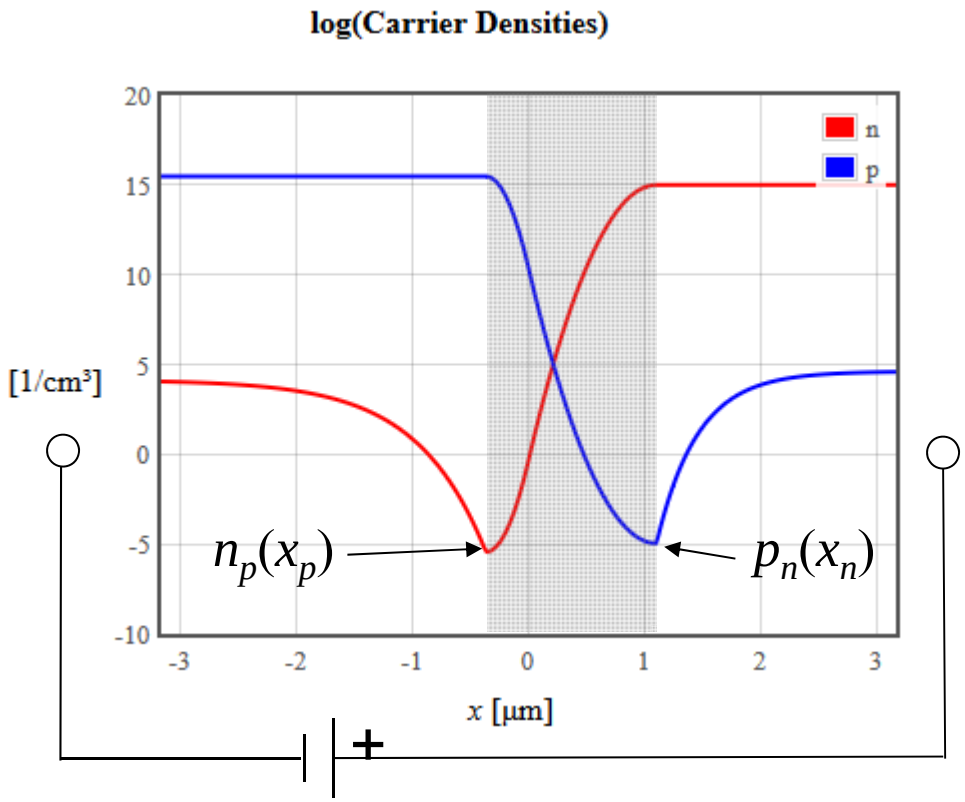
Electrons and holes are driven towards the junction.
The depletion region becomes narrower

$$n_p(x_p) = N_D \exp\left(\frac{-e(V_{bi} - V)}{k_B T}\right)$$

$$p_n(x_n) = N_A \exp\left(\frac{-e(V_{bi} - V)}{k_B T}\right)$$

Minority electrons are injected into the p-region
Minority holes are injected into the n-region

Reverse bias, V < 0



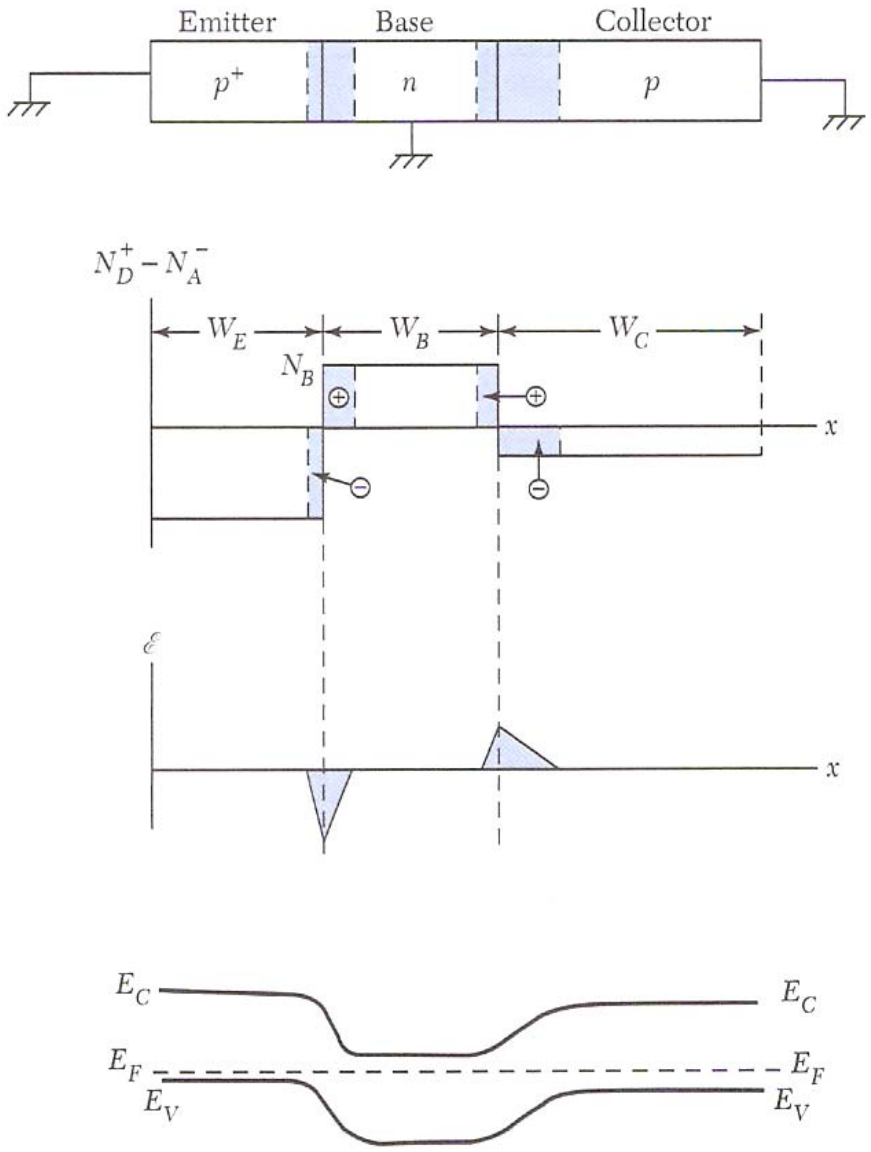
Electrons and holes are driven away from the junction.
The depletion region becomes wider

$$n_p(x_p) = N_D \exp\left(\frac{-e(V_{bi} - V)}{k_B T}\right)$$

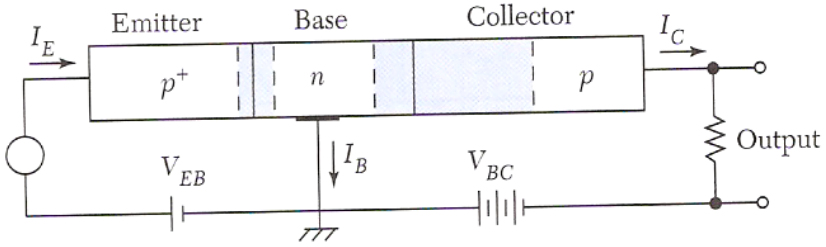
$$p_n(x_n) = N_A \exp\left(\frac{-e(V_{bi} - V)}{k_B T}\right)$$

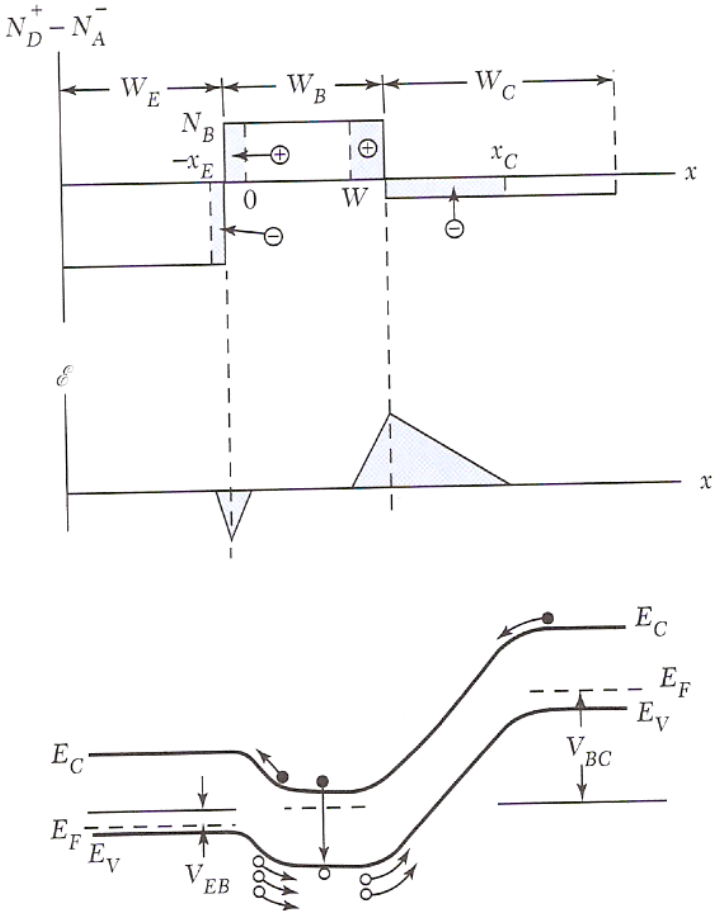
Minority electrons are extracted from the p-region by the electric field
Minority holes are extracted from the n-region by the electric field

pnp transistor, no bias



pnp transistor, forward active bias

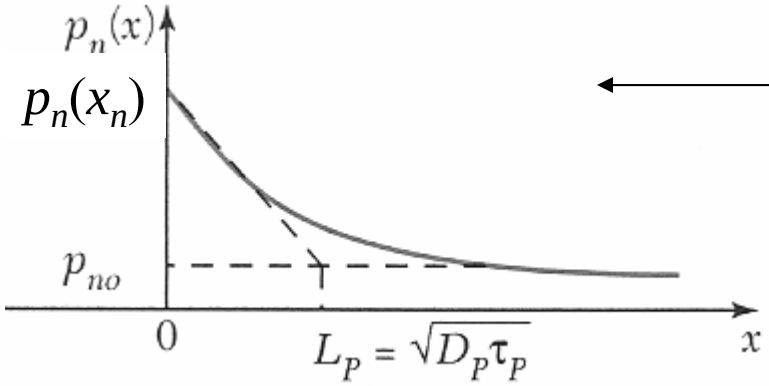




Always dissipate power due to the forward bias

The base-emitter voltage controls the minority carriers injected from the emitter to the base. These diffuse to the base-collector junction and are swept into the collector.

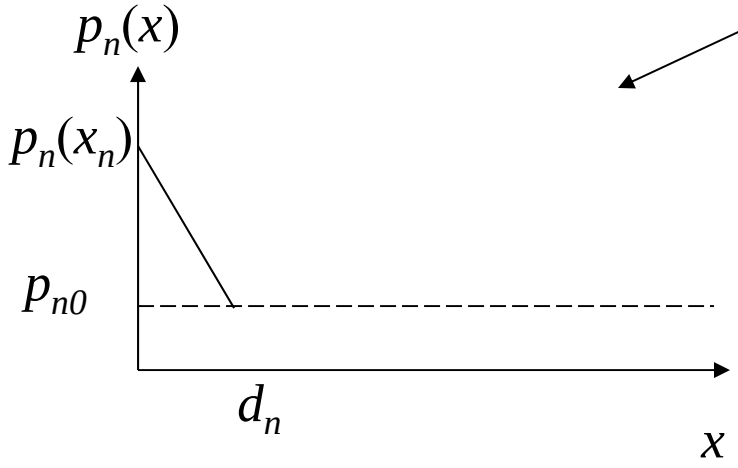
Long/Short diode



Long diode $d_n >> L_p$

Short diode

$d_n << L_p$

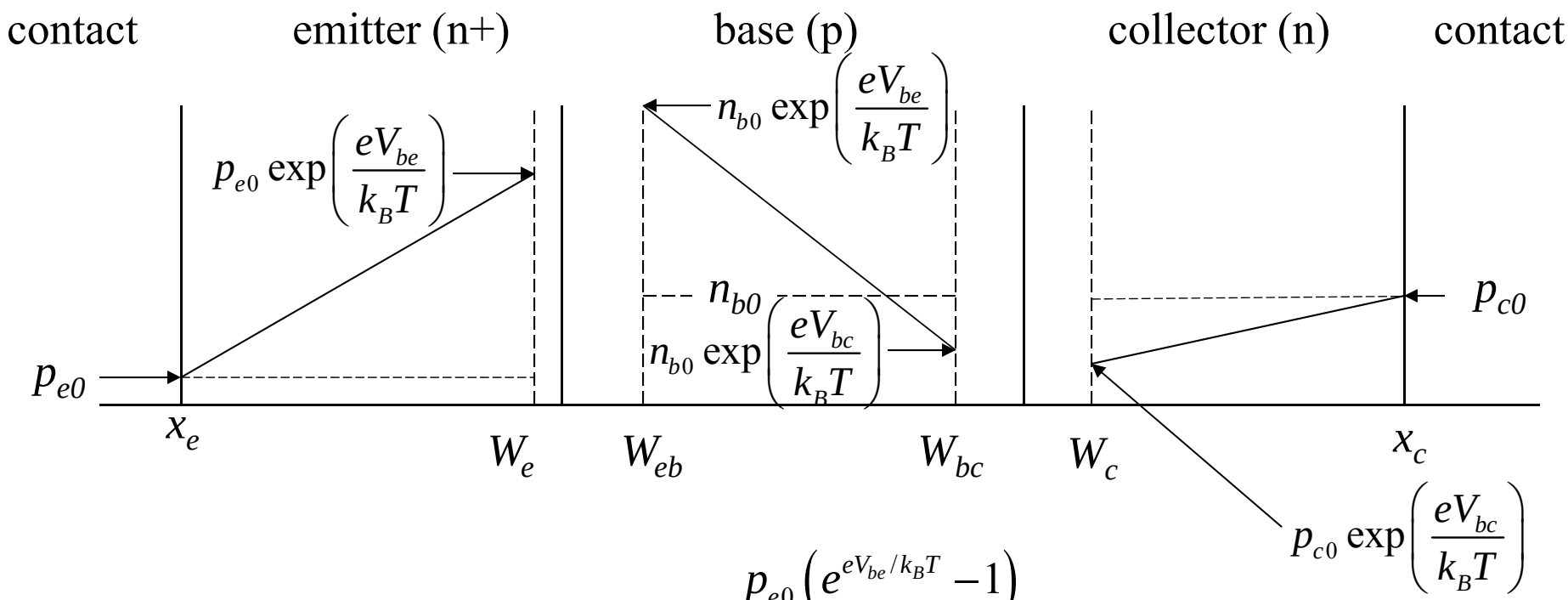


Metal contact is much closer to the depletion region than the diffusion length

$$J_{diff,p} = eD_p \frac{dp}{dx}$$

$$J_{diff,p} = eD_p \frac{dp}{dx} = eD_p \frac{\left(p_n(x_n) - p_{n0}\right)}{d_n}$$

Minority carrier concentration



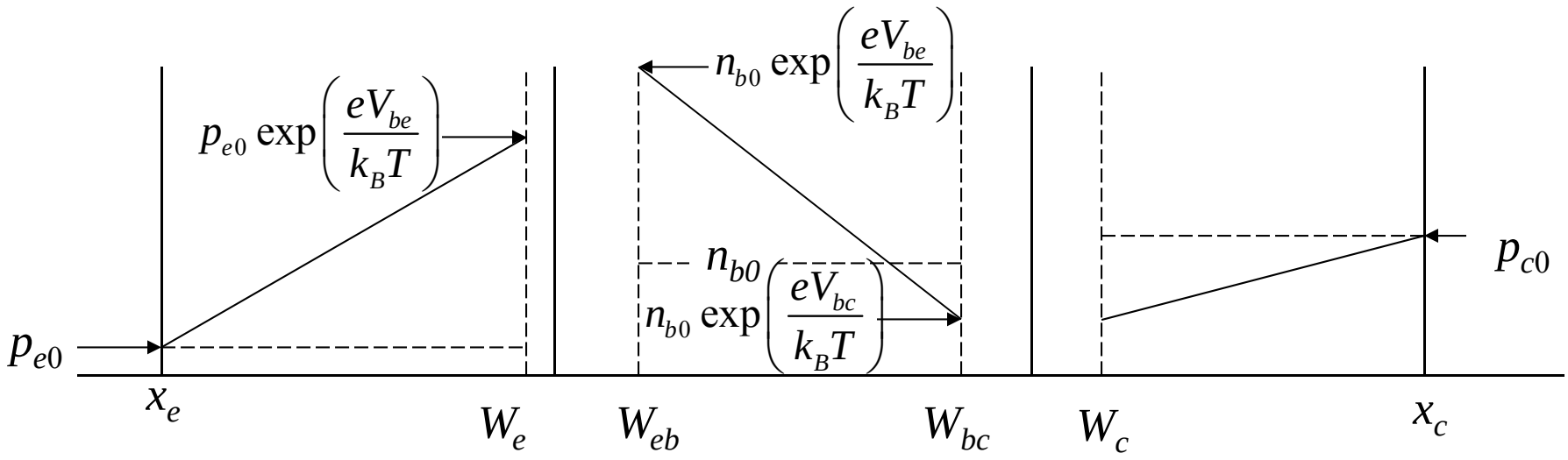
$$I_{Ep} = eA_{be}D_p \frac{p_{e0}\left(e^{eV_{be}/k_BT} - 1\right)}{W_e - x_e}$$

$$I_{En} = -eA_{be}D_n \frac{n_{b0}\left(e^{eV_{be}/k_BT} - e^{eV_{bc}/k_BT}\right)}{W_{bc} - W_{be}}$$

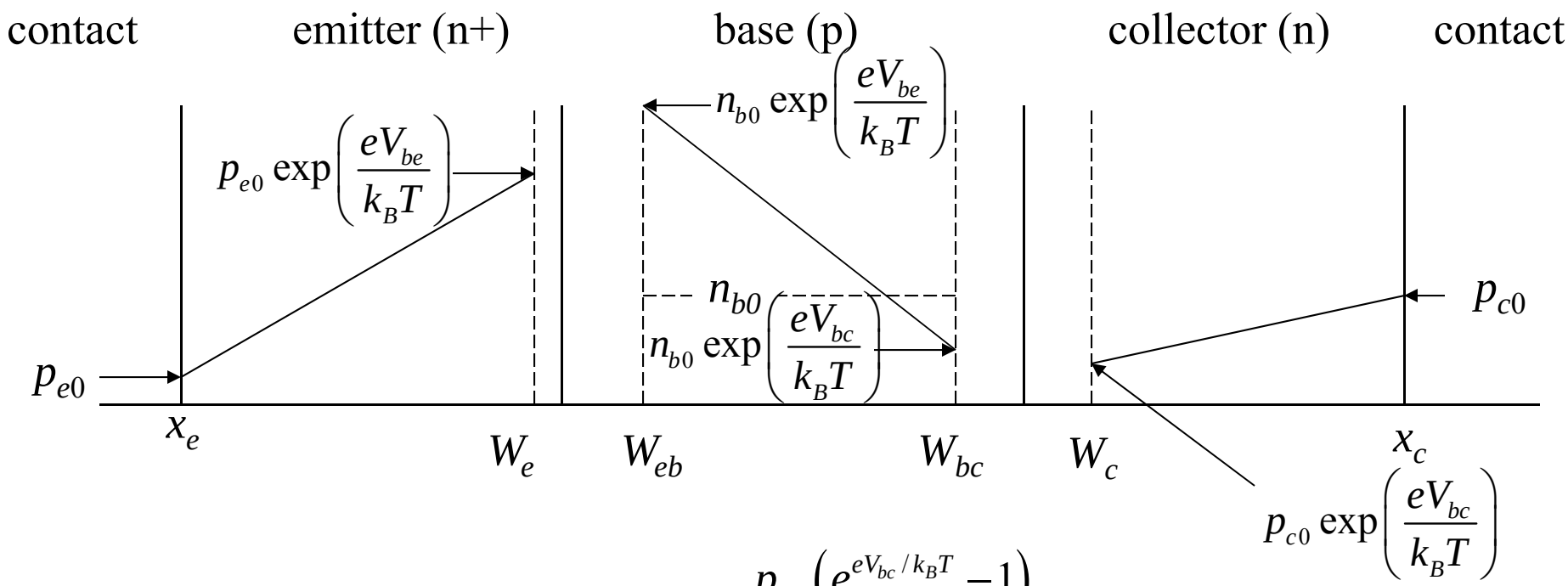
Emitter current

$$I_E = I_{En} + I_{Ep} = \left[\frac{eA_{be}D_p p_{e0}}{W_{eb} - x_e} + \frac{eA_{be}D_n n_{b0}}{W_{bc} - W_{be}} \right] \left(e^{eV_{be}/k_BT} - 1 \right) - \frac{eA_{be}D_n n_{b0}}{W_{bc} - W_{be}} \left(e^{eV_{bc}/k_BT} - 1 \right)$$

$$I_E = I_{ES} \left(e^{eV_{be}/k_BT} - 1 \right) - \alpha_R I_{CS} \left(e^{eV_{bc}/k_BT} - 1 \right)$$



Collector current



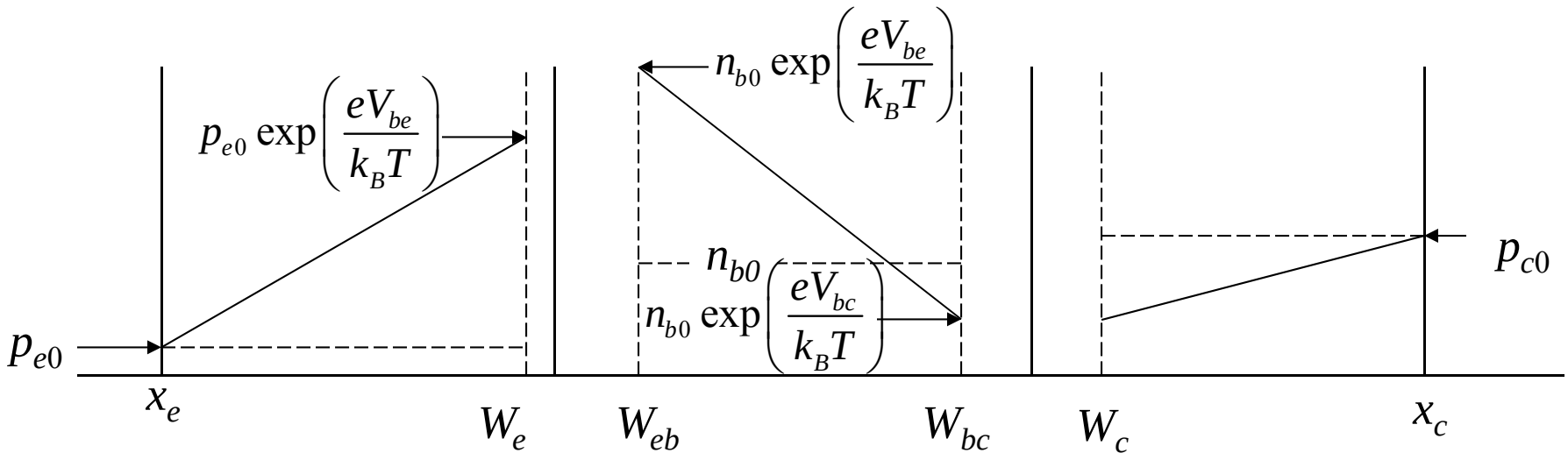
$$I_{cp} = -eA_{bc}D_p \frac{p_{c0}\left(e^{eV_{bc}/k_BT} - 1\right)}{x_c - W_c}$$

$$I_{cn} = -eA_{bc}D_n \frac{n_{b0}\left(e^{eV_{be}/k_BT} - e^{eV_{bc}/k_BT}\right)}{W_{bc} - W_{eb}}$$

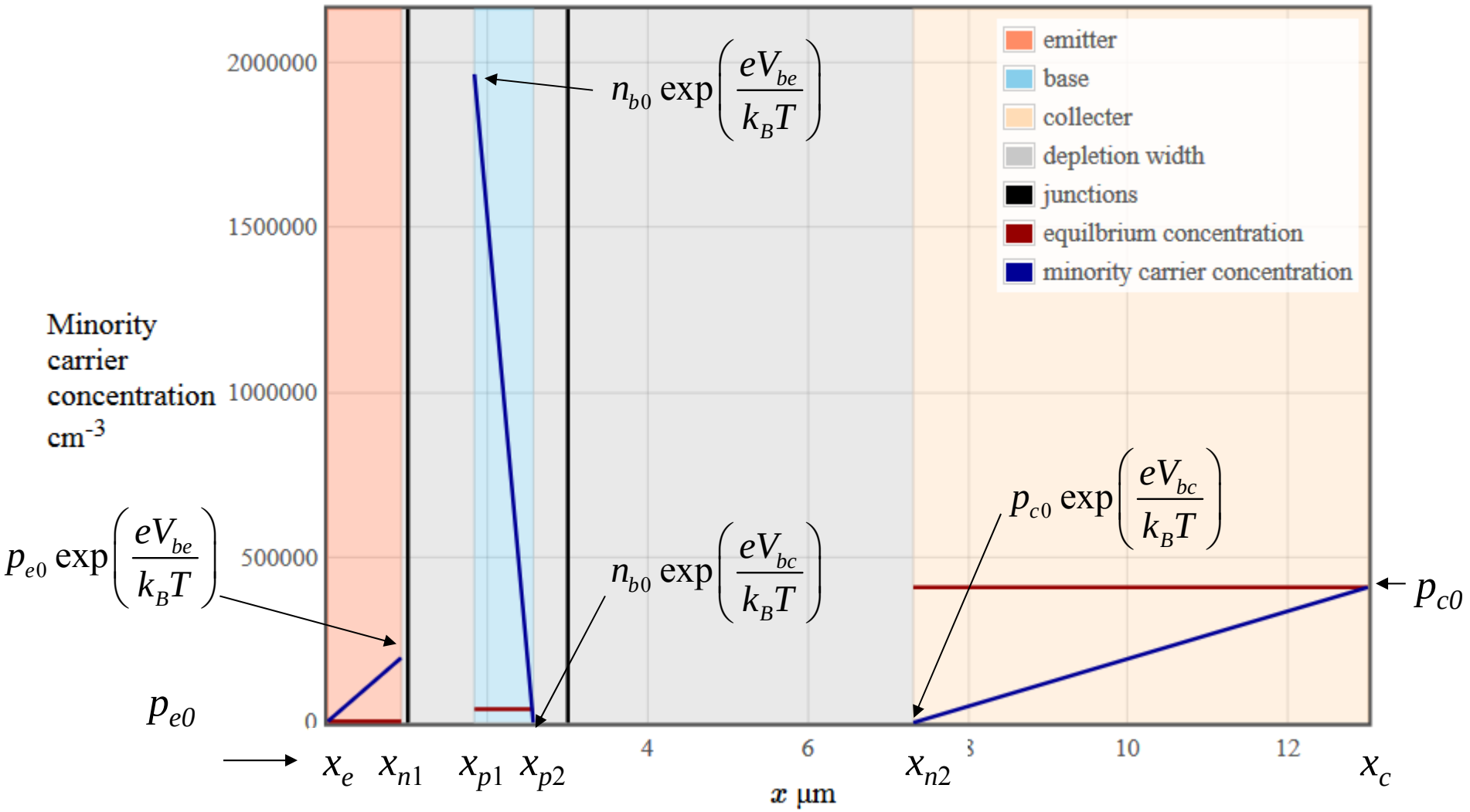
Collector current

$$I_c = I_{cp} + I_{cn} = \frac{eA_{bc}D_n n_{b0}}{W_{bc} - W_{be}}\left(e^{eV_{be}/k_BT} - 1\right) - \left[\frac{eA_{bc}D_p p_{c0}}{x_c - W_c} + \frac{eA_{bc}D_n n_{b0}}{W_{bc} - W_{be}}\right]\left(e^{eV_{bc}/k_BT} - 1\right)$$

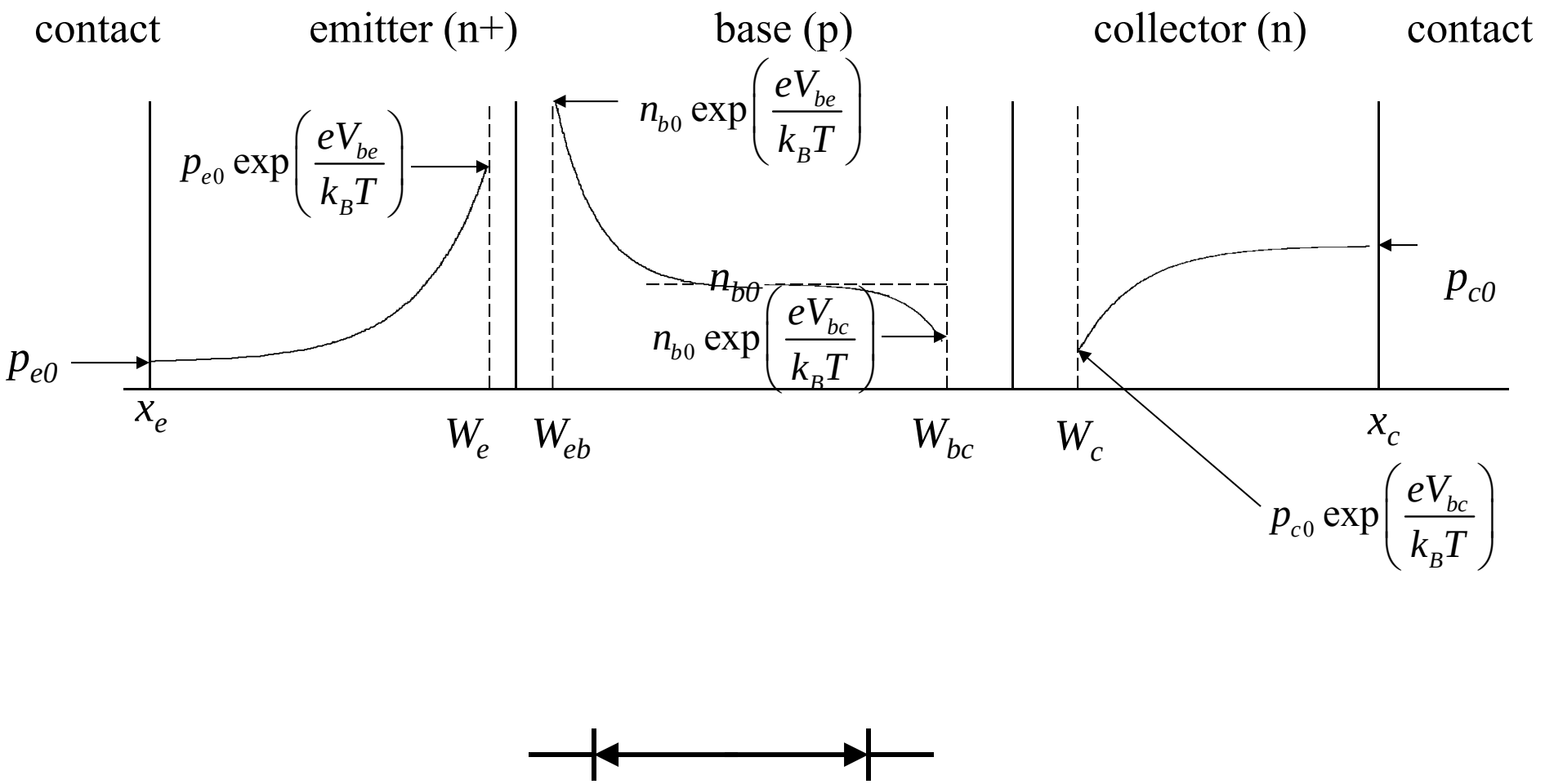
$$I_c = I_{cp} + I_{cn} = \alpha_F I_{ES}\left(e^{eV_{be}/k_BT} - 1\right) - I_{CS}\left(e^{eV_{bc}/k_BT} - 1\right)$$



Minority carrier concentration



Not an npn transistor

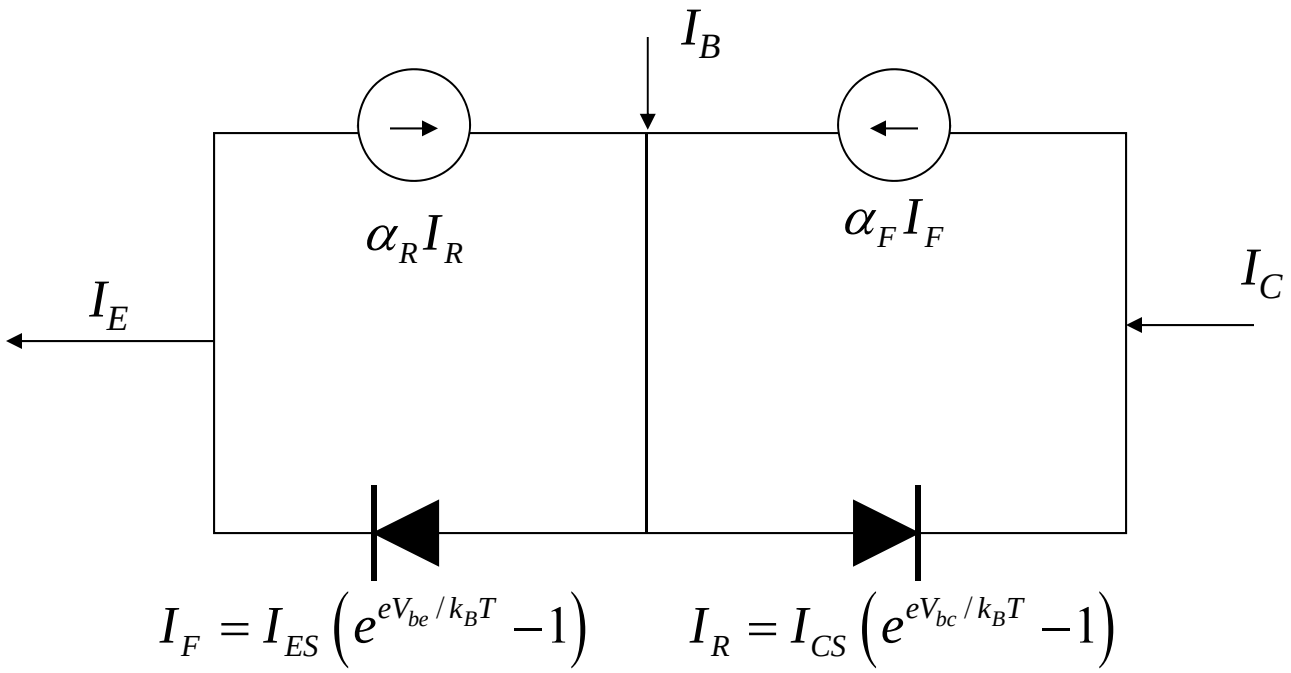


Ebers-Moll model

$$I_E = I_{ES}\left(e^{eV_{be}/k_BT} - 1\right) - \alpha_R I_{CS}\left(e^{eV_{bc}/k_BT} - 1\right)$$

$$I_C = \alpha_F I_{ES}\left(e^{eV_{be}/k_BT} - 1\right) - I_{CS}\left(e^{eV_{bc}/k_BT} - 1\right)$$

$$I_B = I_E - I_C$$



Emitter efficiency

$$\gamma_e = \frac{I_{En}}{I_{En} + I_{Ep}} = \frac{1}{1 + I_{Ep} / I_{En}}$$ ← for npn

$$I_{Ep} = eA_{be} D_p \frac{p_{e0}\left(e^{eV_{be}/k_B T} - 1\right)}{W_{eb} - x_e}$$

$$I_{En} = -eA_{be} D_n \frac{n_{b0}\left(e^{eV_{be}/k_B T} - e^{eV_{bc}/k_B T}\right)}{W_{bc} - W_{be}}$$

For $\gamma_e \sim 1$, $W_{bc} - W_{be} << L_b$, $W_{eb} - x_e$ and $n_{b0} >> p_{e0}$

neutral base width

$\frac{n_i^2}{N_{Ab}}$

$\frac{n_i^2}{N_{De}}$

Small base width and heavy emitter doping

Base transport factor

$$B = \frac{I_c}{I_{En}}$$

ratio of the injected current to the collected current

recombination in the base would reduce the base transport factor

A thin base with low doping results in a base transport factor ~ 1

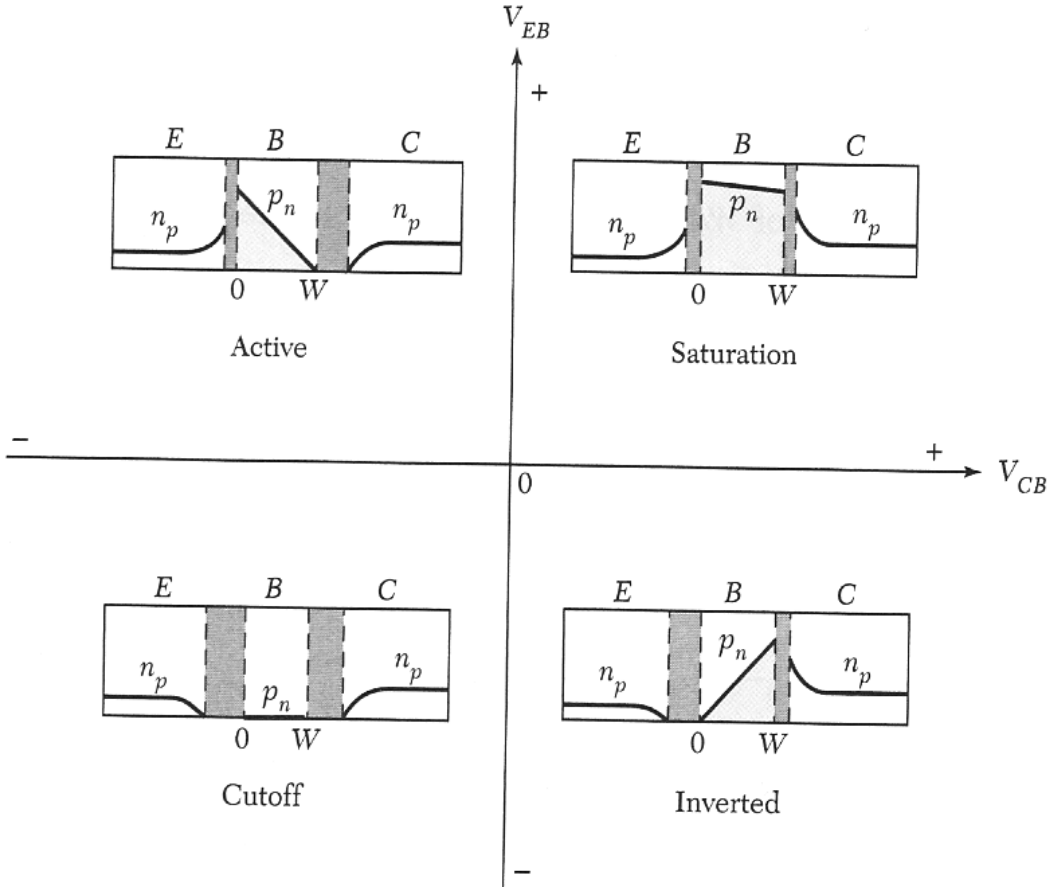
Current transfer ratio

$$\alpha = \frac{I_C}{I_E} = B\gamma_e$$

$\alpha \sim 1$ for a good BJT

Transistor modes

1. Forward active: emitter-base **forward**, base-collector **reverse**
2. Saturation: emitter-base **forward**, base-collector **forward**
3. Reverse active: emitter-base **reverse**, base-collector **forward**
4. Cut-off: emitter-base **reverse**, base-collector **reverse**

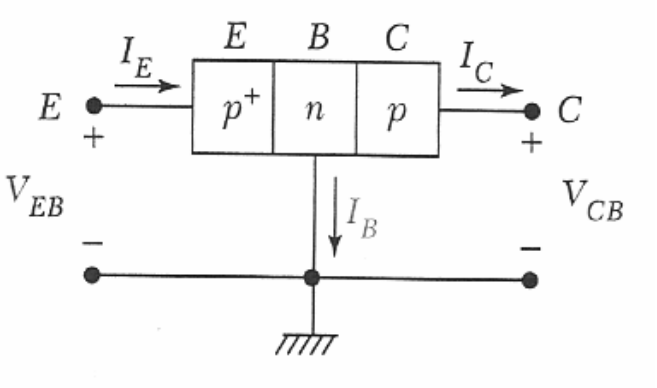


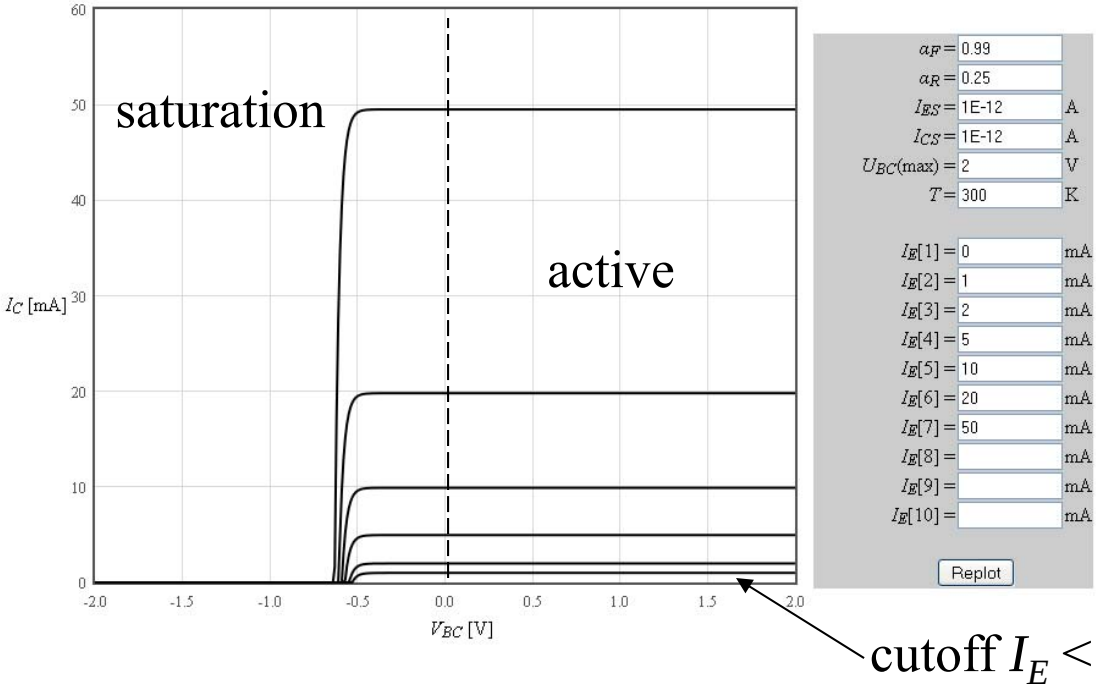
Common base configuration

$$I_E = I_{ES}\left(e^{eV_{be}/k_BT} - 1\right) - \alpha_R I_{CS}\left(e^{eV_{bc}/k_BT} - 1\right)$$

solve for V_{be}

$$I_c = \alpha_F I_{ES}\left(e^{eV_{be}/k_BT} - 1\right) - I_{CS}\left(e^{eV_{bc}/k_BT} - 1\right)$$





cutoff $I_E < 0$

http://lamp.tu-graz.ac.at/~hadley/psd/L13/commonbase/pnp_current.html