Heterojunction bipolar transistors, thyristors, and Latch-up
Heterojunction bipolar transistors

Emitter contact

$\begin{align*}
n^+ - \text{GaAs} \\
n - \text{AlGaAs}
\end{align*}$

$p^+ - \text{GaAs}$

Collector contact

$\begin{align*}
n - \text{GaAs}
\end{align*}$

Sub - collector

Semiinsulating GaAs substrate

$\Delta E_c$

$\Delta E_v$
Heterojunction bipolar transistor

small emitter-base capacitance to increase speed
HBT current gain

\[ I_C = \beta I_B \]

\[ \beta = \frac{\alpha}{1 - \alpha} \approx \frac{n_{B0}}{p_{E0}} \] (nnp)

Higher doping in the emitter makes the minority carrier concentration lower in the emitter.

\[ n_{B0} = \frac{n_i^2}{N_A} = \frac{N_C N_v \exp(-E_{gB} / k_B T)}{N_A} \]

\[ p_{E0} = \frac{n_i^2}{N_D} = \frac{N'_C N'_v \exp(-E_{gE} / k_B T)}{N_D} \]

If the emitter and the base have different band gaps

\[ \beta = \frac{N_E}{N_B} \frac{N_c N_v}{N'_c N'_v} \exp\left(\frac{\Delta E_g}{k_B T}\right) \sim 100000 \]
A HBT has an emitter bandgap of 1.62 and a base bandgap of 1.42. A BJT has an emitter bandgap of 1.42 and a base bandgap of 1.42. Both have an emitter doping of $10^{18}$ cm$^{-3}$ and a base doping of $10^{15}$ cm$^{-3}$. How much larger is the gain in the HBT?

\[
\frac{\beta_{\text{HBT}}}{\beta_{\text{BJT}}} = \exp\left(\frac{\Delta E_g}{k_B T}\right) = \exp\left(\frac{1.62 - 1.42}{0.0259}\right) = 2257
\]
HBT

Trade off gain for higher speed

Higher base doping
  lower base resistance
  reduced Early effect
  less trouble with punch through
  base can be made thinner -> faster transistors

Because of higher base doping, a higher collector doping is possible without punch through
  lower collector resistance
HBT current gain

band discontinuity reduces emitter efficiency
Graded layer emitter and base improve performance

Si/SiGe
AlInAs/InGaAs
Heterojunction bipolar transistors

Fastest InP/InGaAs HBT's have an $f_T$ of 710 GHz.

Higher doping in the base allows for a thinner base without punch through and lower base resistance and thus higher frequency operation.
Microwave engineering

Electronics: $L \ll \lambda$, $f \approx 10$ GHz

Microwave: $\lambda < L$, $10$ GHz $< f < 1$ THz

TeraHertz: $\lambda \ll L$, $1$ THz $< f < 100$ THz

Optics: $\lambda \ll L$, $100$ THz
Thyristors

Forward blocking

Forward conducting

Reverse blocking
Thyristors

\[ \beta_1 \beta_2 > 1 \]

Used for switching high currents or voltages
Latch-up

Both BJT's conduct, creating a low resistance path between $V_{dd}$ and GND. The product of the gains of the two transistors in the feedback loop, is greater than one. The result of latchup is at the minimum a circuit malfunction, and in the worst case, the destruction of the device.

http://www.ece.drexel.edu/courses/ECE-E431/latch-up/latch-up.html
If the p-concentration in the channel is low, electrons emitted into the channel by the forward biased junction diffuse across the channel without recombining.
Interdigitated contacts in power transistors
IGBT - Insulated Gate Bipolar Transistor

An IGBT is a combination of an insulated gate FET and a bipolar transistor. It is primarily used for switching high power loads.

Used to switch large currents (in electric cars or trains).

http://lampx.tugraz.at/~hadley/psd/L13/igbt.html
BiCMOS

Only one additional step to CMOS is needed for BiCMOS

Bipolar junction transistors:
- high speed
- high gain
- low output impedance
- good for analog amplifiers

CMOS
- high impedance
- low power logic

Figure 27.6 Simple BiCMOS technology: triple diffused-type bipolar transistor added to a CMOS process with minimal extra steps; only p-base diffusion mask is added to CMOS process flow. Reproduced from Alvarez (1989) by permission of Kluwer Fransila

See: http://www.iue.tuwien.ac.at/phd/puchner/node48_app.html
Antimony (Sb) has a low vapor pressure and won't evaporate during the subsequent CVD step.
Epi-growth

Remove oxide
Clean surface
Silicon epitaxy
CVD SiH₄ + PH₃

p-Si

n-eqi

n+ subcollector
Collector Contact

p-Si

n+ subcollector

n-epi

n+

Deposit oxide
Spin resist
Expose
Develop
Etch Oxide
Strip resist
Implant collector contact n+
Anneal

p-Si
Guard ring

Deposit oxide
Spin resist
Expose
Develop
Etch Oxide
Strip resist
Implant collector contact p+
Anneal

p-Si

n+ subcollector

n-epl

p+ n+
p+
Deposit oxide
Spin resist
Exposure
Develop
Etch Oxide
Strip resist
Implant base
Anneal
n+ emitter

n+ subcollector

Deposit oxide
Spin resist
Exposure
Develop
Etch Oxide
Strip resist
Implant base
Anneal

p-Si

n+ emitter

n+ subcollector

Deposit oxide
Spin resist
Exposure
Develop
Etch Oxide
Strip resist
Implant base
Anneal

p-Si

n+ emitter

n+ subcollector

Deposit oxide
Spin resist
Exposure
Develop
Etch Oxide
Strip resist
Implant base
Anneal

p-Si

n+ emitter

n+ subcollector

Deposit oxide
Spin resist
Exposure
Develop
Etch Oxide
Strip resist
Implant base
Anneal

p-Si